

# **Little Logic**

# Data Book



November 2001

**Logic Products** 

# Little Logic Data Book







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#### INTRODUCTION

Little-logic devices from Texas Instruments help complete your design puzzle. With their extremely small size, they enable you to simplify design routing, maximize ASIC design development, and significantly reduce redesign time, effectively extending the life of your product. With the miniaturization of portable electronics, these devices are ideal for your applications where board space is limited. Little logic is available as single gates, dual gates, or triple gates.

#### **Single Gates**

Single gates are now available in a 5-ball NanoStar™ (YEA) package, the smallest single-gate logic package available. Other package options include the 5-pin DBV (SOT-23) package and the ultra-small 5-pin DCK (SC-70) package for maximum board savings. Single-gate logic functions are offered in a variety of technologies for your design needs. For your 5-V design, use AHC1G/AHCT1G (Advanced High-Speed CMOS). AHCT1G devices have TTL inputs, enabling backward compatibility with TTL switching standards. LVC1G (Low-Voltage CMOS) should be used in your low-voltage applications where power savings are essential. TI understands future needs will require even lower voltage/power operation. To meet these new challenges, we proudly offer the first 1.8-V logic solution in our AUC1G (Advanced Ultra Low-Voltage CMOS) devices. CBT1G (Crossbar Technology) allows the flexibility of implementing a single high-speed line switch between two ports.

#### **Dual and Triple Gates**

There are two package options available, the 8-pin DCT (SM-8) and the 8-pin DCU (US-8). Dual gates result from placing two 2-input, 1-output functions, such as AND, OR, NOR, etc., in these packages. When 1-input, 1-output functions, such as inverters and buffers, are placed in an 8-pin package, a "bonus" gate results in a triple gate. In addition, 8-pin packages allow us to offer a D-type flip-flop and a 2-line to 1-line data selector/multiplexer, previously not available in such a small package. LVC dual- and triple-gate releases are in progress.

#### **Introducing AUC**

AUC is the industry's first logic family that is optimized for 1.8-V systems with operation from sub-1 V (0.8 V) to 3.6 V. This family meets a variety of demands that have been placed on digital electronic designs, including the move to lower supply voltages, faster speeds, smaller device sizes, and lower power consumption, without compromising signal integrity. AUC was developed to meet design parameters for advanced systems, such as telecommunications equipment, high-performance workstations, PCs and networking servers, and next-generation portable and consumer electronics. As designers convert core processors, ASICs, and memory to lower-voltage technologies, they need the supporting low-voltage logic functions AUC provides.

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#### INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

#### operating conditions and characteristics (in sequence by letter symbols)

C<sub>i</sub> Input capacitance

The capacitance of an input terminal of the device

C<sub>io</sub> Input/output capacitance

The capacitance of an input/output (I/O) terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

C<sub>o</sub> Output capacitance

The capacitance of an output terminal of the device with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

C<sub>pd</sub> Power dissipation capacitance

Used to determine the no-load dynamic power dissipation per logic function (see individual circuit pages):  $P_D = C_{pd} V_{CC}^2 f + I_{CC} V_{CC}$ 

f<sub>max</sub> Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification

I<sub>BHH</sub> Bus-hold high sustaining current

The bus-hold circuit can source at least the minimum high sustaining current at  $V_{IH}$  min.  $I_{BHH}$  should be measured after raising  $V_{IN}$  to  $V_{CC}$  and then lowering it to  $V_{IH}$  min.

I<sub>BHL</sub> Bus-hold low sustaining current

The bus-hold circuit can sink at least the minimum low sustaining current at  $V_{IL}$  max.  $I_{BHL}$  should be measured after lowering  $V_{IN}$  to GND and then raising it to  $V_{IL}$  max.

I<sub>BHHO</sub> Bus-hold high overdrive current

An external driver must sink at least I<sub>BHHO</sub> to switch this node from high to low.

I<sub>BHLO</sub> Bus-hold low overdrive current

An external driver must source at least I<sub>BHI O</sub> to switch this node from low to high.

I<sub>CC</sub> Supply current

The current into\* the V<sub>CC</sub> supply terminal of an integrated circuit

∆I<sub>CC</sub> Supply current change

The increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or  $V_{CC}$ 

I<sub>CEX</sub> Output high leakage current

The maximum leakage current into\* an output that is in a high state and  $V_O = V_{CC}$ 

I<sub>l(hold)</sub> Input hold current

The input current that holds the input at the previous state when the driving device goes to the high-impedance state

\*Current out of a terminal is given as a negative value.



#### GLOSSARY SYMBOLS, TERMS, AND DEFINITIONS

#### I<sub>IH</sub> High-level input current

The current into\* an input when a high-level voltage is applied to that input

#### I<sub>IL</sub> Low-level input current

The current into\* an input when a low-level voltage is applied to that input

#### Input/output power-off leakage current

The maximum leakage current into\* an input or output terminal of the device with the specified voltage applied to the terminal and  $V_{CC} = 0 \text{ V}$ 

#### I<sub>OH</sub> High-level output current

The current into\* an output with input conditions applied that, according to the product specification, establishes a high level at the output

#### I<sub>OHS</sub> Static high-level output current

The static and testable current into\* a DOC™ circuit output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive current is not specified for devices with DOC circuit outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

#### I<sub>OL</sub> Low-level output current

The current into\* an output with input conditions applied that, according to the product specification, establishes a low level at the output

#### I<sub>OLS</sub> Static low-level output current

The static and testable current into\* a DOC circuit output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive current is not specified for devices with DOC circuit outputs because of its transient nature; however, it is similar to the dynamic drive current that is available from a high-drive (nondamping resistor) standard-output device.

#### I<sub>OZ</sub> Off-state (high-impedance state) output current (of a 3-state output)

The current flowing into\* an output with the input conditions applied that, according to the product specification, establishes the high-impedance state at the output

#### I<sub>OZPD</sub> Power-down off-state (high-impedance state) output current (of a 3-state output)

The current flowing into\* an output that is switched to or held in the high-impedance state as the device is being powered down to  $V_{CC} = 0 \text{ V}$ 

#### I<sub>OZPU</sub> Power-up off-state (high-impedance state) output current (of a 3-state output)

The current flowing into\* an output that is switched to or held in the high-impedance state as the device is being powered up from  $V_{CC} = 0 \text{ V}$ 

#### jitter Jitter

Dispersion of a time parameter of the pulse waveforms in a pulse train with respect to a reference time, interval, or duration. Unless otherwise specified by a mathematical adjective, peak-to-peak jitter is assumed.

#### jitter(RMS) RMS jitter

The root mean square jitter, one-sixth of the maximum peak-to-peak jitter

<sup>\*</sup>Current out of a terminal is given as a negative value. DOC is a trademark of Texas Instruments.



#### SR Slew rate

The average rate of change (i.e., V/ns) for a waveform that is changing from one defined logic level to another defined logic level

#### t<sub>a</sub> Access time

The time interval between the application of a specified input pulse and the availability of valid signals at an output

#### t<sub>c</sub> Clock cycle time

Clock cycle time is 1/f<sub>max</sub>

#### t<sub>dis</sub> Disable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from either of the defined active levels (high or low) to the high-impedance (off) state

NOTE: For 3-state outputs,  $t_{dis} = t_{PHZ}$  or  $t_{PLZ}$ . Open-collector outputs change only if they are low at the time of disabling, so  $t_{dis} = t_{PLH}$ .

#### t<sub>en</sub> Enable time (of a 3-state or open-collector output)

The propagation time between the specified reference points on the input and output voltage waveforms with the output changing from the high-impedance (off) state to either of the defined active levels (high or low)

NOTE: In the case of memories, this is the access time from an enable input (e.g.,  $\overline{OE}$ ). For 3-state outputs,  $t_{en} = t_{PZH}$  or  $t_{PZL}$ . Open-collector outputs change only if they are responding to data that would cause the output to go low, so  $t_{en} = t_{PHL}$ .

#### t<sub>f</sub> Fall time

The time interval between two reference points (90% and 10%, unless otherwise specified) on a waveform that is changing from the defined high level to the defined low level

#### th Hold time

The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal

NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is to be expected.

2. The hold time may have a negative value, in which case, the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is to be expected.

#### t<sub>pd</sub> Propagation delay time

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ( $t_{pd} = t_{pHI}$  or  $t_{pIH}$ )

#### t<sub>PHL</sub> Propagation delay time, high-to-low level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level

#### t<sub>PHZ</sub> Disable time (of a 3-state output) from high level

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined high level to the high-impedance (off) state



#### Propagation delay time, low-to-high level output <sup>t</sup>PLH

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level

#### Disable time (of a 3-state output) from low level t<sub>PLZ</sub>

The time interval between the specified reference points on the input and the output voltage waveforms with the 3-state output changing from the defined low level to the high-impedance (off) state

#### Enable time (of a 3-state output) to high level <sup>t</sup>PZH

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined high level

#### Enable time (of a 3-state output) to low level $t_{PZL}$

The time interval between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the high-impedance (off) state to the defined low level

#### t<sub>r</sub> Rise time

The time interval between two reference points (10% and 90%, unless otherwise specified) on a waveform that is changing from the defined low level to the defined high level

#### Input skew t<sub>sk(i)</sub>

The difference between any two propagation delay times that originate at different inputs and terminate at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. t<sub>sk(i)</sub> describes the ability of the gate to shape the pulse to the same duration, regardless of the input used as the controlling input.

#### Limit skew t<sub>sk(l)</sub>

The difference between 1) the greater of the maximum specified values of tpl H and tpHI and 2) the lesser of the minimum specified values of tpl H and tpHI. Limit skew is not directly observed on a device. It is calculated from the data-sheet limits for t<sub>PLH</sub> and t<sub>PHL</sub>. t<sub>sk(I)</sub> quantifies for the designer how much variation in propagation delay time is induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, t<sub>sk(l)</sub> also accounts for process variation. In fact, all other skew specifications [ $t_{sk(0)}$ ,  $t_{sk(j)}$ ,  $t_{sk(p)}$ , and  $t_{sk(pr)}$ ] are subsets of  $t_{sk(l)}$ ; they are never greater than  $t_{sk(l)}$ .

#### **Output skew** t<sub>sk(o)</sub>

The skew between specified outputs of a single logic device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads

#### Pulse skew t<sub>sk(p)</sub>

The magnitude of the time difference between the propagation delay times, tpHL and tpLH, when a single switching input causes one or more outputs to switch

#### Process skew t<sub>sk(pr)</sub>

The magnitude of the difference in propagation delay times between corresponding terminals of two logic devices when both logic devices operate with the same supply voltages, operate at the same temperature, and have identical package styles, identical specified loads, identical internal logic functions, and the same manufacturer



#### t<sub>su</sub> Setup time

The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is specified.

2. The setup time may have a negative value, in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is specified.

#### t<sub>w</sub> Pulse duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform

#### V<sub>IH</sub> High-level input voltage

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables

NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is to be expected.

#### V<sub>IK</sub> Input clamp voltage

The maximum voltage developed across an input diode with test current applied

#### V<sub>IL</sub> Low-level input voltage

An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables

NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is to be expected.

#### V<sub>OH</sub> High-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a high level at the output

#### V<sub>OHS</sub> Static high-level output voltage

The static and testable voltage at a DOC circuit output with input conditions applied that, according to the product specifications, establishes a static high level at the output. The dynamic drive voltage is not specified for devices with DOC circuit outputs because of its transient nature.

#### V<sub>OL</sub> Low-level output voltage

The voltage at an output terminal with input conditions applied that, according to product specification, establishes a low level at the output

#### V<sub>OLS</sub> Static low-level output voltage

The static and testable voltage at a DOC circuit output with input conditions applied that, according to the product specifications, establishes a static low level at the output. The dynamic drive voltage is not specified for devices with DOC circuit outputs because of its transient nature.

#### V<sub>T+</sub> Positive-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage,  $V_{T-}$ 

#### V<sub>T</sub>\_ Negative-going input threshold level

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V<sub>T+</sub>



#### **EXPLANATION OF FUNCTION TABLES**

The following symbols are used in function tables on TI data sheets:

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level ↓ = transition from high to low level

= value/level or resulting value/level is routed to indicated destination

= value/level is re-entered

X = irrelevant (any input, including transitions)Z = off (high-impedance) state of a 3-state output

a . . . h = the level of steady-state inputs A through H, respectively

Q<sub>0</sub> = level of Q before the indicated steady-state input conditions were established

 $\overline{Q}_0$  = complement of  $Q_0$  or level of  $\overline{Q}$  before the indicated steady-state input

conditions were established

 $Q_n$  = level of Q before the most recent active transition indicated by  $\downarrow$  or  $\uparrow$ 

= one high-level pulse = one low-level pulse

Toggle = each output changes to the complement of its previous level on each active

transition indicated by  $\downarrow$  or  $\uparrow$ 

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with  $\uparrow$  and/or  $\downarrow$ , this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q<sub>0</sub>, or  $\overline{Q}_0$ ), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse,  $\neg \neg \neg \neg \neg$ , the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

Among the most complex function tables are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. Below is the function table of a 4-bit bidirectional universal shift register.

#### **FUNCTION TABLE**

	INPUTS							OUTI	PUTS				
CLEAR	MO	DE	CLOCK	SEF	RIAL		PARA	LLEL		٥.	A QB QC	0-	0-
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	Α	В	С	D	QA		٠ <b>٠</b> ٠	$Q_{D}$
L	Х	Х	Х	Х	Х	Х	Х	Х	Х	L	L	L	L
Н	Х	Χ	L	Х	Х	Х	Χ	Χ	Χ	Q <sub>A0</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$
Н	Н	Н	<b>↑</b>	Х	Х	а	b	С	d	а	b	С	d
Н	L	Н	<b>↑</b>	Х	Н	Н	Н	Н	Н	Н	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$
Н	L	Н	<b>↑</b>	Х	L	L	L	L	L	L	$Q_{An}$	$Q_Bn$	$Q_{Cn}$
Н	Н	L	<b>↑</b>	Н	Х	Х	Χ	Χ	Χ	Q <sub>Bn</sub>	$Q_{Cn}$	$Q_{Dn}$	Н
Н	Н	L	<b>↑</b>	L	Х	Х	Χ	Χ	Χ	Q <sub>Bn</sub>	$Q_{Cn}$	$Q_{Dn}$	L
Н	L	L	Х	Х	Χ	Х	Χ	Χ	Χ	Q <sub>A0</sub>	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$

The first line of the table represents a synchronous clearing of the register and says that if clear is low, all four outputs will be reset low regardless of the other inputs. In the following lines, clear is inactive (high) and so has no effect.

The second line shows that so long as the clock input remains low (while clear is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of clear high and clock low was established. Since on other lines of the table only the rising transition of the clock is shown to be active, the second line implicitly shows that no further change in the outputs occurs while the clock remains high or on the high-to-low transition of the clock.

The third line of the table represents synchronous parallel loading of the register and says that if S1 and S0 are both high then, without regard to the serial input, the data entered at A is at output  $Q_A$ , data entered at B is at  $Q_B$ , and so forth, following a low-to-high clock transition.

The fourth and fifth lines represent the loading of high- and low-level data, respectively, from the shift-right serial input and the shifting of previously entered data one bit; data previously at  $Q_A$  is now at  $Q_B$ , the previous levels of  $Q_B$  and  $Q_C$  are now at  $Q_C$  and  $Q_D$ , respectively, and the data previously at  $Q_D$  is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is low and S0 is high and the levels at inputs A through D have no effect.

The sixth and seventh lines represent the loading of high- and low-level data, respectively, from the shift-left serial input and the shifting of previously entered data one bit; data previously at  $Q_B$  is now at  $Q_A$ , the previous levels of  $Q_C$  and  $Q_D$  are now at  $Q_B$  and  $Q_C$ , respectively, and the data previously at  $Q_A$  is no longer in the register. This entry of serial data and shift takes place on the low-to-high transition of the clock when S1 is high and S0 is low and the levels at inputs A through D have no effect.

The last line shows that as long as both inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady-state combination of clear high and both mode inputs low was established.

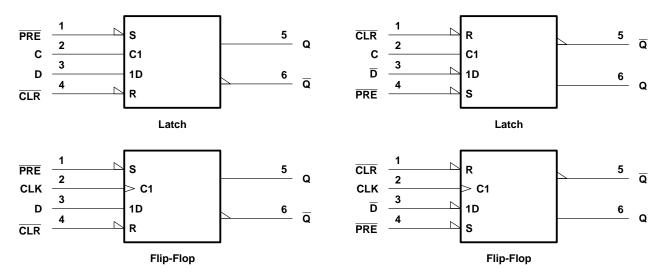
The function table functional tests do not reflect all possible combinations or sequential modes.

#### D-TYPE FLIP-FLOP AND LATCH SIGNAL CONVENTIONS

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop or latch and to draw its logic symbol based on the assumption of true data (D) inputs. Outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called  $\overline{Q}$ . An input that causes a Q output to go high or a  $\overline{Q}$  output to go low is called preset (PRE). An input that causes a  $\overline{Q}$  output to go high or a Q output to go low is called clear (CLR). Bars are used over these pin names ( $\overline{PRE}$  and  $\overline{CLR}$ ) if they are active low.

The devices on several data sheets are second-source designs, and the pin-name conventions used by the original manufacturers have been retained. That makes it necessary to designate the inputs and outputs of the inverting circuits  $\overline{D}$  and Q.

In some applications, it may be advantageous to redesignate the data input from D to  $\overline{D}$  or vice versa. In that case, all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbols. Arbitrary pin numbers are shown.



The figures show that when  $\underline{Q}$  and  $\overline{Q}$  exchange names, the preset and clear pins also exchange names. The polarity indicators ( $\sqsubseteq$ ) on  $\overline{PRE}$  and  $\overline{CLR}$  remain, as these inputs are still active low, but the presence or absence of the polarity indicator changes at D (or  $\overline{D}$ ), Q, and  $\overline{Q}$ . Pin 5 (Q or  $\overline{Q}$ ) is still in phase with the data input (D or  $\overline{D}$ ); their active levels change together.

#### **Example:** SN 2 3 5 6 8 9 10

#### **Standard Prefix**

Examples: SN – Standard Prefix

SNJ - Conforms to MIL-PRF-38535 (QML)

#### **Temperature Range**

Examples: 54 - Military

74 - Commercial

#### 3 **Family**

Blank - Transistor-Transistor Logic Examples:

> ABT - Advanced BiCMOS Technology ABTE/ETL - Advanced BiCMOS Technology/

**Enhanced Transceiver Logic** 

AC/ACT - Advanced CMOS Logic

AHC/AHCT - Advanced High-Speed CMOS Logic

ALB - Advanced Low-Voltage BiCMOS ALS - Advanced Low-Power Schottky Logic

ALVC - Advanced Low-Voltage CMOS Technology

AS - Advanced Schottky Logic

AUC - Advanced Ultra Low-Voltage CMOS Logic

AVC - Advanced Very Low-Voltage CMOS Logic

BCT - BiCMOS Bus-Interface Technology

CBT - Crossbar Technology

CBTLV - Low-Voltage Crossbar Technology CD4000 - CMOS B-Series Integrated Circuits

F - F Logic

FB - Backplane Transceiver Logic/Futurebus+

FCT - Fast CMOS TTL Logic GTL - Gunning Transceiver Logic

HC/HCT - High-Speed CMOS Logic

HSTL - High-Speed Transceiver Logic

LS - Low-Power Schottky Logic

LV - Low-Voltage CMOS Technology

LVC - Low-Voltage CMOS Technology

LVT - Low-Voltage BiCMOS Technology

PCA/PCF – I<sup>2</sup>C Inter-Integrated Circuit Applications

S - Schottky Logic

SSTL/SSTV - Stub Series-Terminated Logic TVC - Translation Voltage Clamp Logic

#### Special Features

Examples: Blank = No Special Features

C - Configurable V<sub>CC</sub> (LVCC)

D – Level-Shifting Diode (CBTD)

H - Bus Hold (ALVCH)

K - Undershoot-Protection Circuitry (CBTK)

R - Damping Resistor on Inputs/Outputs (LVCR)

S - Schottky Clamping Diode (CBTS)

Z - Power-Up 3-State (LVCZ)

#### Bit Width

Examples: Blank = Gates, MSI, and Octals

1G - Single Gate

2G - Dual Gate

3G - Triple Gate

8 - Octal IEEE 1149.1 (JTAG)

16 - Widebus™ (16, 18, and 20 bit)

18 - Widebus IEEE 1149.1 (JTAG)

32 - Widebus+™ (32 and 36 bit)

#### 6 **Options**

Examples: Blank = No Options

2 - Series Damping Resistor on Outputs

4 - Level Shifter

25 – 25- $\Omega$  Line Driver

#### **Function**

Examples: 244 - Noninverting Buffer/Driver

374 - D-Type Flip-Flop

573 - D-Type Transparent Latch 640 - Inverting Transceiver

#### **Device Revision**

Blank = No Revision

Letter Designator A-Z

#### **Packages**

Commercial: D, DW - Small-Outline Integrated Circuit (SOIC)

DB, DL - Shrink Small-Outline Package (SSOP)

DBB, DGV - Thin Very Small-Outline Package (TVSOP)

DBQ - Quarter-Size Outline Package (QSOP)

DBV, DCK, NS, PS - Small-Outline Package (SOP) DCT, DGG, PW - Thin Shrink Small-Outline Package

(TSSOP)

DCU - Very Small-Outline Package (VSOP)

FN - Plastic Leaded Chip Carrier (PLCC)

GKE, GKF - MicroSTAR BGA™ Low-Profile Fine-Pitch

Ball Grid Array (LFBGA)

GQL - MicroStar Jr.™ Very-Thin-Profile Fine-Pitch

Ball Grid Array (VFBGA)

N, NP, NT - Plastic Dual-In-Line Package (PDIP)

PAG, PAH, PCA, PCB, PM, PN, PZ -

Thin Quad Flatpack (TQFP) PH, PQ, RC - Quad Flatpack (QFP)

YEA - NanoStar™ Die-Size Ball Grid Array (DSBGA)†

Military: FK - Leadless Ceramic Chip Carrier (LCCC)

GB – Ceramic Pin Grid Array (CPGA)

HFP, HS, HT, HV - Ceramic Quad Flatpack (CQFP)

J, JT - Ceramic Dual-In-Line Package (CDIP)

W, WA, WD - Ceramic Flatpack (CFP)

#### 10 Tape and Reel

Devices in the DB and PW package types include the R designation for reeled product. Existing product inventory designated LE may remain, but all products are being converted to the R designation.

Examples: Old Nomenclature - SN74LVTxxxDBLE

New Nomenclature - SN74LVTxxxADBR

LE - Left Embossed (valid for DB and PW packages only)

R – Standard (valid for all surface-mount packages)

There is no functional difference between LE and R designated products, with respect to the carrier tape, cover tape, or reels used.

† DSBGA is the JEDEC reference for wafer chip scale package (WCSP).



In digital-system design, consideration must be given to thermal management of components. The small size of the small-outline packages makes this even more critical. Figures 1–5 show the high-effect (High-K) thermal resistance for the small-outline 14-, 16-, 20-, 24-, and 48-pin packages for various rates of airflow calculated in accordance with JESD 51-7.

The thermal resistances in Figures 1–5 can be used to approximate typical and maximum virtual junction temperatures. In general, the junction temperature for any device can be calculated using the following equation:

$$T_J = R_{\theta JA} \times P_T + T_A$$

where:

 $T_{.1}$  = virtual junction temperature (°C)

 $R_{\theta JA}$  = thermal resistance, junction to free air (°C/W)

P<sub>T</sub> = total power dissipation of the device (W)

 $T_A$  = free-air temperature (°C)

#### JUNCTION-TO-AMBIENT THERMAL RESISTANCE

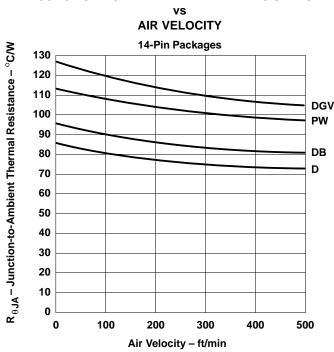
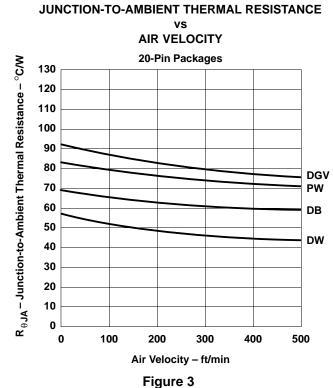
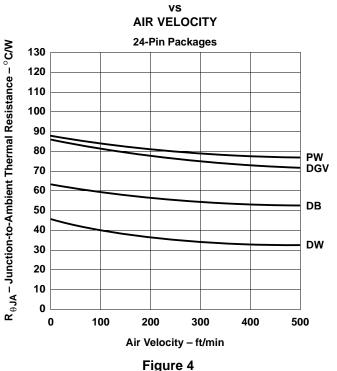


Figure 1

#### JUNCTION-TO-AMBIENT THERMAL RESISTANCE **AIR VELOCITY** 16-Pin Packages $R_{\theta\, JA}-$ Junction-to-Ambient Thermal Resistance – $^{\circ}\text{C/W}$ DGV PW DB D Air Velocity - ft/min Figure 2



#### JUNCTION-TO-AMBIENT THERMAL RESISTANCE



#### **AIR VELOCITY** 48-Pin Packages $R_{\theta JA}$ – Junction-to-Ambient Thermal Resistance – $^{\circ}$ C/W DGG DL DGV

Air Velocity - ft/min

Figure 5

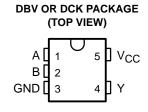
JUNCTION-TO-AMBIENT THERMAL RESISTANCE

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- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable



#### description

This single 2-input positive-NAND gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G00 performs the Boolean function  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

TA	PACKAGE	i†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G00DBVR	
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G00DCKR	

<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Y
Н	Н	L
L	Χ	Н
Х	L	Н

#### logic diagram (positive logic)



<sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or p (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

Supply voltage		0.0			
		0.8	2.7	V	
	V <sub>CC</sub> = 0.8 V	Vcc			
High-level input voltage	V <sub>CC</sub> = 1.1 V to 2.3 V	0.65 × V <sub>CC</sub>		V	
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7			
	V <sub>CC</sub> = 0.8 V		0		
/ <sub>IL</sub> Low-level input voltage / <sub>I</sub> Input voltage	V <sub>CC</sub> = 1.1 V to 2.3 V		0.35 × V <sub>CC</sub>	V	
	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		
Input voltage		0	2.7	V	
Output voltage		0	Vcc	V	
	V <sub>CC</sub> = 0.8 V		-0.7		
High-level output current	V <sub>CC</sub> = 1.1 V		-3		
	V <sub>CC</sub> = 1.4 V		<b>-</b> 5	mA	
	V <sub>CC</sub> = 1.65 V		-8		
	V <sub>CC</sub> = 2.3 V		-9		
	V <sub>CC</sub> = 0.8 V		0.7		
	V <sub>CC</sub> = 1.1 V		3		
Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA	
	V <sub>CC</sub> = 1.65 V		8		
	V <sub>CC</sub> = 2.3 V		9		
Input transition rise or fall rate			20	ns/V	
Operating free-air temperature	-40	85	°C		
	Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current  Input transition rise or fall rate  Operating free-air temperature	Low-level input voltage $ \begin{array}{c} V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 0.8 \ V \\ V_{CC} = 1.1 \ V \ to \ 2.3 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ \hline \end{array} $ Input voltage $ \begin{array}{c} V_{CC} = 0.8 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ \hline \end{array} $ High-level output current $ \begin{array}{c} V_{CC} = 0.8 \ V \\ V_{CC} = 1.1 \ V \\ \hline V_{CC} = 1.1 \ V \\ \hline V_{CC} = 1.65 \ V \\ \hline V_{CC} = 2.3 \ V \\ \hline V_{CC} = 0.8 \ V \\ \hline V_{CC} = 1.1 \ V \\ \hline \end{array} $ Low-level output current $ \begin{array}{c} V_{CC} = 1.4 \ V \\ \hline V_{CC} = 1.4 \ V \\ \hline V_{CC} = 1.1 \ V \\ \hline \hline V_{CC} = 1.65 \ V \\ \hline V_{CC} = 1.65 \ V \\ \hline \hline V_{CC} = 2.3 \ V \\ \hline \end{array} $ Input transition rise or fall rate $ \begin{array}{c} V_{CC} = 2.3 \ V \\ \hline \end{array} $ Operating free-air temperature	$\begin{array}{c c} V_{CC} = 2.3 \ V \ to \ 2.7 \ V & 1.7 \\ \hline V_{CC} = 0.8 \ V & \\ \hline V_{CC} = 1.1 \ V \ to \ 2.3 \ V & \\ \hline V_{CC} = 2.3 \ V \ to \ 2.7 \ V & \\ \hline \end{array}$ Low-level input voltage $\begin{array}{c c} 0 & \\ \hline O & \\$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT		
		I <sub>OH</sub> = -100 μA		0.8 V to 2.7 V	V <sub>CC</sub> -0.1					
	$I_{OH} = -0.7 \text{ mA}$	0.8 V		0.55						
Vou		$I_{OH} = -3 \text{ mA}$		1.1 V	V <sub>CC</sub> -0.3			V		
VOH		I <sub>OH</sub> = -5 mA		1.4 V	V <sub>CC</sub> -0.4			V		
		I <sub>OH</sub> = -8 mA		1.65 V	V <sub>CC</sub> -0.45					
		$I_{OH} = -9 \text{ mA}$		2.3 V	1.8			7		
		I <sub>OL</sub> = 100 μA		0.8 V to 2.7 V				).2		
		I <sub>OL</sub> = 0.7 mA	0.8 V		0.25					
\/		I <sub>OL</sub> = 3 mA		1.1 V			0.3	v		
VOL		I <sub>OL</sub> = 5 mA		1.4 V			0.4	V		
		I <sub>OL</sub> = 8 mA		1.65 V			0.45			
		I <sub>OL</sub> = 9 mA		2.3 V			0.6			
П	A or B input	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	μΑ		
l <sub>off</sub>		$V_I$ or $V_O = 2.7 V$		0			±10	μΑ		
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	·	0.8 V to 2.7 V			10	μΑ		
Ci		$V_I = V_{CC}$ or GND		2.5 V				pF		

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 2.5 V,  $T_A$  = 25°C.

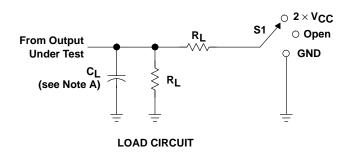
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER FROM TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT		
	(INFOI)	(INFO1) (OO1FO1)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
<sup>t</sup> pd	A or B	Y						ns

#### operating characteristics, $T_A = 25^{\circ}C$

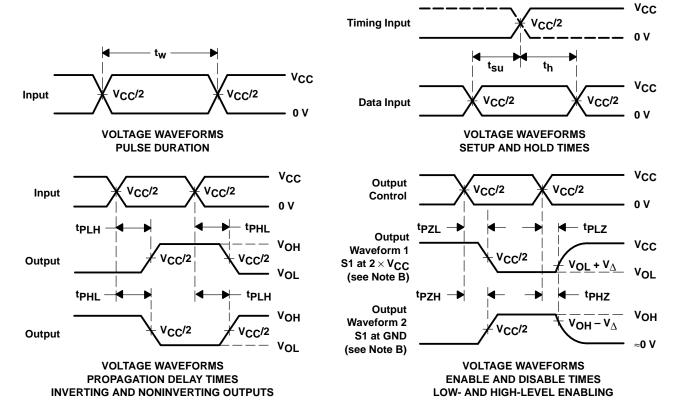
PARAMETER		PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V V <sub>CC</sub> = 2.5 V		UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

VCC	CL	RL	$v_{\scriptscriptstyle\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V ± 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable

# DBV OR DCK PACKAGE (TOP VIEW) A 1 5 VCC B 2 GND 3 4 Y

#### description

This single 2-input positive-NOR gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G02 performs the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

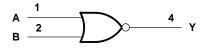
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G02DBVR	
-40 C to 85 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G02DCKR	

<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

	INP	JTS	OUTPUT
	Α	В	Υ
I	Н	Χ	L
I	Χ	Н	L
I	L	L	Н

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or p	ower-off state, V <sub>O</sub>
(see Note 1)	–0.5 V to 3.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sta</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

Supply voltage		0.0		
		0.8	2.7	V
	V <sub>CC</sub> = 0.8 V	Vcc		
High-level input voltage	V <sub>CC</sub> = 1.1 V to 2.3 V	0.65 × V <sub>CC</sub>		V
	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	V <sub>CC</sub> = 0.8 V		0	
Low-level input voltage	V <sub>CC</sub> = 1.1 V to 2.3 V		0.35 × V <sub>CC</sub>	V
	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
Input voltage		0	2.7	V
Output voltage		0	Vcc	V
	V <sub>CC</sub> = 0.8 V		-0.7	mA
High-level output current	V <sub>CC</sub> = 1.1 V		-3	
	V <sub>CC</sub> = 1.4 V		<b>-</b> 5	
	V <sub>CC</sub> = 1.65 V		-8	
	V <sub>CC</sub> = 2.3 V		-9	
	V <sub>CC</sub> = 0.8 V		0.7	
	V <sub>CC</sub> = 1.1 V		3	
Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
	V <sub>CC</sub> = 1.65 V		8	
	V <sub>CC</sub> = 2.3 V		9	
Input transition rise or fall rate	•		20	ns/V
Operating free-air temperature			85	°C
	Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current  Input transition rise or fall rate  Operating free-air temperature	Low-level input voltage $ \begin{array}{c} V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ V_{CC} = 0.8 \ V \\ V_{CC} = 1.1 \ V \ to \ 2.3 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ \hline \end{array} $ Input voltage $ \begin{array}{c} V_{CC} = 0.8 \ V \\ V_{CC} = 2.3 \ V \ to \ 2.7 \ V \\ \hline \end{array} $ High-level output current $ \begin{array}{c} V_{CC} = 0.8 \ V \\ V_{CC} = 1.1 \ V \\ \hline V_{CC} = 1.1 \ V \\ \hline V_{CC} = 1.65 \ V \\ \hline V_{CC} = 2.3 \ V \\ \hline V_{CC} = 0.8 \ V \\ \hline V_{CC} = 1.1 \ V \\ \hline \end{array} $ Low-level output current $ \begin{array}{c} V_{CC} = 1.4 \ V \\ \hline V_{CC} = 1.4 \ V \\ \hline V_{CC} = 1.1 \ V \\ \hline \hline V_{CC} = 1.65 \ V \\ \hline V_{CC} = 1.65 \ V \\ \hline \hline V_{CC} = 2.3 \ V \\ \hline \end{array} $ Input transition rise or fall rate $ \begin{array}{c} V_{CC} = 2.3 \ V \\ \hline \end{array} $ Operating free-air temperature	$\begin{array}{c c} V_{CC} = 2.3 \ V \ to \ 2.7 \ V & 1.7 \\ \hline V_{CC} = 0.8 \ V & \\ \hline V_{CC} = 1.1 \ V \ to \ 2.3 \ V & \\ \hline V_{CC} = 2.3 \ V \ to \ 2.7 \ V & \\ \hline \end{array}$ Low-level input voltage $\begin{array}{c c} 0 & \\ \hline O & \\$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# PRODUCT PREVIEW

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	V <sub>CC</sub> -0.1				
		I <sub>OH</sub> = -0.7 mA	0.8 V		0.55			
Vou		I <sub>OH</sub> = -3 mA	1.1 V	V <sub>CC</sub> -0.3			V	
VOH		I <sub>OH</sub> = -5 mA	1.4 V	V <sub>CC</sub> -0.4			V	
		I <sub>OH</sub> = -8 mA	1.65 V	V <sub>CC</sub> -0.45				
		I <sub>OH</sub> = -9 mA	2.3 V	1.8				
		I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2	0.2	
		$I_{OL} = 0.7 \text{ mA}$	0.8 V		0.25			
\/		$I_{OL} = 3 \text{ mA}$	1.1 V			0.3	V	
VOL		$I_{OL} = 5 \text{ mA}$	1.4 V			0.4	V	
		I <sub>OL</sub> = 8 mA	1.65 V			0.45		
		$I_{OL} = 9 \text{ mA}$	2.3 V			0.6		
lį	A or B input	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μΑ	
l <sub>off</sub>		$V_I$ or $V_O = 2.7 V$	0			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ	
C <sub>i</sub>		$V_I = V_{CC}$ or GND	2.5 V				pF	

 $<sup>\</sup>overline{\dagger}$  All typical values are at  $V_{CC} = 2.5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

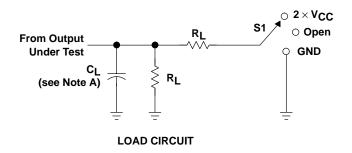
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER FROM (INPUT)		V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT	
	(INFO1)	(001701)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
<sup>t</sup> pd	A or B	Y						ns

#### operating characteristics, $T_A = 25^{\circ}C$

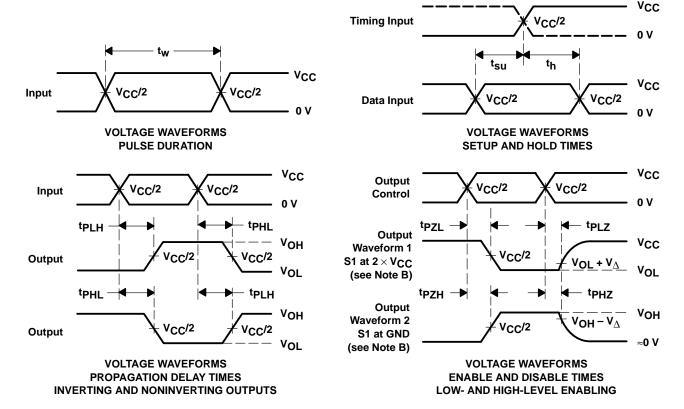
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V V <sub>CC</sub> = 2		UNIT	
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF	

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

Vcc	CL	RL	$v_{\scriptscriptstyle\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V ± 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



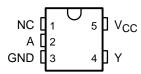
- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable

### DBV OR DCK PACKAGE (TOP VIEW)



#### NC - No internal connection

#### description

This single inverter gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G04 performs the Boolean function  $Y = \overline{A}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

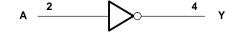
TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G04DBVR	
-40 C to 85 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G04DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)





<sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or p	ower-off state, V <sub>O</sub>
(see Note 1)	–0.5 V to 3.6 V
Output voltage range, VO (see Notes 1 and 2)	0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sta</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		0.8	2.7	V	
		V <sub>CC</sub> = 0.8 V	Vcc			
$V_{IH}$	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$	0.65 × V <sub>CC</sub>		V	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7			
		V <sub>CC</sub> = 0.8 V		0		
VIL	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$		$0.35 \times V_{CC}$	V	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7		
٧ı	Input voltage	•	0	2.7	V	
٧o	Output voltage		0	Vcc	V	
	IOH High-level output current		V <sub>CC</sub> = 0.8 V		-0.7	
		V <sub>CC</sub> = 1.1 V		-3		
lOH		V <sub>CC</sub> = 1.4 V		<b>-</b> 5	mA	
		V <sub>CC</sub> = 1.65 V		-8		
		V <sub>CC</sub> = 2.3 V		-9		
		V <sub>CC</sub> = 0.8 V		0.7		
		V <sub>CC</sub> = 1.1 V		3		
loL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA	
		V <sub>CC</sub> = 1.65 V		8		
		V <sub>CC</sub> = 2.3 V		9		
Δt/Δν	Input transition rise or fall rate	•		20	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITION	ONS	Vcc	MIN	TYP	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	$A\mu = -100  \mu$ A 0.0 = HC		V <sub>CC</sub> -0.1				
		$I_{OH} = -0.7 \text{ mA}$		0.8 V		0.55			
1		I <sub>OH</sub> = -3 mA		1.1 V	V <sub>CC</sub> -0.3			V	
VOH		I <sub>OH</sub> = -5 mA		1.4 V	V <sub>CC</sub> -0.4			V	
		I <sub>OH</sub> = -8 mA		1.65 V	V <sub>CC</sub> -0.45				
		I <sub>OH</sub> = -9 mA		2.3 V	1.8				
		I <sub>OL</sub> = 100 μA		0.8 V to 2.7 V			0.2		
		I <sub>OL</sub> = 0.7 mA		0.8 V		0.25			
1		I <sub>OL</sub> = 3 mA		1.1 V			0.3	<b>→</b> ∨ I	
VOL		I <sub>OL</sub> = 5 mA		1.4 V			0.4		
		I <sub>OL</sub> = 8 mA		1.65 V			0.45		
		I <sub>OL</sub> = 9 mA		2.3 V			0.6		
lį	A input	V <sub>I</sub> = V <sub>CC</sub> or GND		0 to 2.7 V			±5	μΑ	
l <sub>off</sub>	•	$V_I$ or $V_O = 2.7 V$		0			±10	μΑ	
Icc	•	$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	0.8 V to 2.7 V			10	μΑ	
Ci		$V_I = V_{CC}$ or GND		2.5 V				pF	

 $<sup>\</sup>overline{\dagger}$  All typical values are at  $V_{CC} = 2.5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

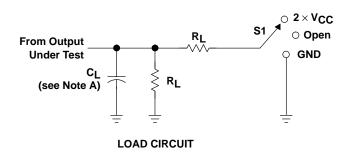
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
	(INFO1)	(001701)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
t <sub>pd</sub>	А	Y						ns

#### operating characteristics, $T_A = 25^{\circ}C$

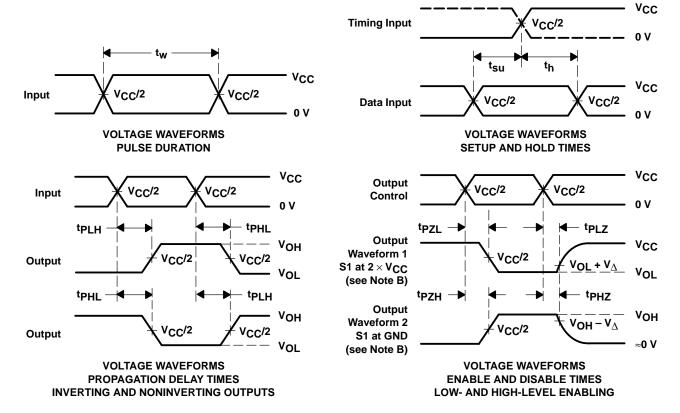
PARAMETER		PARAMETER TEST CONDITIONS VCC =		V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
	PARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

VCC	CL	RL	$oldsymbol{V}_\Delta$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



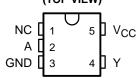
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable
- Unbuffered Output

#### description

This single inverter gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1GU04 contains one inverter with an unbuffered output and performs the Boolean function  $Y = \overline{A}$ .

### DBV OR DCK PACKAGE (TOP VIEW)



NC - No internal connection

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1GU04DBVR	
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1GU04DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)





<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT			
VCC	Supply voltage	0.8	2.7	V				
$V_{IH}$	High-level input voltage	$I_{O} = -100 \mu\text{A}$	$0.75 \times V_{CC}$		V			
$\vee_{IL}$	Low-level input voltage	$I_{O} = 100  \mu A$		$0.25 \times V_{CC}$	V			
٧ <sub>I</sub>	Input voltage	nput voltage						
۷o	Output voltage		0	VCC	V			
ЮН		V <sub>CC</sub> = 0.8 V		-0.7				
		V <sub>CC</sub> = 1.1 V		-3				
	High-level output current	V <sub>CC</sub> = 1.4 V		<b>-</b> 5	mA			
		V <sub>CC</sub> = 1.65 V		-8				
		V <sub>CC</sub> = 2.3 V		-9				
l <sub>OL</sub>		V <sub>CC</sub> = 0.8 V		0.7				
		V <sub>CC</sub> = 1.1 V		3				
	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA			
		V <sub>CC</sub> = 1.65 V		8				
		V <sub>CC</sub> = 2.3 V		9				
Δt/Δν	Input transition rise or fall rate			ns/V				
TA	Operating free-air temperature	-40	85	°C				
JOTE 4	A All was disaster of the desire worth a held of V and OND to accompany desire as one fire. Defeate the Theory is a contract to the contract t							

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v <sub>CC</sub>	MIN	TYP†	MAX	UNIT		
	$I_{OH} = -100 \mu\text{A}$	0.8 V to 2.7 V	V <sub>CC</sub> -0.1					
	$I_{OH} = -0.7 \text{ mA}$	0.8 V		0.55				
V	$I_{OH} = -3 \text{ mA}$	1.1 V	V <sub>CC</sub> -0.3			V		
VOH	$I_{OH} = -5 \text{ mA}$	1.4 V	V <sub>CC</sub> -0.4			V		
	$I_{OH} = -8 \text{ mA}$	1.65 V	V <sub>CC</sub> -0.45					
	$I_{OH} = -9 \text{ mA}$	2.3 V	1.8					
	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2	).2		
	I <sub>OL</sub> = 0.7 mA	0.8 V		0.25				
V	I <sub>OL</sub> = 3 mA	1.1 V			0.3	V		
V <sub>OL</sub>	I <sub>OL</sub> = 5 mA			0.4	V			
	I <sub>OL</sub> = 8 mA	1.65 V			0.45			
	I <sub>OL</sub> = 9 mA	2.3 V			0.6			
I <sub>I</sub> A input	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μΑ		
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ		
C <sub>i</sub>	$V_I = V_{CC}$ or GND	2.5 V				pF		

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 2.5 V,  $T_A$  = 25°C.

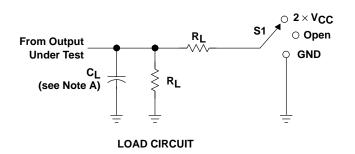
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 0.8 \text{ V}$ $V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$		V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
			TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
t <sub>pd</sub>	Α	Υ						ns

#### operating characteristics, T<sub>A</sub> = 25°C

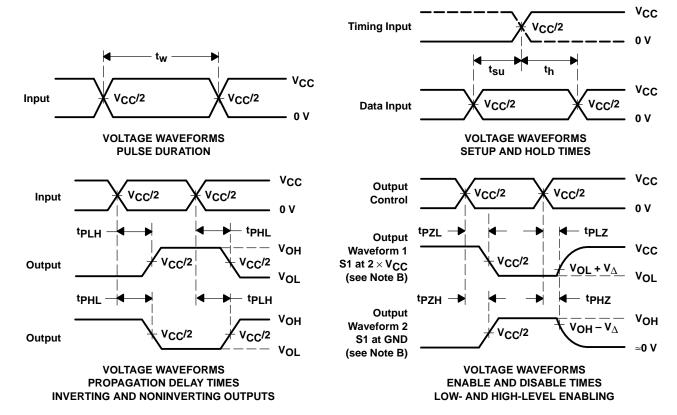
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

VCC	CL	RL	$oldsymbol{V}_\Delta$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V
	1	1	I



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzI and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



## SN74AUC1G06 SINGLE INVERTER BUFFER/DRIVER WITH OPFN-DRAIN OUTPUT

SCES372A - SEPTEMBER 2001 - REVISED OCTOBER 2001

- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable

# NC 1 5 V<sub>CC</sub>

### NC - No internal connection

## description

This single inverter buffer/driver is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The output of the SN74AUC1G06 is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G06DBVR	
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G06DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

## logic diagram (positive logic)





<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, I <sub>O</sub>	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		0.8	2.7	V
		V <sub>CC</sub> = 0.8 V	Vcc		
VIH	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$	0.65 × V <sub>CC</sub>		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
		V <sub>CC</sub> = 0.8 V		0	
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$		0.35 × V <sub>CC</sub>	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
٧ <sub>I</sub>	Input voltage		0	2.7	V
٧o	Output voltage		0	2.7	V
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
lOL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
		V <sub>CC</sub> = 1.65 V		8	
	V <sub>CC</sub> = 2.3 V			9	
Δt/Δν	Input transition rise or fall rate	•		20	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITION	vcc	MIN	TYP	MAX	UNIT	
		I <sub>OL</sub> = 100 μA		0.8 V to 2.7 V			0.2	
1		$I_{OL} = 0.7 \text{ mA}$		0.8 V		0.25		
\ \/a:	V <sub>OL</sub>	I <sub>OL</sub> = 3 mA		1.1 V			0.3	V
VOL		I <sub>OL</sub> = 5 mA		1.4 V			0.4	V
		I <sub>OL</sub> = 8 mA		1.65 V			0.45	
		I <sub>OL</sub> = 9 mA		2.3 V			0.6	
lį	A input	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	μΑ
loff		$V_I$ or $V_O = 2.7 V$		0			±10	μΑ
Icc		$V_I = V_{CC}$ or GND,	I <sub>O</sub> = 0	0.8 V to 2.7 V			10	μΑ
Ci		$V_I = V_{CC}$ or GND		2.5 V				pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 2.5 V, T<sub>A</sub> = 25°C.

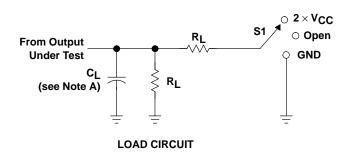
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
	(1141 01)	(0011 01)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
t <sub>pd</sub>	А	Y						ns

## operating characteristics, $T_A = 25^{\circ}C$

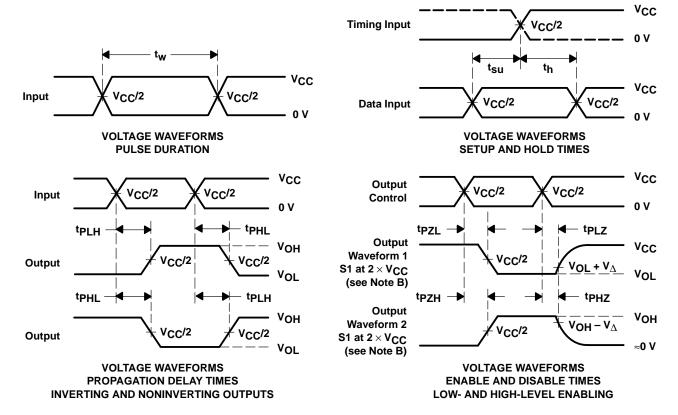
	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
	FARAINETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	S1
<sup>t</sup> PZL (see Note F)	2×V <sub>CC</sub>
<sup>t</sup> PLZ (see Note G)	2×V <sub>CC</sub>
tPHZ/tPZH	2×V <sub>CC</sub>

VCC	CL	RL	$v_{\scriptscriptstyle\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V ± 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. For open-drain outputs, tpLz and tpzL are the same as tpd.
  - F. tpzL is measured at V<sub>CC</sub>/2.
  - G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable

# NC 1 5 V<sub>CC</sub>

NC - No internal connection

## description

This single buffer/driver is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The output of the SN74AUC1G07 is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G07DBVR	
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G07DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	Н
L	L

## logic diagram (positive logic)



<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, I <sub>O</sub>	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		0.8	2.7	V
	High-level input voltage	V <sub>CC</sub> = 0.8 V	Vcc		
VIH		$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$	0.65 × V <sub>CC</sub>		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	Low-level input voltage	V <sub>CC</sub> = 0.8 V		0	
$\vee_{IL}$		$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$		0.35 × V <sub>CC</sub>	٧
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
٧ <sub>I</sub>	Input voltage		0	2.7	V
٧o	Output voltage		0	2.7	V
		V <sub>CC</sub> = 0.8 V		0.7	
	Low-level output current	V <sub>CC</sub> = 1.1 V		3	mA
lOL		V <sub>CC</sub> = 1.4 V		5	
		V <sub>CC</sub> = 1.65 V		8	
		V <sub>CC</sub> = 2.3 V		9	
Δt/Δν	Input transition rise or fall rate	•		20	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	v <sub>CC</sub>	MIN TYP <sup>†</sup> MAX	UNIT
	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V	0.2	
	$I_{OL} = 0.7 \text{ mA}$	0.8 V	0.25	
Va.	$I_{OL} = 3 \text{ mA}$	1.1 V	0.3	V
VOL	I <sub>OL</sub> = 5 mA	1.4 V	0.4	V
	$I_{OL} = 8 \text{ mA}$	1.65 V	0.45	
	$I_{OL} = 9 \text{ mA}$	2.3 V	0.6	
I <sub>I</sub> A input	$V_I = V_{CC}$ or GND	0 to 2.7 V	±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 2.7 V$	0	±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V	10	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	2.5 V		pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 2.5 V, T<sub>A</sub> = 25°C.

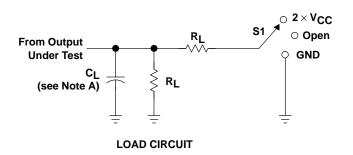
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)			V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
			TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX		
<sup>t</sup> pd	А	Y						ns	

## operating characteristics, $T_A = 25^{\circ}C$

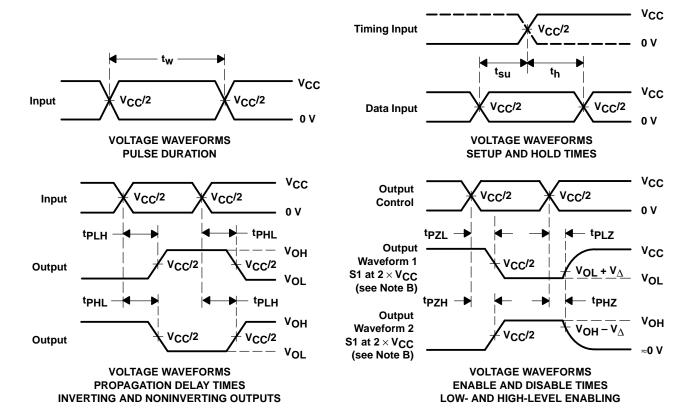
	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	S1
tPZL	2×V <sub>CC</sub>
(see Note F)	
t <sub>PLZ</sub>	2×V <sub>CC</sub>
(see Note G)	
tPHZ/tPZH	2×V <sub>CC</sub>

V <sub>CC</sub>	CL	RL	${f v}_{\!\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



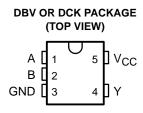
NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. For open-drain outputs, tpLZ and tpZL are the same as tpd.
- F. tpzi is measured at V<sub>CC</sub>/2.
- G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Lambda}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable



## description

This single 2-input positive-AND gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G08 performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G08DBVR	
-40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AUC1G08DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	Н
L	X	L
Х	L	L

## logic diagram (positive logic)





<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Voltage range applied to any output in the high-impedance or power-off sta	
(see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, IO	
Continuous current through V <sub>CC</sub> or GND	
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		0.8	2.7	V
		V <sub>CC</sub> = 0.8 V	Vcc		
$\vee_{IH}$	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$	0.65 × V <sub>CC</sub>		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
	Low-level input voltage	V <sub>CC</sub> = 0.8 V		0	
VIL		$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$		$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	
٧ı	Input voltage	•	0	2.7	V
٧o	Output voltage		0	Vcс	V
	High-level output current	V <sub>CC</sub> = 0.8 V		-0.7	mA
		V <sub>CC</sub> = 1.1 V		-3	
lOH		V <sub>CC</sub> = 1.4 V		<b>-</b> 5	
		V <sub>CC</sub> = 1.65 V		-8	
		V <sub>CC</sub> = 2.3 V		-9	
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
loL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
		V <sub>CC</sub> = 1.65 V		8	
		V <sub>CC</sub> = 2.3 V		9	
Δt/Δν	Input transition rise or fall rate	•		20	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT
		I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	V <sub>CC</sub> -0.1			
		I <sub>OH</sub> = -0.7 mA	0.8 V		0.55		
Vou		I <sub>OH</sub> = -3 mA	1.1 V	V <sub>CC</sub> -0.3			V
VOH	I <sub>OH</sub> = -5 mA	1.4 V	V <sub>CC</sub> -0.4			V	
	I <sub>OH</sub> = -8 mA	1.65 V	V <sub>CC</sub> -0.45				
		I <sub>OH</sub> = -9 mA	2.3 V	1.8			
		I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2	
		$I_{OL} = 0.7 \text{ mA}$	0.8 V		0.25		
\/		$I_{OL} = 3 \text{ mA}$	1.1 V			0.3	V
VOL		$I_{OL} = 5 \text{ mA}$	1.4 V			0.4	V
		I <sub>OL</sub> = 8 mA	1.65 V			0.45	
		I <sub>OL</sub> = 9 mA	2.3 V			0.6	
Ιį	A or B input	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μΑ
l <sub>off</sub>		$V_I$ or $V_O = 2.7 V$	0			±10	μΑ
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ
C <sub>i</sub>		$V_I = V_{CC}$ or GND	2.5 V				pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 2.5 V,  $T_A$  = 25°C.

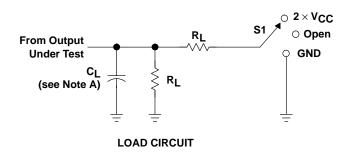
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
	(INFOT)	(114701) (001701)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
t <sub>pd</sub>	A or B	Y						ns

## operating characteristics, $T_A = 25^{\circ}C$

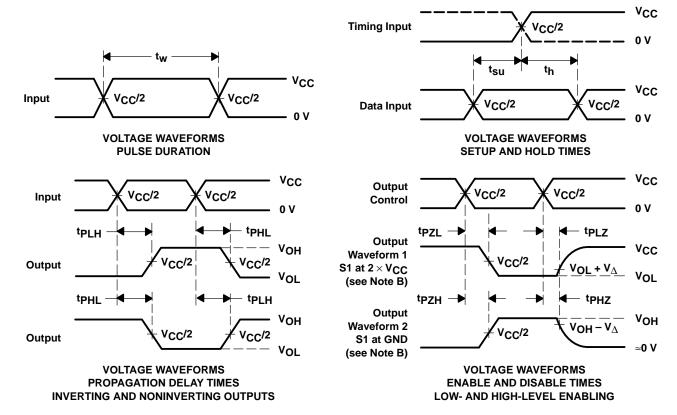
	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	$V_{CC} = 1.8 V$	V <sub>CC</sub> = 2.5 V	UNIT
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

VCC	CL	RL	$v_{\scriptscriptstyle\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	<b>500</b> Ω	0.15 V



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzI and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable

# NC 1 5 V<sub>CC</sub> GND 3 4 Y

NC - No internal connection

## description

This single Schmitt-trigger inverter is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G14 contains one inverter and performs the Boolean function  $Y = \overline{A}$ . The device functions as an independent inverter but, because of Schmitt action, it may have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

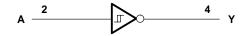
TA	PACKAG	E†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G14DBVR	
-40 C t0 65 C	SOP (SC-70) – DCK	Tape and reel	SN74AUC1G14DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

## logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 3.6 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or	power-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		0.8	2.7	V
٧ı	Input voltage		0	2.7	V
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 0.8 V		-0.7	
		V <sub>CC</sub> = 1.1 V		-3	
ЮН	High-level output current	V <sub>CC</sub> = 1.4 V		<b>–</b> 5	mA
J.1		V <sub>CC</sub> = 1.65 V		-8	
		V <sub>CC</sub> = 2.3 V		2.7 VCC -0.7 -3 -5 -8 -9 0.7 3 5 8 9	
		V <sub>CC</sub> = 0.8 V		0.7	
		V <sub>CC</sub> = 1.1 V		3	
loL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
		V <sub>CC</sub> = 1.65 V		8	
		V <sub>CC</sub> = 2.3 V		2.7 VCC -0.7 -3 -5 -8 -9 0.7 3 5 8	
Δt/Δν	Input transition rise or fall rate				ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP† MAX	UNIT
		0.8 V		0.5	
V <sub>T+</sub>		1.1 V	0.51	0.86	
Positive-going input threshold voltage		1.4 V	0.65	1	V
tilleshold voltage		1.65 V	0.79	1.16	
		2.3 V	1.11	1.56	
		0.8 V		0.3	
V <sub>T</sub> _		1.1 V	0.22	0.53	]
Negative-going input		1.4 V	0.3	0.58	V
threshold voltage		1.65 V	0.39	0.62	
		2.3 V	0.58	0.87	
		0.8 V		0.21	
$\Delta V_{T}$		1.1 V	0.25	0.38	
Hysteresis		1.4 V	0.31	0.5	V
$(V_{T+} - V_{T-})$		1.65 V	0.37	0.62	
		2.3 V	0.48	0.77	
	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V		0.2	
	$I_{OL} = 0.7 \text{ mA}$	0.8 V		0.25	
Va	$I_{OL} = 3 \text{ mA}$	1.1 V		0.3	V
VOL	$I_{OL} = 5 \text{ mA}$	1.4 V		0.4	]
	$I_{OL} = 8 \text{ mA}$	1.65 V		0.45	
	$I_{OL} = 9 \text{ mA}$	2.3 V		0.6	
I <sub>I</sub> A input	$V_I = V_{CC}$ or GND	0 to 2.7 V		±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 2.7 V$	0		±10	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V		10	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	2.5 V			pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 2.5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

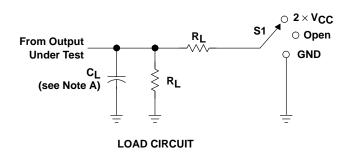
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
	(1141 01)	(0011 01)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
<sup>t</sup> pd	А	Y						ns

## operating characteristics, T<sub>A</sub> = 25°C

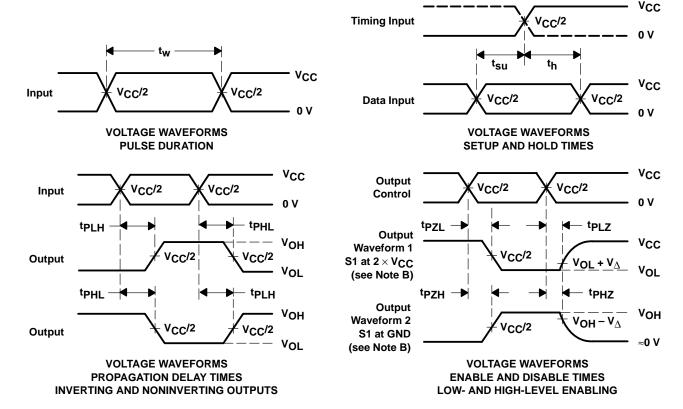
Ī		PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
		FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
I	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

Vcc	CL	RL	$v_{\scriptscriptstyle\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V ± 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V ± 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_0 = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tplH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable

# NC 1 5 V<sub>CC</sub> A 2 GND 3 4 Y

## description

NC - No internal connection

This single Schmitt-trigger buffer is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G17 contains one buffer and performs the Boolean function Y = A. The device functions as an independent buffer but, because of Schmitt action, it may have different input threshold levels for positive-going  $(V_{T+})$  and negative-going  $(V_{T-})$  signals.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

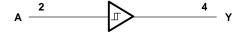
TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G17DBVR	
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G17DCKR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	Н
L	L

## logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or po	
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, I <sub>O</sub>	
Continuous current through V <sub>CC</sub> or GND	
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
VCC	Supply voltage		0.8	2.7	V
VI	V <sub>I</sub> Input voltage			2.7	V
٧o	Output voltage		0	VCC	V
		$V_{CC} = 0.8 \text{ V}$		-0.7	
		V <sub>CC</sub> = 1.1 V		-3	
IOH High-level output cur	High-level output current	V <sub>CC</sub> = 1.4 V		<b>–</b> 5	mA
	$V_{CC} = 1.65 \text{ V}$	V <sub>CC</sub> = 1.65 V		-8	
		V <sub>CC</sub> = 2.3 V		-9	
		$V_{CC} = 0.8 \text{ V}$		0.7	
		V <sub>CC</sub> = 1.1 V		3	
loL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA
	V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> = 1.65 V		8	
	V <sub>CC</sub> = 2.3 V			9	
Δt/Δv	Input transition rise or fall rate				ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	ν <sub>CC</sub>	MIN	TYP <sup>†</sup>	MAX	UNIT
		0.8 V		0.5		
V <sub>T+</sub>		1.1 V	0.51		0.86	
Positive-going input threshold voltage		1.4 V	0.65		1	V
tilicariola voltage		1.65 V	0.79		1.16	
		2.3 V	1.11		1.56	
		0.8 V		0.3		
V <sub>T</sub> _		1.1 V	0.22		0.53	
Negative-going input		1.4 V	0.3		0.58	V
threshold voltage		1.65 V	0.39		0.62	
		2.3 V	0.58		0.87	
		0.8 V		0.21		
ΔVT		1.1 V	0.25		0.38	
Hysteresis		1.4 V	0.31		0.5	V
$(V_{T+} - V_{T-})$		1.65 V	0.37		0.62	
		2.3 V	0.48		0.77	
	I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2	
	$I_{OL} = 0.7 \text{ mA}$	0.8 V		0.25		
Vo.	I <sub>OL</sub> = 3 mA	1.1 V			0.3	V
VOL	I <sub>OL</sub> = 5 mA	1.4 V			0.4	V
	I <sub>OL</sub> = 8 mA	1.65 V			0.45	
	I <sub>OL</sub> = 9 mA	2.3 V			0.6	
I <sub>I</sub> A input	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 2.7 V$	0			±10	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	2.5 V				pF

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

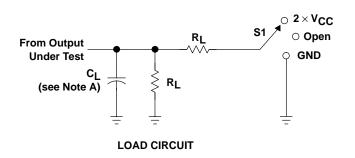
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT
	(IIVFOI)	(001701)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
t <sub>pd</sub>	Α	Υ						ns

## operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

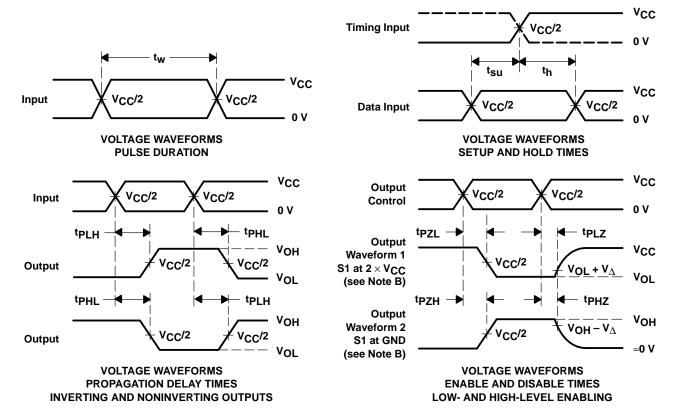
<sup>†</sup> All typical values are at  $V_{CC}$  = 2.5 V,  $T_A$  = 25°C. ‡ All values at  $V_{CC}$  = 0.8 V are tested at  $T_A$  = 25°C.

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

VCC	CL	RL	${f v}_{\Delta}$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V

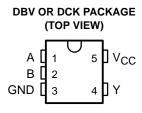


- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzI and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Optimized for 1.8-V Operation and Is 3.3-V Tolerant
- Sub 1-V Operable



## description

This single 2-input positive-OR gate is operational at 0.8-V to 2.7-V  $V_{CC}$ , but is designed specifically for 1.65-V to 1.95-V  $V_{CC}$  operation.

The SN74AUC1G32 performs the Boolean function Y = A + B or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

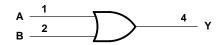
TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AUC1G32DBVR	
-40 C 10 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AUC1G32DCKR	

<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INPU	JTS	OUTPUT
Α	В	Υ
Н	Х	Н
Х	Н	Н
L	L	L

## logic diagram (positive logic)



<sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or p	ower-off state, V <sub>O</sub>
(see Note 1)	–0.5 V to 3.6 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±20 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sta</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. This value is limited to 3.6 V maximum.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vcc	Supply voltage		0.8	2.7	V	
		V <sub>CC</sub> = 0.8 V	Vcc			
$V_{IH}$	High-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$	0.65 × V <sub>C</sub> C		V	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7			
		V <sub>CC</sub> = 0.8 V		0		
VIL	Low-level input voltage	$V_{CC} = 1.1 \text{ V to } 2.3 \text{ V}$		$0.35 \times V_{CC}$	V	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7		
٧ı	Input voltage		0	2.7	V	
٧o	Output voltage		0	Vcc	V	
	High-level output current	V <sub>CC</sub> = 0.8 V		-0.7	mA	
		V <sub>CC</sub> = 1.1 V		-3		
ЮН		V <sub>CC</sub> = 1.4 V		-5		
		V <sub>CC</sub> = 1.65 V		-8		
		V <sub>CC</sub> = 2.3 V		-9		
		V <sub>CC</sub> = 0.8 V		0.7		
		V <sub>CC</sub> = 1.1 V		3		
lOL	Low-level output current	V <sub>CC</sub> = 1.4 V		5	mA	
		V <sub>CC</sub> = 1.65 V		8		
		V <sub>CC</sub> = 2.3 V		9		
Δt/Δν	Input transition rise or fall rate			20	ns/V	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	AMETER	TEST CONDITIONS	Vcc	MIN	TYP	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	0.8 V to 2.7 V	V <sub>CC</sub> -0.1				
		I <sub>OH</sub> = -0.7 mA	0.8 V		0.55			
Vou		I <sub>OH</sub> = -3 mA	1.1 V	V <sub>CC</sub> -0.3			V	
VOH		I <sub>OH</sub> = -5 mA	1.4 V	V <sub>CC</sub> -0.4			V	
		I <sub>OH</sub> = -8 mA	1.65 V	V <sub>CC</sub> -0.45				
		I <sub>OH</sub> = -9 mA	2.3 V	1.8				
		I <sub>OL</sub> = 100 μA	0.8 V to 2.7 V			0.2		
		$I_{OL} = 0.7 \text{ mA}$	0.8 V		0.25			
\/		$I_{OL} = 3 \text{ mA}$	1.1 V			0.3	V	
VOL		$I_{OL} = 5 \text{ mA}$	1.4 V			0.4	V	
		I <sub>OL</sub> = 8 mA	1.65 V			0.45		
		I <sub>OL</sub> = 9 mA	2.3 V			0.6		
Ιį	A or B input	$V_I = V_{CC}$ or GND	0 to 2.7 V			±5	μΑ	
l <sub>off</sub>		$V_I$ or $V_O = 2.7 V$	0			±10	μΑ	
Icc		$V_I = V_{CC}$ or GND, $I_O = 0$	0.8 V to 2.7 V			10	μΑ	
C <sub>i</sub>		$V_I = V_{CC}$ or GND	2.5 V				pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 2.5 V,  $T_A$  = 25°C.

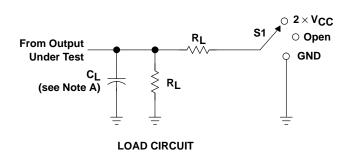
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER (INPUT) (OUTPUT)	V <sub>CC</sub> = 0.8 V	V <sub>CC</sub> = 1.2 V ± 0.1 V	V <sub>CC</sub> = 1.5 V ± 0.1 V	V <sub>CC</sub> = 1.8 V ± 0.15 V	V <sub>CC</sub> = 2.5 V ± 0.2 V	UNIT	
	(INFO1)	(001701)	TYP	MIN MAX	MIN MAX	MIN TYP MAX	MIN MAX	
t <sub>pd</sub>	A or B	Y						ns

## operating characteristics, $T_A = 25^{\circ}C$

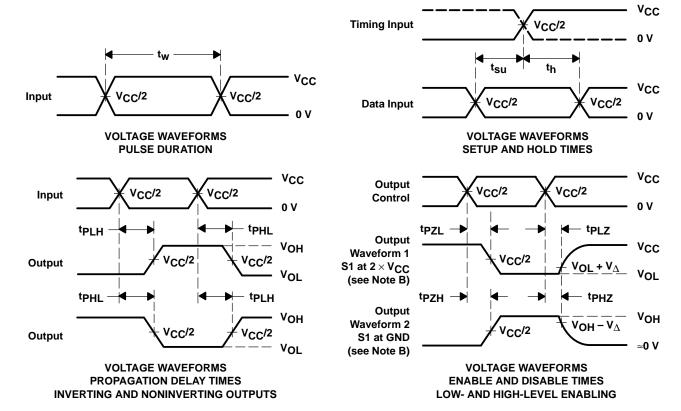
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub> = 1.5 V	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

VCC	CL	RL	$oldsymbol{V}_\Delta$
0.8 V	15 pF	<b>2 k</b> Ω	0.1 V
1.2 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	<b>2 k</b> Ω	0.1 V
1.8 V $\pm$ 0.15 V	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	30 pF	500 Ω	0.15 V
	1	1	I



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ , slew rate  $\geq$  1 V/ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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- Available in Texas Instruments' NanoStar™ **Package**
- Supports 5-V V<sub>CC</sub> Operation
- Ioff Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## **DBV OR DCK PACKAGE** (TOP VIEW) Ū ∨<sub>CC</sub> вſ GND [ YEA PACKAGE (BOTTOM VIEW) GND 03 40 01 50

## description

This single 2-input positive-NAND gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G00 performs the Boolean function  $Y = \overline{A} \cdot \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
4000 +- 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G00YEAR	CA
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G00DBVR	C00_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G00DCKR	CA_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Y
Н	Н	L
L	Χ	Н
Х	L	Н

## logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

<sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of  $V_{\hbox{CC}}$  is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cupply valtage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
\ <i>/</i>	High level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		v
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
\/	Low level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
VIL	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	V
۷o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
loh	High-level output current	V <sub>CC</sub> = 3 V		-16	mA
		VCC = 3 V		-24	
Vo ГОН		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
TA	Operating free-air temperature	•	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT	
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
Vон		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8				
		$I_{OL} = 100 \mu\text{A}$	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
1/		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V	
VOL		$I_{OL}$ = 16 mA	2.1/			0.4	V	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
II	A or B inputs	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>		$V_I$ or $V_O = 5.5 V$	0			±10	μΑ	
ICC		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
∆lcc		One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V			500	μΑ	
Ci		$V_I = V_{CC}$ or GND	3.3 V		4		pF	

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

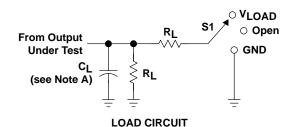
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		ν <sub>CC</sub> :		UNIT
	(INFOT)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Υ	3.1	8	1.3	5.5	1	4.7	1	4	ns

## operating characteristics, T<sub>A</sub> = 25°C

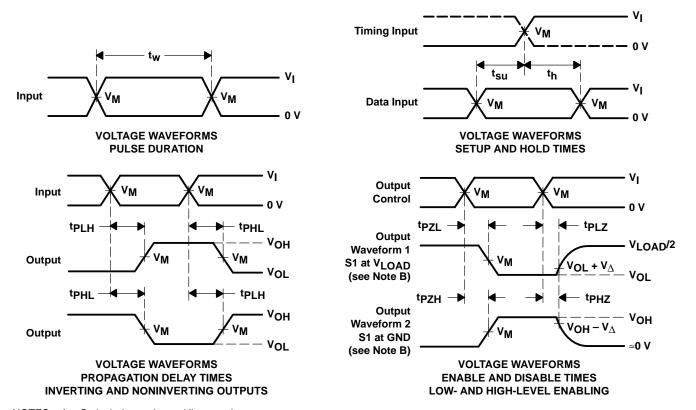
ſ	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	VCC = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		PARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII	
I	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	22	22	23	25	pF	

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INPUTS			V	C. B.		, I
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



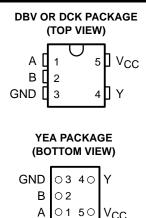
NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™ **Package**
- Supports 5-V V<sub>CC</sub> Operation
- Ioff Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



## description

This single 2-input positive-NOR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G02 performs the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

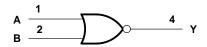
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 1- 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G02YEAR	CB
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G02DBVR	C02_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G02DCKR	CB_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Υ
Н	Х	L
Х	Н	L
L	L	Н

## logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

<sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of  $V_{\hbox{CC}}$  is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/	Cupply valtage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
\/	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
٧IH	r light-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		v
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
١/	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
۷IL	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	٧
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
IOH	High-level output current	V <sub>CC</sub> = 3 V		-16	mA
		VCC = 3 V		-24	
V <sub>IL</sub> V <sub>I</sub> V <sub>O</sub> IOH  LOL		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 3 V		16	mA
		vCC = 3 v		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
\/ - ·		$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	.,,
VOL		$I_{OL} = 16 \text{ mA}$	3 V			0.4	V
		I <sub>OL</sub> = 24 mA				0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
ΙĮ	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
l <sub>off</sub>		$V_I$ or $V_O = 5.5 V$	0			±10	μΑ
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
∆lCC		One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V			500	μΑ
Ci		$V_I = V_{CC}$ or GND	3.3 V		4	·	pF

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

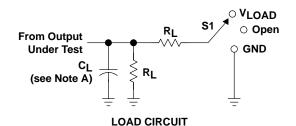
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Υ	2.8	8	1.2	5.5	1	4.5	1	4	ns

## operating characteristics, $T_A = 25^{\circ}C$

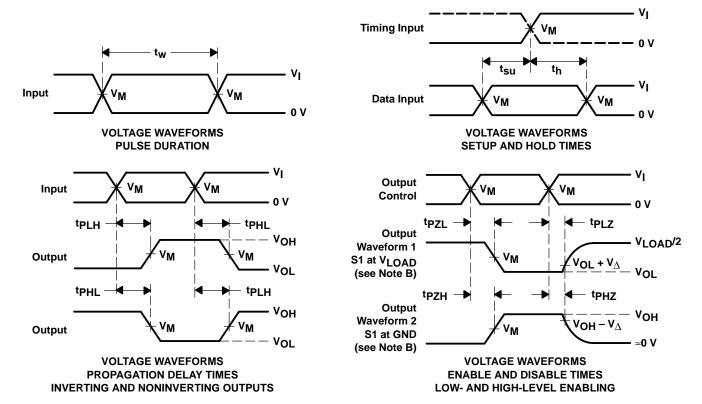
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	23	23	23	25	pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INPUTS			V	0	í	\ \ \
VCC	٧ <sub>I</sub>	V <sub>I</sub> t <sub>r</sub> /t <sub>f</sub> V <sub>M</sub>		VLOAD	CL	$R_L$	$V_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V ± 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

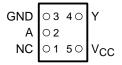
Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# NC 1 5 V<sub>CC</sub> A 1 2 GND 13 4 Y

#### YEA PACKAGE (BOTTOM VIEW)



NC - No internal connection

#### description

This single inverter gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G04 performs the Boolean function  $Y = \overline{A}$ .

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

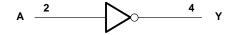
TA	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G04YEAR	cc_
	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G04DBVR	C04_
	SOP (SC-70) - DCK	Tape and reel	SN74LVC1G04DCKR	CC_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.



<sup>&</sup>lt;sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of  $V_{\hbox{CC}}$  is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
V	Cupply valtage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
\ <i>/</i>	High level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
V/	Low lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
٧ <sub>I</sub>	Input voltage		0	5.5	V	
۷o	Output voltage		0	VCC	V	
		V <sub>CC</sub> = 1.65 V		-4		
	High-level output current	V <sub>CC</sub> = 2.3 V		-8		
loh		V <sub>CC</sub> = 3 V		-16	mA	
		VCC = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V3V		16	mA	
		VCC = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYPT MA	X UNIT
	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
.,	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
VOH	$I_{OH} = -16 \text{ mA}$	2.1/	2.4		
	I <sub>OH</sub> = -24 mA	3 V	2.3		
	I <sub>OH</sub> = -32 mA	4.5 V	3.8		
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V		C	.1
	I <sub>OL</sub> = 4 mA	1.65 V		0.4	.5
.,	I <sub>OL</sub> = 8 mA	2.3 V		C	3
VOL	I <sub>OL</sub> = 16 mA	2.1/		C	4 V
	I <sub>OL</sub> = 24 mA	3 V		0.	55
	I <sub>OL</sub> = 32 mA	4.5 V		0.	55
lį	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		:	:5 μA
I <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$	0		±	0 μΑ
ICC	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			0 μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		5	0 μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5	pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

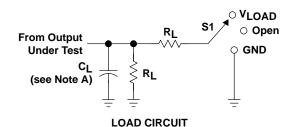
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		ν <sub>CC</sub> =		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	А	Υ	3	7.5	1.4	5.2	1	4.2	1	3.7	ns

#### operating characteristics, $T_A = 25^{\circ}C$

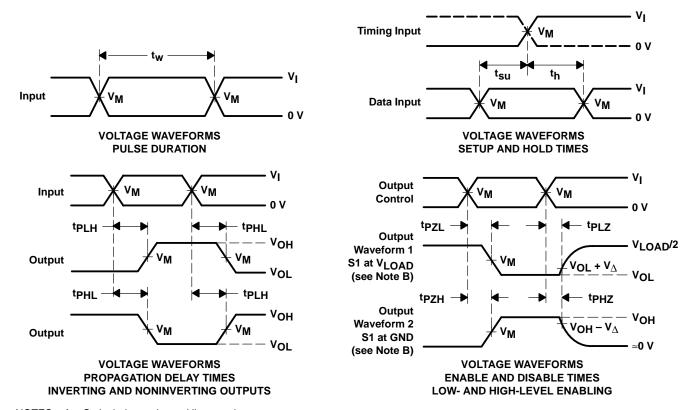
Г		PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
	PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONII	
	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	16	18	18	20	pF	

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INPUTS		.,			_	.,
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- Unbuffered Output
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description

This single inverter gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

#### 

NC - No internal connection

The SN74LVC1GU04 contains one inverter with an unbuffered output, and performs the Boolean function  $Y = \overline{A}$ .

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>	•	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1GU04YEAR	CD_
	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1GU04DBVR	CU4_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1GU04DCKR	CD_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

<sup>&</sup>lt;sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	−50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vcc	Supply voltage		1.65	5.5	V
٧ıH	High-level input voltage	$I_{O} = -100 \mu A$	0.75 × V <sub>CC</sub>		V
$V_{IL}$	Low-level input voltage	I <sub>O</sub> = 100 μA		0.25 × V <sub>CC</sub>	V
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 1.65 V		-4	
	IOH High-level output current	V <sub>CC</sub> = 2.3 V		-8	mA
loh		V <sub>CC</sub> = 3 V		-16	
		VCC = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 3 V		16	mA
		√GC = 3 v		24	
		$V_{CC} = 4.5 \text{ V}$		32	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
		I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
M	V <sub>II</sub> = 0 V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
VOH	VIL = 0 V	$I_{OH} = -16 \text{ mA}$	3 V	2.4			V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
V	\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	V
VOL	VIH= VCC	I <sub>OL</sub> = 16 mA	2.1/			0.4	]
		I <sub>OL</sub> = 24 mA	3 V			0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
lį	V <sub>I</sub> = 5.5 V or GND		0 to 5.5 V			±5	μΑ
Icc	V <sub>I</sub> = 5.5 V or GND,	IO = 0	1.65 V to 5.5 V			10	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND		3.3 V		7		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

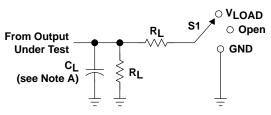
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (INPUT) (OUTPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(1141 01)	(1017-01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1.3	5	1	4	1.1	3.7	1	3	ns

#### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V V <sub>CC</sub> = 3.3 V		V <sub>CC</sub> = 5 V	UNIT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	9	11	13	27	pF	

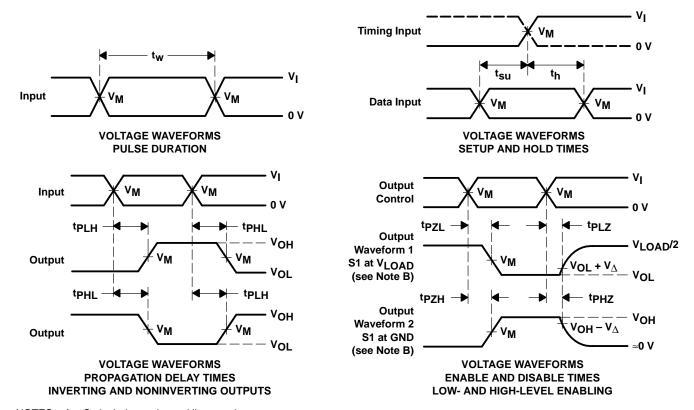
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

**LOAD CIRCUIT** 

V	INPUTS			V	0	Б.	V
vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

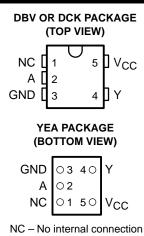
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



SCES295E - JUNE 2000 - REVISED AUGUST 2001

- Available in Texas Instruments' NanoStar™ **Package**
- Supports 5-V V<sub>CC</sub> Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

This single inverter buffer/driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

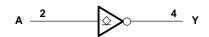
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
1000 / 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G06YEAR	CT
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G06DBVR	C06_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G06DCKR	CT_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

SCES295E - JUNE 2000 - REVISED AUGUST 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or p	power-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>Stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cumply voltage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
\/	High level input valtage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
V	Low lovel input veltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V
$V_{IL}$	√ <sub>IL</sub> Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	5.5	V
		V <sub>CC</sub> = 1.65 V		4	
		$V_{CC} = 2.3 \text{ V}$		8	
loL	Low-level output current	V <sub>CC</sub> = 3 V		16	mA
		VCC = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCES295E - JUNE 2000 - REVISED AUGUST 2001

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN TYPT MAX	UNIT
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45	
\/ - ·	I <sub>OL</sub> = 8 mA	2.3 V	0.3	V
VOL	I <sub>OL</sub> = 16 mA	2.1/	0.4	V
	I <sub>OL</sub> = 24 mA	3 V	0.55	
	I <sub>OL</sub> = 32 mA	4.5 V	0.55	
lį	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0	±10	μΑ
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V	500	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V	4	pF
Co	$V_O = V_{CC}$ or GND	3.3 V	5	pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

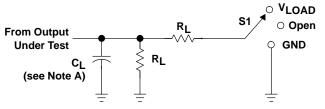
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO (OUTPUT)	V <sub>CC</sub> =		UNIT							
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t <sub>pd</sub>	Δ	<b>V</b>	2.2	5.6	1.1	4	1.2	1	1	વ	ns

#### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

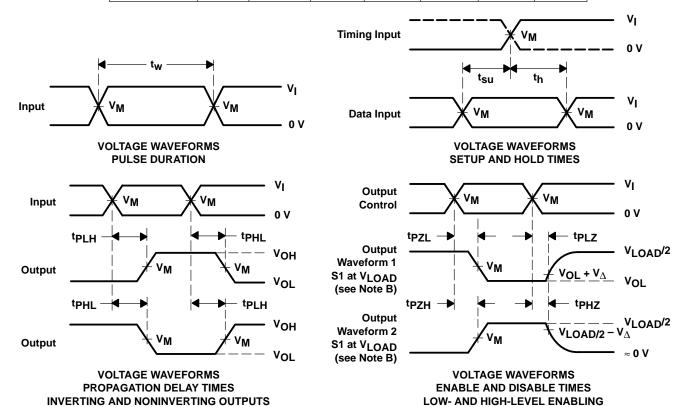
# PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	<b>S1</b>
tPZL (see Notes E and F)	VLOAD
tPLZ (see Notes E and G)	VLOAD
tPHZ/tPZH	VLOAD

**LOAD CIRCUIT** 

	IN	IPUT					
VCC	VI	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤ <b>2.5</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. Since this device has open-drain outputs, tpLz and tpzL are the same as tpd.
- F. tp7I is measured at V<sub>M</sub>.
- G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



SCES296F - FEBRUARY 2000 - REVISED AUGUST 2001

- Available in Texas Instruments' NanoStar™ **Package**
- Supports 5-V V<sub>CC</sub> Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- Ioff Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### **DBV OR DCK PACKAGE** (TOP VIEW) NC АΓ GND [ YEA PACKAGE (BOTTOM VIEW) 0340

NC - No internal connection

#### description

This single buffer/driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>	-	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 / 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G07YEAR	cv
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G07DBVR	C07_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G07DCKR	CV_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	Н
L	L

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

SCES296F - FEBRUARY 2000 - REVISED AUGUST 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	–0.5 V to 6.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/	Cupply valtage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		V	
		V <sub>CC</sub> = 1.65 V to 1.95 V				
V	Lligh level input veltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V	
VIH	nigri-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V	
	Low-level input voltage  Input voltage  Output voltage  Low-level output current	V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
V	Low level input valtage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V	
			$0.3 \times V_{CC}$			
٧ <sub>I</sub>	Input voltage		0	5.5	V	
٧o	Output voltage		0	5.5	V	
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
loL	Low-level output current	V 0 0 - 2 V		16	mA	
		VCC = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		]		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCES296F - FEBRUARY 2000 - REVISED AUGUST 2001

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN TYPT MAX	UNIT
	$I_{OL} = 100 \mu\text{A}$	1.65 V to 5.5 V	0.1	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45	
.,,	I <sub>OL</sub> = 8 mA	2.3 V	0.3	.,
VOL	I <sub>OL</sub> = 16 mA	2.1/	0.4	V
	I <sub>OL</sub> = 24 mA	3 V	0.55	
	I <sub>OL</sub> = 32 mA	4.5 V	0.55	
lį	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0	±10	μΑ
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V	500	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V	4	pF
Co	$V_O = V_{CC}$ or GND	3.3 V	5	pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

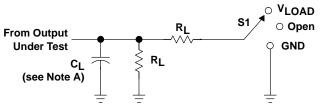
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	PARAMETER FROM TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<sup>t</sup> pd	A	Y	2.4	8.3	1	5.5	1.5	4.2	1	3.5	ns

#### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP TYP		TYP	TYP	UNII
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF

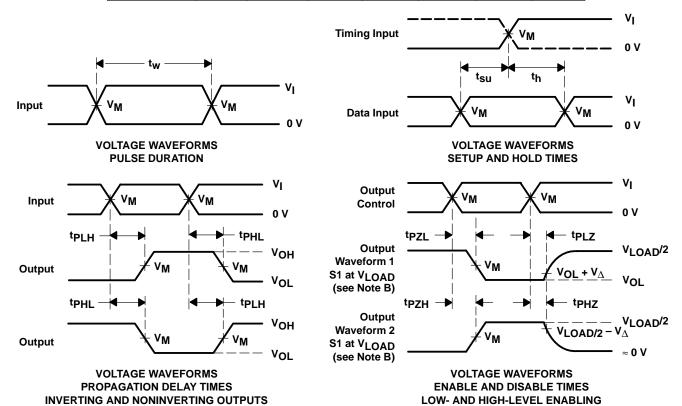
#### PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	<b>S1</b>
tpzL (see Notes E and F)	VLOAD
tpLZ (see Notes E and G)	VLOAD
tPHZ/tPZH	VLOAD

**LOAD CIRCUIT** 

	IN	IPUT							
vcc	VI	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$		
1.8 V $\pm$ 0.15 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V		
2.5 V $\pm$ 0.2 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	<b>500</b> Ω	0.15 V		
3.3 V $\pm$ 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V		
5 V $\pm$ 0.5 V	VCC	≤ <b>2.5</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V		

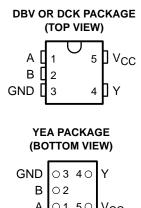


- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. Since this device has open-drain outputs, tpLZ and tpZL are the same as tpd.
  - F. tpzi is measured at V<sub>M</sub>.
  - G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

The SN74LVC1G08 performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A + B}$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGET	•	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 1- 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G08YEAR	CE_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G08DBVR	C08_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G08DCKR	CE_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Υ
Н	Н	Н
L	Χ	L
Х	L	L

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

<sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or po	ower-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{ K }(V_{ C } < 0)$	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT			
Vaa	Supply voltage	Operating	1.65	5.5	V			
VCC	Supply voltage	Data retention only	1.5		l v			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$					
\/	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		\/			
VIH	riigii-ieveriiiput voitage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		\ \			
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$					
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>				
٧/	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		8.0	ľ			
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$				
٧ <sub>I</sub>	Input voltage		0	5.5	V			
٧o	Output voltage		0	Vcc	V			
		V <sub>CC</sub> = 1.65 V		-4				
	High-level output current	V <sub>CC</sub> = 2.3 V		-8				
loh		V <sub>CC</sub> = 3 V		-16	mA			
		VCC = 3 V		-24				
		V <sub>CC</sub> = 4.5 V		-32				
		V <sub>CC</sub> = 1.65 V		4				
		V <sub>CC</sub> = 2.3 V		8				
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 3 V		16	mA			
		VCC = 3 V		24				
		V <sub>CC</sub> = 4.5 V		32				
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20				
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V			
		$V_{CC} = 5 V \pm 0.5 V$		5				
TA	Operating free-air temperature		-40	85	°C			

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
V		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
	I <sub>OL</sub> = 100 μA		1.65 V to 5.5 V			0.1	
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45	
\/ - ·		$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	V
VOL		$I_{OL} = 16 \text{ mA}$	2.1/			0.4	V
		I <sub>OL</sub> = 24 mA	3 V			0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
ΙĮ	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
l <sub>off</sub>		$V_I \text{ or } V_O = 5.5 \text{ V}$	0			±10	μΑ
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
∆lCC		One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V			500	μΑ
Ci		$V_I = V_{CC}$ or GND	3.3 V		4	·	pF

<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

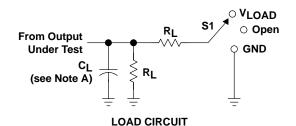
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
		(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.4	8	1.1	5.5	1	4.5	1	4	ns

#### operating characteristics, $T_A = 25^{\circ}C$

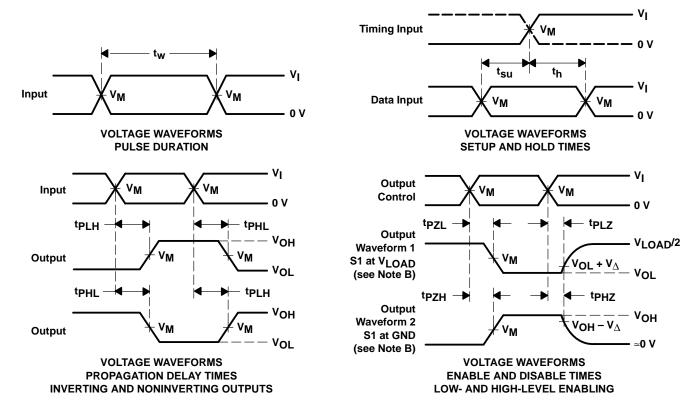
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	21	24	26	31	pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INF	PUTS			0	D.	\ \ \
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	RL	$V_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# 

#### NC - No internal connection

#### description

This single Schmitt-trigger inverter is designed for 1.65-V to 5.5-V  $\rm V_{CC}$  operation.

The SN74LVC1G14 device contains one inverter, and performs the Boolean function  $Y = \overline{A}$ . The device functions as an independent inverter, but because of Schmitt action, it may have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

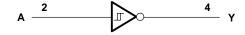
TA	PACKAGE <sup>†</sup>	•	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 to 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G14YEAR	CF_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G14DBVR	C14_
	SOP (SC-70) - DCK	Tape and reel	SN74LVC1G14DCKR	CF_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)



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DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or po	ower-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/	Cupply voltage	Operating	1.65	5.5	V
Vcc	Supply voltage	Data retention only	1.5		V
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
IOH	High-level output current	V <sub>CC</sub> = 3 V		-16	mA
				-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 0 V		16	mA
		VCC = 3 V		24	
	V	V <sub>CC</sub> = 4.5 V		32	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	ONDITIONS	vcc	MIN	TYPT MAX	UNIT
			1.65 V	0.79	1.16	
V <sub>T+</sub>			2.3 V	1.11	1.56	
Positive-going input			3 V	1.5	1.87	V
threshold voltage			4.5 V	2.16	2.74	
			5.5 V	2.61	3.33	
			1.65 V	0.39	0.62	
V <sub>T</sub> _			2.3 V	0.58	0.87	
Negative-going input			3 V	0.84	1.14	V
threshold voltage			4.5 V	1.41	1.79	
			5.5 V	1.87	2.29	
			1.65 V	0.37	0.62	
$\Delta V_{T}$			2.3 V	0.48	0.77	
Hysteresis			3 V	0.56	0.87	V
$(V_{T+} - V_{T-})$			4.5 V	0.71	1.04	
			5.5 V	0.71	1.11	
	I <sub>OH</sub> = -100 μA		1.65 V to 4.5 V	V <sub>CC</sub> -0.1		
	I <sub>OH</sub> = -4 mA		1.65 V	1.2		
\/	I <sub>OH</sub> = -8 mA		2.3 V	1.9		V
VOH	I <sub>OH</sub> = -16 mA		3 V	2.4		V
	I <sub>OH</sub> = -24 mA		] 3 V	2.3		
	I <sub>OH</sub> = -32 mA		4.5 V	3.8		
	I <sub>OL</sub> = 100 μA		1.65 V to 4.5 V		0.1	
	I <sub>OL</sub> = 4 mA		1.65 V		0.45	
\/	I <sub>OL</sub> = 8 mA		2.3 V		0.3	V
VOL	I <sub>OL</sub> = 16 mA		2.1/		0.4	V
	I <sub>OL</sub> = 24 mA		3 V		0.55	
	I <sub>OL</sub> = 32 mA		4.5 V		0.55	
lį	V <sub>I</sub> = 5.5 V or GND		0 to 5.5 V		±5	μΑ
l <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0		±10	μΑ
lcc	$V_I = 5.5 \text{ V or GND},$	I <sub>O</sub> = 0	1.65 V to 5.5 V		10	μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		4.5	pF

 $<sup>\</sup>uparrow$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		= V <sub>CC</sub> ± 0.		UNIT
	(1141 01)	(101701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

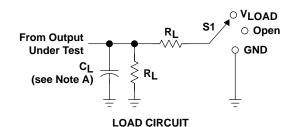
#### SN74LVC1G14 SINGLE SCHMITT-TRIGGER INVERTER

SCES218F - APRIL 1999 - REVISED JULY 2001

#### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	$V_{CC} = 2.5 \text{ V}$	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	20	21	22	25	pF

#### PARAMETER MEASUREMENT INFORMATION



5 V  $\pm$  0.5 V

TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

	INPUTS		.,	.,		_	.,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V

V<sub>CC</sub>/2

 $\textbf{2} \times \textbf{V}_{\textbf{CC}}$ 

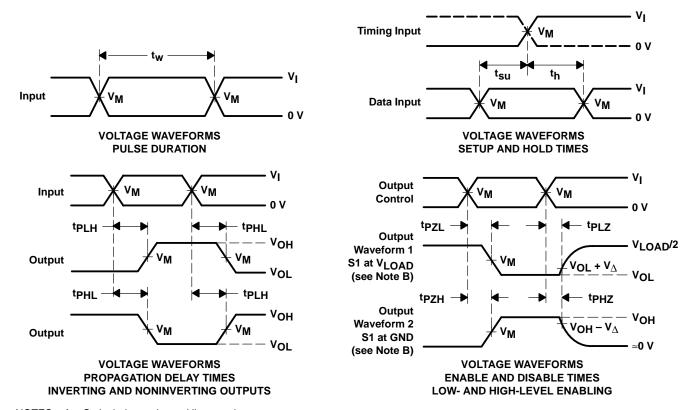
50 pF

500  $\Omega$ 

0.3 V

≤2.5 ns

**VCC** 



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



SCES351A - JUNE 2001 - REVISED JULY 2001

- Available in Texas Instruments' NanoStar™ Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### 

#### description

NC - No internal connection

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G17 contains one buffer and performs the Boolean function Y = A. The device functions as an independent buffer, but because of Schmitt action, it may have different input threshold levels for positive-going  $(V_{T+})$  and negative-going  $(V_{T-})$  signals.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 1- 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G17YEAR	C7_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G17DBVR	C17_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G17DCKR	C7_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	Н
L	L

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.



DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

SCES351A - JUNE 2001 - REVISED JULY 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	-0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, I <sub>O</sub>	
Continuous current through V <sub>CC</sub> or GND	
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>sta</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/	Cumphyyoltoma	Operating	1.65 5.5		V	
Vcc	Data retention  Input voltage  Output voltage  VCC = 1.65 V VCC = 2.3 V  VCC = 3 V  VCC = 4.5 V  VCC = 1.65 V  VCC = 3 V  VCC = 2.3 V	Data retention only	1.5		V	
٧ <sub>I</sub>	Input voltage		0	5.5	V	
۷o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
		V <sub>CC</sub> = 2.3 V		-8		
loh	High-level output current	V <sub>CC</sub> = 3 V		-16	mA	
				-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V2V		16	mA	
		ACC = 2 A		24		
	Vcc	V <sub>CC</sub> = 4.5 V		32		
TA	Operating free-air temperature	_	-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



SCES351A - JUNE 2001 - REVISED JULY 2001

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CO	ONDITIONS	vcc	MIN	TYPT MAX	UNIT
			1.65 V	0.76	1.13	
V <sub>T+</sub>			2.3 V	1.08	1.56	
Positive-going input			3 V	1.48	1.92	V
threshold voltage			4.5 V	2.19	2.74	
			5.5 V	2.65	3.33	
			1.65 V	0.35	0.59	
$V_{T-}$			2.3 V	0.56	0.88	
Negative-going input			3 V	0.89	1.2	V
threshold voltage			4.5 V	1.51	1.97	
			5.5 V	1.88	2.4	
			1.65 V	0.36	0.64	
$\Delta V_{T}$			2.3 V	0.45	0.78	
Hysteresis			3 V	0.51	0.83	V
$(V_{T+} - V_{T-})$			4.5 V	0.58	0.93	
			5.5 V	0.69	1.04	
	I <sub>OH</sub> = -100 μA		1.65 V to 4.5 V	V <sub>CC</sub> -0.1		
	I <sub>OH</sub> = -4 mA		1.65 V	1.2		
\/a	I <sub>OH</sub> = –8 mA		2.3 V	1.9		V
VOH	I <sub>OH</sub> = -16 mA		3 V	2.4		V
	I <sub>OH</sub> = -24 mA		3 V	2.3		
	I <sub>OH</sub> = -32 mA		4.5 V	3.8		
	I <sub>OL</sub> = 100 μA		1.65 V to 4.5 V		0.1	
	I <sub>OL</sub> = 4 mA		1.65 V		0.45	
\/	I <sub>OL</sub> = 8 mA		2.3 V		0.3	V
VOL	I <sub>OL</sub> = 16 mA		3 V		0.4	V
	I <sub>OL</sub> = 24 mA		3 V		0.55	
	I <sub>OL</sub> = 32 mA		4.5 V		0.55	
lį	V <sub>I</sub> = 5.5 V or GND		0 to 5.5 V		±5	μΑ
loff	V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0		±10	μΑ
lcc	$V_I = 5.5 \text{ V or GND},$	I <sub>O</sub> = 0	1.65 V to 5.5 V		10	μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		4.5	pF

 $<sup>\</sup>uparrow$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		= V <sub>CC</sub> ± 0.		UNIT
	(1141 01)	(001101)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	Α	Υ	3.8	11	2	6.5	1.8	5.5	1.2	5	ns

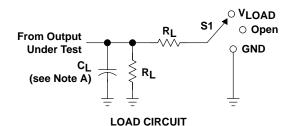
#### SN74LVC1G17 SINGLE SCHMITT-TRIGGER BUFFER

SCES351A - JUNE 2001 - REVISED JULY 2001

#### operating characteristics, $T_A = 25^{\circ}C$

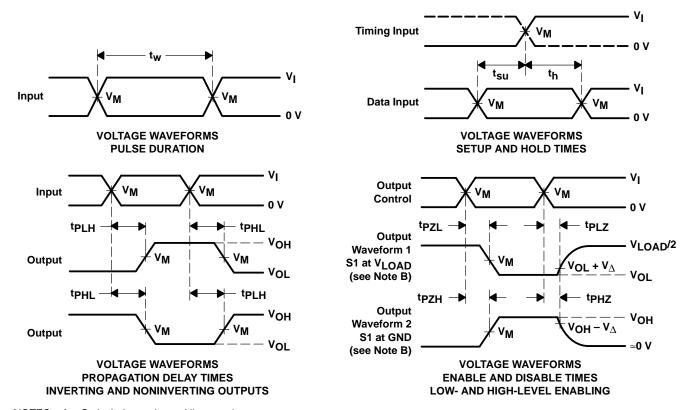
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V   V <sub>CC</sub> = 2.5 V   V <sub>CC</sub> = 3.3 V   V <sub>CC</sub>		V <sub>CC</sub> = 5 V	UNIT	
		TEST CONDITIONS	TYP	TYP	TYP TYP		UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	20	21	22	26	pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

Wa a	INPUTS			V	0	В.	V
VCC	VI	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™ Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# DBV OR DCK PACKAGE (TOP VIEW) A 1 5 VCC B 2 YCC GND 3 4 Y YEA PACKAGE (BOTTOM VIEW) GND 3 40 Y B 02 A 01 50 VCC

#### description

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G32 performs the Boolean function Y = A + B or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G32YEAR	CG_
	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G32DBVR	C32_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G32DCKR	CG_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Υ
Н	Χ	Н
Х	Н	Н
L	L	L

#### logic diagram (positive logic)



NanoStar is a trademark of Texas Instruments.

TEXAS INSTRUMENTS

<sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or po	ower-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{ K }(V_{ } < 0)$	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/	Cupality selfage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
١/	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		
VIH	nigh-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
$V_{IL}$	Low level input valtage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	] , [
	Low-level input voltage  VCC = 3 V to 3.6 V		0.8	ı v	
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	V
۷o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	mA
	High-level output current	V <sub>CC</sub> = 2.3 V		-8	
IOH		V 2.V		-16	
		VCC = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2 V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	v <sub>cc</sub>	MIN	TYP <sup>†</sup>	MAX	UNIT	
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		$I_{OH} = -32 \text{ mA}$	2.3 V 1.9  3 V 2.4  3 V 3.8  1.65 V to 5.5 V 0.1  1.65 V 0.45  2.3 V 0.3  3 V 0.55  4.5 V 0.55					
		$I_{OL} = 100 \mu\text{A}$	1.65 V to 5.5 V			0.1		
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45		
\/		$I_{OL} = 8 \text{ mA}$	2.3 V			0.3		
VOL		$I_{OL} = 16 \text{ mA}$	2.1/			0.4	V	
		$I_{OL} = 24 \text{ mA}$	3 V			1		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
П	A or B inputs	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>		$V_I$ or $V_O = 5.5 V$	0			±10	μΑ	
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
∆lcc		One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V			500	μΑ	
Ci		$V_I = V_{CC}$ or GND	3.3 V		4	·	pF	

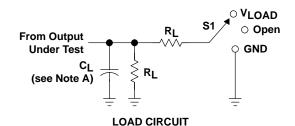
<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Υ	2.8	8	1.2	5.5	1.1	4.5	1	4	ns

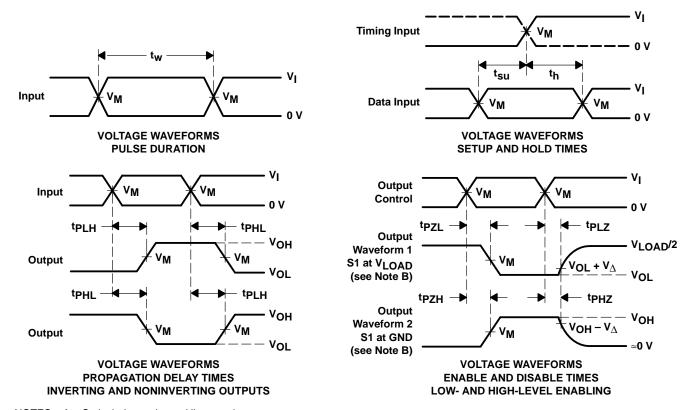
#### operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
	FARAWETER	TEST CONDITIONS	TYP TYP		TYP	TYP	ONII
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	20	20	21	22	pF



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

Vcc		INPUTS		,,	.,		RL	.,
		٧ı	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	KL	$oldsymbol{V}_\Delta$
1.8 \	V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5	$V \pm 0.2 V$	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3	$V \pm 0.3 V$	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V	$\prime \pm$ 0.5 V	Vcc	≤2.5 ns	V <sub>CC</sub> /2	2×VCC	50 pF	<b>500</b> Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

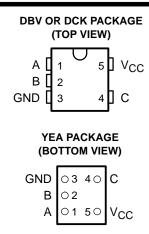
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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- Available in Texas Instruments' NanoStar™
   Package
- 1.65-V to 5.5-V V<sub>CC</sub> Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed Typically 0.5 ns (V<sub>CC</sub> = 3 V, C<sub>L</sub> = 50 pF)
- Low On-State Impedance Typically ≈5.5 Ω (V<sub>CC</sub> = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

This single analog switch is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

#### ORDERING INFORMATION

TA	PACKAGET	•	ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G66YEAR	C6
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G66DBVR	C66_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G66DCKR	C6_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### **FUNCTION TABLE**

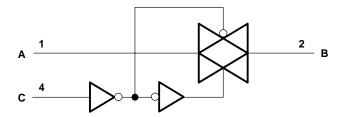
CONTROL INPUT (C)	SWITCH
L	OFF
Н	ON

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<sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	–0.5 V to 6.5 V
Switch I/O voltage range, V <sub>I/O</sub> (see Notes 1, 2, and 3)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Control input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
I/O port diode current, $I_{IOK}$ ( $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$ )	±50 mA
On-state switch current, $I_T (V_{I/O} = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 4): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
  - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 3. This value is limited to 5.5 V maximum.
  - 4. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 5)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	5.5	V	
V <sub>I/O</sub>	I/O port voltage		0	Vcс	V	
		V <sub>CC</sub> = 1.65 V to 1.95 V	V <sub>CC</sub> × 0.65			
\/	High level input voltage, central input	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V <sub>CC</sub> × 0.7		V	
VIH	High-level input voltage, control input	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> × 0.7		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V <sub>CC</sub> × 0.7			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		V <sub>CC</sub> × 0.35		
\/	Low lovel input valtage, control input	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$	V	
$V_{IL}$	Low-level input voltage, control input	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		$V_{CC} \times 0.3$	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$		
٧ <sub>I</sub>	Control input voltage		0	5.5	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		20		
Δt/Δν	lanut transition via Mall time	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		20	20/1	
Δι/Δν	Input transition rise/fall time	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		10	115/V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		10		
T <sub>A</sub>	Operating free-air temperature		-40	85	°C	

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	DITIONS	VCC	MIN TY	/P <sup>†</sup>	MAX	UNIT	
			I <sub>S</sub> = 4 mA	1.65 V		12	30		
_	On-state switch resistance	$V_I = V_{CC}$ or GND,	$I_S = 8 \text{ mA}$	2.3 V		9	20	Ω	
ron	On-state switch resistance	$V_C = V_{IH}$ (see Figures 1 and 2)	I <sub>S</sub> = 24 mA	3 V		7.5	15	22	
		<b>3</b> ,	Is = 32 mA	4.5 V		5.5	10		
			I <sub>S</sub> = 4 mA	1.65 V	7	4.5	100		
	Peak on resistance	$V_I = V_{CC}$ to GND,	I <sub>S</sub> = 8 mA	2.3 V		20	30	Ω	
ron(p)	Peak on resistance	V <sub>C</sub> = V <sub>IH</sub> (see Figures 1 and 2)	I <sub>S</sub> = 24 mA	3 V	1	1.5	20	22	
		(coo : .gaa : aa =/	I <sub>S</sub> = 32 mA	4.5 V		7.5	15		
	Off state switch had a management	$V_I = V_{CC}$ and $V_O = GI$		5.5.7			±1		
IS(off)	Off-state switch leakage current	$V_I = GND \text{ and } V_O = V_O$ $V_C = V_{IL} \text{ (see Figure 3)}$		5.5 V			±0.1 <sup>†</sup>	μΑ	
lo( )	On state switch lookage current	$V_I = V_{CC}$ or GND, $V_C$	= V <sub>IH</sub> , V <sub>O</sub> = Open	5.5 V			±1		
IS(on)	On-state switch leakage current	(see Figure 4)		5.5 V			±0.1 <sup>†</sup>	μΑ	
II	Control input current	V <sub>C</sub> = V <sub>CC</sub> or GND		5.5 V			±1	μА	
'	Control input current	VC = VCC 01 GIVD		3.5 V			±0.1 <sup>†</sup>	μΛ	
loo	Supply current	V <sub>C</sub> = V <sub>CC</sub> or GND		5.5 V			10	μΑ	
ICC	Зарріў сапені	VC = VCC 01 GIVD		3.5 V			1†	μΛ	
∆ICC	Supply current change	$V_C = V_{CC} - 0.6 V$	$V_C = V_{CC} - 0.6 V$				500	μΑ	
C <sub>ic</sub>	Control input capacitance			5 V		2		pF	
C <sub>io(off)</sub>	Switch input/output capacitance			5 V		6	·	pF	
C <sub>io(on)</sub>	Switch input/output capacitance			5 V		13		рF	

<sup>†</sup> T<sub>A</sub> = 25°C

#### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		VCC =		UNIT
	(IIII O1)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub> ‡	A or B	B or A		2		1.2		8.0		0.6	ns
t <sub>en</sub> §	С	A or B	2.5	12	1.9	6.5	1.8	5	1.5	4.2	ns
t <sub>dis</sub> ¶	С	A or B	2.2	10	1.4	6.9	2	6.5	1.4	5	ns

<sup>‡</sup> tpLH and tpHL are the same as tpd. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).

§ tpZL and tpHZ are the same as ten.

¶ tpLZ and tpHZ are the same as tdis.



SCES323A - JUNE 2001 - REVISED AUGUST 2001

#### analog switch characteristics, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	VCC	TYP	UNIT	
				1.65 V	35	35   200   75   395   MHz   300   30	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	120		
			f <sub>in</sub> = sine wave (see Figure 6)	3 V	175		
Frequency response†	A or B	B or A	,	4.5 V	195	MHz	
(switch ON)	N OI B	B 0174		1.65 V	>300	1411.12	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$ $f_{\text{in}} = \text{sine wave}$	2.3 V	>300		
			(see Figure 6)	3 V	>300		
				4.5 V	>300		
				1.65 V	35		
Crosstalk	С	A or B	$C_L$ = 50 pF, $R_L$ = 600 $Ω$ , $f_{in}$ = 1 MHz (square wave)	2.3 V	50	m∨	
(control input to signal output)	Ü	7.012	(see Figure 7)	3 V	70	mV	
				4.5 V	100		
			0 50 5 0 000 0	1.65 V			
			$C_L$ = 50 pF, $R_L$ = 600 $Ω$ , $f_{in}$ = 1 MHz (sine wave)	2.3 V	-58	8	
			(see Figure 8)	3 V	-58		
Feed-through attenuation <sup>‡</sup>	A or B	B or A		4.5 V	-58	dB	
(switch OFF)			C. 5 . E D. 50 O	1.65 V	-42		
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$ $f_{\text{in}} = 1 \text{ MHz (sine wave)}$	2.3 V	-42		
			(see Figure 8)	3 V	-42		
				4.5 V	-42		
			C 50 pF B 10 kO	1.65 V	0.1		
			$C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kHz (sine wave)	2.3 V	0.025		
			(see Figure 9)	3 V	0.015		
Sine-wave distortion	A or B	B or A		4.5 V	0.01	%	
			C. = 50 pE B. = 10 kg	1.65 V	0.15		
			$C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 10 kHz (sine wave)	2.3 V	0.025		
			(see Figure 9)	3 V	0.015		
				4.5 V	0.01		

<sup>†</sup> Adjust f<sub>in</sub> voltage to obtain 0 dBm at output. Increase f<sub>in</sub> frequency until dB meter reads –3 dB. ‡ Adjust f<sub>in</sub> voltage to obtain 0 dBm at input.

#### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	8	9	9	11	pF

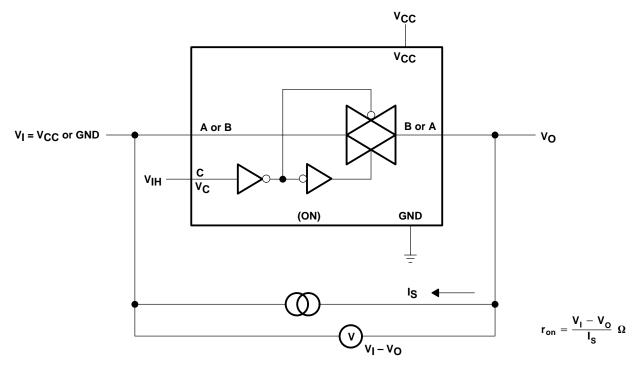


Figure 1. On-State Resistance Test Circuit

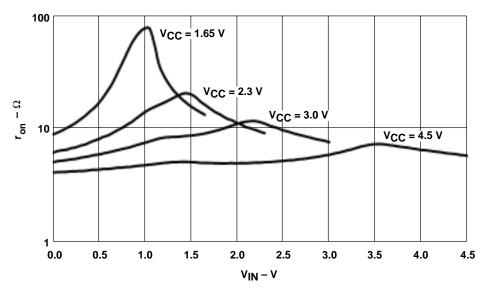


Figure 2. Typical  $r_{on}$  as a Function of Input Voltage (V<sub>I</sub>) for V<sub>I</sub> = 0 to V<sub>CC</sub>

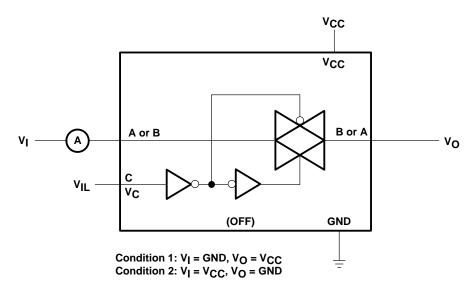


Figure 3. Off-State Switch Leakage-Current Test Circuit

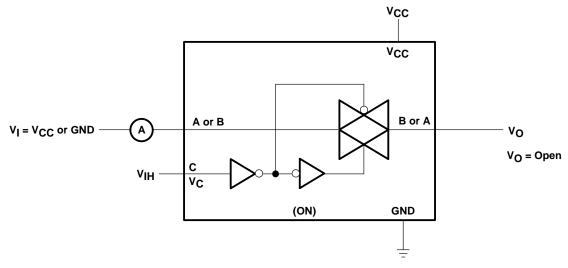
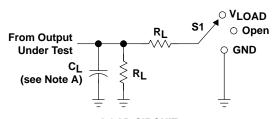


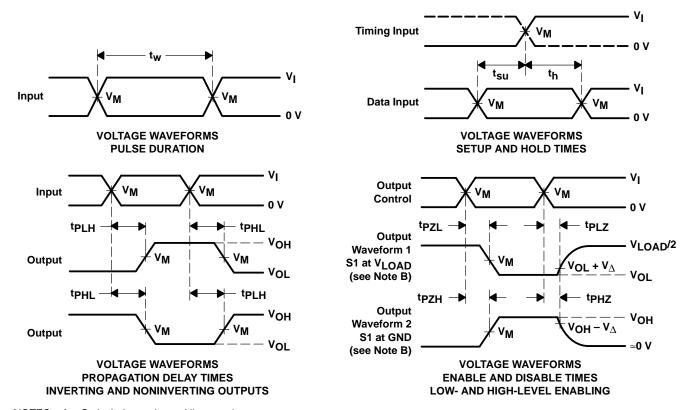
Figure 4. On-State Leakage-Current Test Circuit



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

IRCUIT

W	INF	PUTS		V	0	í	, , , , , , , , , , , , , , , , , , ,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×VCC	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms



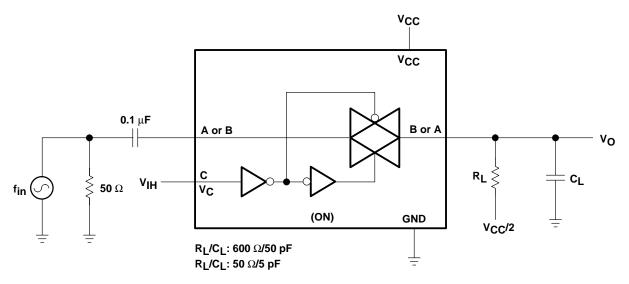


Figure 6. Frequency Response (Switch ON)

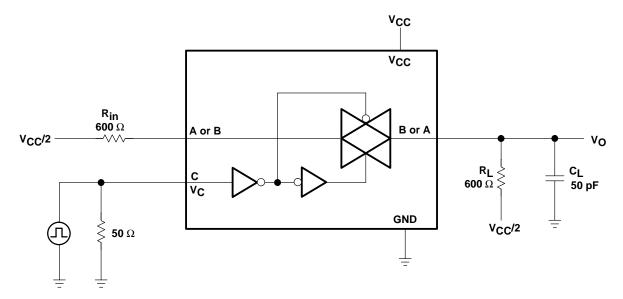


Figure 7. Crosstalk (Control Input – Switch Output)

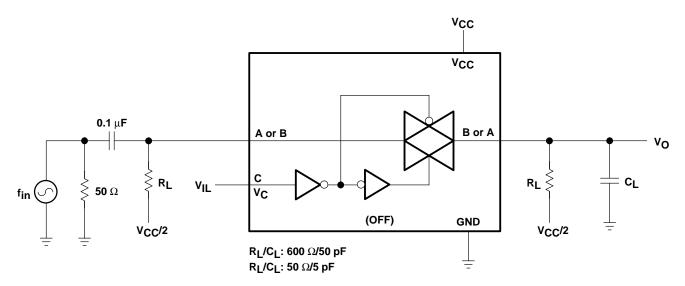


Figure 8. Feedthrough (Switch Off)

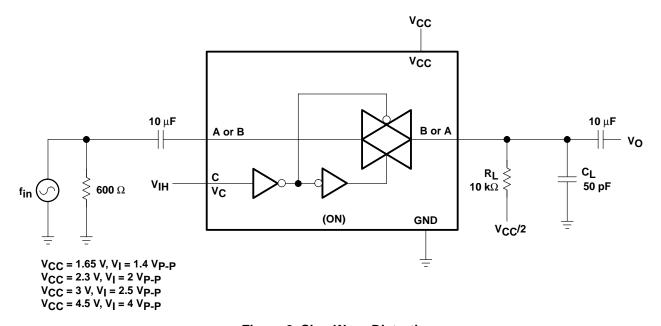


Figure 9. Sine-Wave Distortion

#### SN74LVC1G79 SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220G - APRIL 1999 - REVISED JULY 2001

Available in Texas Instruments' NanoStar™
 Package

- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# DBV OR DCK PACKAGE (TOP VIEW) D 1 5 VCC CLK 2 GND 3 4 Q YEA PACKAGE (BOTTOM VIEW) GND 3 40 Q CLK 2 D 1 50 VCC

#### description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 1 - 0500	NanoStar WCSP (DSBGA) – YEA		SN74LVC1G79YEAR	CR_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G79DBVR	C79_
	SOP (SC-70) - DCK	Tape and reel	SN74LVC1G79DCKR	CR_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

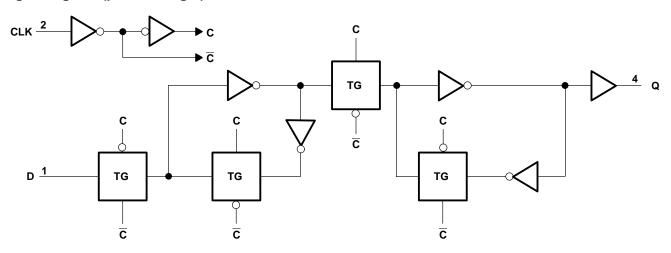
#### **FUNCTION TABLE**

INPL	JTS	OUTPUT
CLK D		Q
1	Н	Н
1	L	L
L	Χ	$Q_0$

NanoStar is a trademark of Texas Instruments.

DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### SN74LVC1G79 SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES220G - APRIL 1999 - REVISED JULY 2001

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/os	Supply voltage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		V	
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>			
\ <i>/</i>	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V		
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		\ \ \	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>C</sub> C		
V/	Laurence in mortunal tames	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V	
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>		
٧ı	Input voltage	•	0	5.5	V	
۷o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
		V <sub>CC</sub> = 2.3 V		-8		
ЮН	High-level output current	V 2 V		-16	mA	
		VCC = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current			16	mA	
		V <sub>CC</sub> = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		10	ns/V	
		V <sub>CC</sub> = 5 V ± 0.5 V		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAME	ETER	TEST CO	ONDITIONS	VCC	MIN	TYP†	MAX	UNIT
		I <sub>OH</sub> = -100 μA		1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$		1.65 V	1.2			
\/		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9				
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		I <sub>OH</sub> = -24 mA	3 V	2.3				
		I <sub>OH</sub> = -32 mA	4.5 V	3.8				
		I <sub>OL</sub> = 100 μA		1.65 V to 5.5 V			0.1	
		$I_{OL} = 4 \text{ mA}$	1.65 V			0.45		
\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \		$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	V	
VOL		I <sub>OL</sub> = 16 mA		2.1/			0.4	V
		I <sub>OL</sub> = 24 mA		3 V			0.55	
		I <sub>OL</sub> = 32 mA		4.5 V			0.55	
l <sub>l</sub> Dir	nput	V <sub>I</sub> = 5.5 V or GND		0 to 5.5 V			±10	μΑ
l <sub>off</sub>		$V_I$ or $V_O = 5.5 V$		0			±10	μΑ
Icc		V <sub>I</sub> = 5.5 V or GND,	IO = 0	1.65 V to 5.5 V			10	μΑ
∆lCC		One input at V <sub>CC</sub> – 0.6 V,	Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
Ci		$V_I = V_{CC}$ or GND		3.3 V		4	·	pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> =		VCC =		VCC =		± 0.		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	f <sub>clock</sub> Clock frequency			160		160		160		160	MHz
t <sub>W</sub>	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
	Octor Cock to Cock OLK	Data high	2.2		1.4		1.3		1.2		
t <sub>Su</sub> Setup ti	Setup time before CLK↑	Data low	2.6		1.4		1.3		1.2		ns
th	Hold time, data after CLK↑		0.3		0.4	·	1		0.5	·	ns

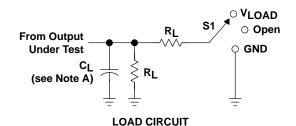
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			160		160		160		160		MHz
<sup>t</sup> pd	CLK	Q	3.9	9.9	2	7	1.7	5.2	1	4.5	ns

#### operating characteristics, T<sub>A</sub> = 25°C

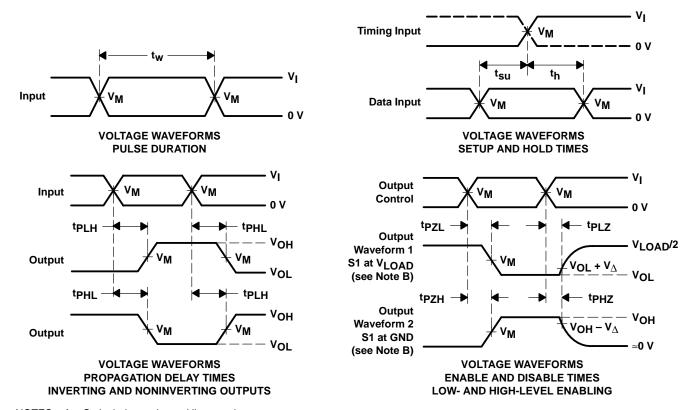
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	26	26	27	30	pF





TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INF	PUTS	.,	.,		_	.,
Vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

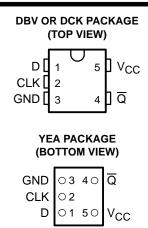
Figure 1. Load Circuit and Voltage Waveforms



#### SN74LVC1G80 SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES221G - APRIL 1999 - REVISED JULY 2001

- Available in Texas Instruments' NanoStar™ **Package**
- Supports 5-V V<sub>CC</sub> Operation
- Ioff Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the  $\overline{\mathbb{Q}}$  output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the level at the output.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE	-	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 1- 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G80YEAR	CX_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G80DBVR	C80_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G80DCKR	CX_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

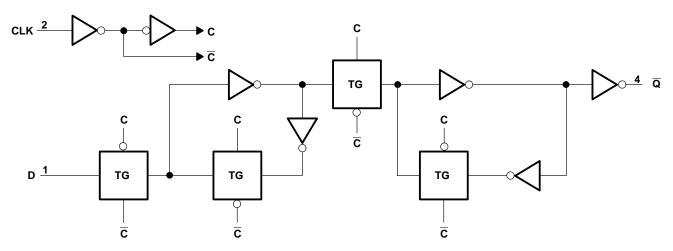
#### **FUNCTION TABLE**

INPL	JTS	ОИТРИТ
CLK	D	Q
1	Н	L
1	L	Н
L	Χ	$Q_0$

NanoStar is a trademark of Texas Instruments.

<sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74LVC1G80 SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP

SCES221G - APRIL 1999 - REVISED JULY 2001

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/os	Supply voltage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
\ <i>/</i>	High lovel input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		\ \ \
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>C</sub> C	
V/	Law lavel input valtage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
٧ı	Input voltage	•	0	5.5	V
۷o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
ЮН	High-level output current	V 2 V		-16	mA
		VCC = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current			16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		10	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAR	RAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
\/ - · ·		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
VOH		$I_{OH} = -16 \text{ mA}$	3 V	2.4			V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			
		$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	
VOL		I <sub>OL</sub> = 16 mA	2.1/			0.4	V
		I <sub>OL</sub> = 24 mA	3 V			0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
ΙĮ	D input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±10	μΑ
l <sub>off</sub>		$V_I$ or $V_O = 5.5 V$	0			±10	μΑ
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
∆lcc		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
Ci		$V_I = V_{CC}$ or GND	3.3 V		3.5	·	pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			V <sub>CC</sub> =		V <sub>CC</sub> =		VCC =		VCC =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	f <sub>clock</sub> Clock frequency			160		160		160		160	MHz
t <sub>W</sub>	Pulse duration, CLK high or low		2.5		2.5		2.5		2.5		ns
	Octor Constant OLIC	Data high	2.3		1.5		1.3		1.1		
t <sub>SU</sub> Setup time before CLK↑		Data low	2.5		1.5		1.3		1.1		ns
t <sub>h</sub>	Hold time, data after CLK↑		0		0.2		0.9		0.4		ns

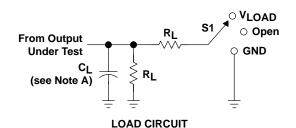
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	RAMETER FROM TO (OUTPUT)		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(IIVI O1)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			160		160		160		160		MHz
<sup>t</sup> pd	CLK	Q	4.4	9.9	2.3	7	2	5.2	1.3	4.5	ns

#### operating characteristics, T<sub>A</sub> = 25°C

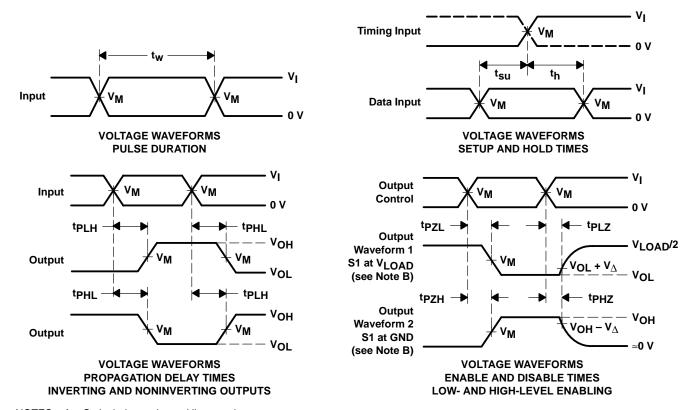
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP TYP TYP		TYP	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	24	24	25	27	pF





TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INF	PUTS	.,				.,
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



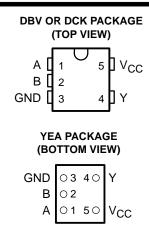
NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™ Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

This single 2-input exclusive-OR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G86 performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
4000 / 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G86YEAR	CH_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G86DBVR	C86_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G86DCKR	CH_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
н	Н	L

NanoStar is a trademark of Texas Instruments.

DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

# EXCLUSIVE OR

These are five equivalent exclusive-OR symbols valid for an SN74LVC1G86 gate in positive logic; negation may be shown at any two ports.

# 

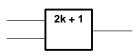
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

#### **EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

#### **ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Voltage range applied to any output in the high-impedance or power-off state, V <sub>O</sub>	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	1.000000000000000000000000000000000000
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	155°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cupply valtage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
\ <i>/</i>	High level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		v
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
V/	Low level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
$V_{IL}$	V <sub>IL</sub> Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	V
۷o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
loh	High-level output current	igh-level output current VCC = 3 V		-16	mA
		VCC = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 2V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		10	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
TA	Operating free-air temperature	<u> </u>	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP† MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
Vou	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V
Voн	$I_{OH} = -16 \text{ mA}$	3 V	2.4		_ v
	$I_{OH} = -24 \text{ mA}$	3 V	2.3		
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V		0.	
	I <sub>OL</sub> = 4 mA	1.65 V		0.4	5
Val	I <sub>OL</sub> = 8 mA	2.3 V		0.	3 <sub>V</sub>
VOL	I <sub>OL</sub> = 16 mA	3 V		0.	ı v
	I <sub>OL</sub> = 24 mA	3 V		0.5	5
	I <sub>OL</sub> = 32 mA	4.5 V		0.5	5
lį	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0		±1	μΑ
<sup>I</sup> CC	$V_I = V_{CC}$ or GND, $I_O = 0$	1.65 V to 5.5 V		1	μΑ
Δl <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		50	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V		6	pF

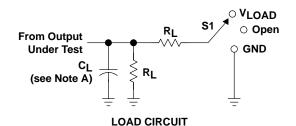
<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	A or B		3.5	9.9	1.8	5.5	1.3				ns

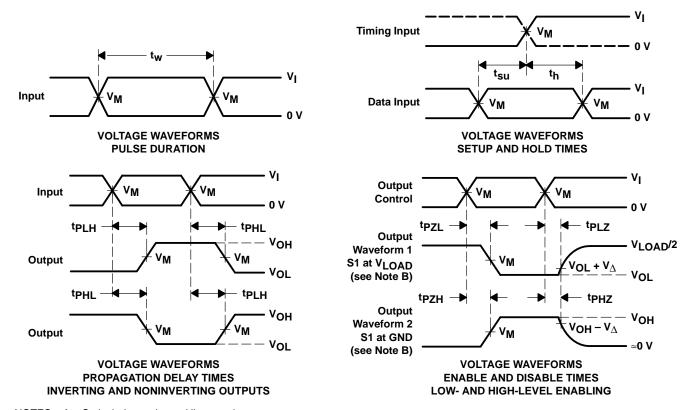
#### operating characteristics, T<sub>A</sub> = 25°C

	DADAMETED	PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 1.8 V V <sub>CC</sub> = 2.5 V		V <sub>CC</sub> = 3.3 V V <sub>CC</sub> = 5 V	
	PANAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
Cpc	Power dissipation capacitance	f = 10 MHz	22	22	22	24	pF



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INF	PUTS		V	0	í	, , , , , , , , , , , , , , , , , , ,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# DBV OR DCK PACKAGE (TOP VIEW) OE 1 5 VCC A 2 A Y YEA PACKAGE (BOTTOM VIEW) GND 03 40 Y A 02 OE 01 50 VCC

#### description

This bus buffer gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G125 is a single line driver with a 3-state output. The output is disabled when the output-enable  $(\overline{OE})$  input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

TA	PACKAGE <sup>1</sup>	t	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
1000 / 0500	NanoStar WCSP (DSBGA) - YEA	Tape and reel	SN74LVC1G125YEAR	CM_
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G125DBVR	C25_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G125DCKR	CM_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

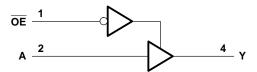
INP	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

NanoStar is a trademark of Texas Instruments.

DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### logic diagram (positive logic)

SCES223F - APRIL 1999 - REVISED JULY 2001



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	
(see Note 1)	0.5 V to 6.5 V
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	
DCK package	252°C/W
YEA package	
Storage temperature range, T <sub>Stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of  $V_{\hbox{\scriptsize CC}}$  is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Vac	Supply voltage	Operating	1.65	5.5	V
VCC	Supply vollage	Data retention only	1.5		l v
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
V	High lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	riigii-ieveriiiput voitage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		ď
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
٧/	Low level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
$V_{IL}$	High-level input voltage  Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	ľ
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
loh	High-level output current	V <sub>CC</sub> = 3 V		-16	mA
		VCC = 3 V		-24	
	High-level input voltage  Low-level input voltage  Input voltage Output voltage  High-level output current  Low-level output current	V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
loL	Low-level output current	Vac - 3 V		16	mA
		VCC = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
.,	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			
VOH    IOH = -100 μA   1.65 V to 5.5 V   VCC-0.1     IOH = -4 mA   1.65 V to 5.5 V   VCC-0.1     IOH = -8 mA   2.3 V   1.9     IOH = -16 mA   3 V   2.3     IOH = -32 mA   4.5 V   3.8     IOL = 100 μA   1.65 V to 5.5 V   0.0     IOL = 4 mA   2.3 V   0.0     IOL = 8 mA   2.3 V   0.0     IOL = 16 mA   3 V   0.0     IOL = 16 mA   3 V   0.0     IOL = 24 mA   4.5 V   0.0     IOL = 32 mA   3 V   0.0     IOL = 32 mA   4.5 V   0.0     IOL = 32 mA   4.5 V   0.0     IOL = 32 mA   3.6 V   0.0     IOZ   VO = 0 to 5.5 V   3.6 V     IOZ   VO = 0 to 5.5 V   0.0     IOC   One input at VCC - 0.6 V   Other inputs at VCC or GND   3 V to 5.5 V     Solution   Solution		V				
	I <sub>OH</sub> = -24 mA	3 V	2.3			
	I <sub>OH</sub> = -32 mA	4.5 V	3.8		0.1 0.45 0.3 0.4 0.55 0.55 ±10 10 10	
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.45	
VOL	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.3	.,
	I <sub>OL</sub> = 16 mA	2.1/			0.4	V
	I <sub>OL</sub> = 24 mA	$ \begin{array}{c ccccc}  & 1.65  \text{V} & 1.2 \\  & 2.3  \text{V} & 1.9 \\  & & & & & \\  & & & & & \\  & & & & & $				
	I <sub>OL</sub> = 32 mA	4.5 V			0.1 0.45 0.3 0.4 0.55 0.55 ±5 ±10 10	
I <sub>I</sub> A or OE inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0			±10	μΑ
loz	$V_0 = 0 \text{ to } 5.5 \text{ V}$	3.6 V			10	μΑ
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
ΔICC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V		4		pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

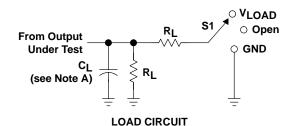
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		UNIT						
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	А	Υ	2.8	8	1.2	5.5	1	4.5	1	4	ns
t <sub>en</sub>	ŌĒ	Υ	3.3	9.4	1.5	6.6	1	5.3	1	5	ns
t <sub>dis</sub>	ŌĒ	Y	1.3	9.2	1	5	1	5	1	4.2	ns

#### operating characteristics, T<sub>A</sub> = 25°C

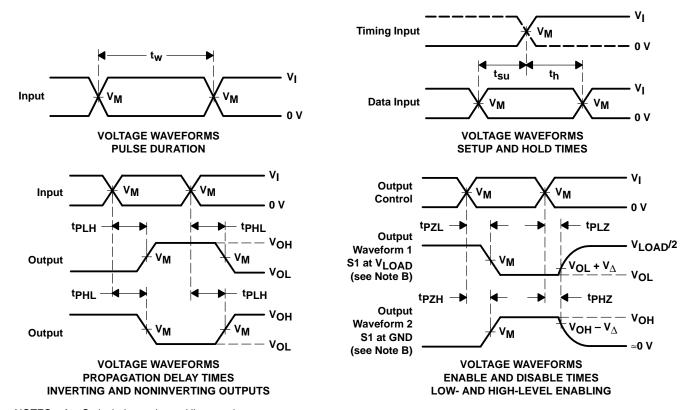
I	PARAMETER		TEST	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
			CONDITIONS	TYP	TYP	TYP	TYP	ONIT	
1	C1	Power dissipation	Outputs enabled	f = 10 MHz	18	18	19	21	ρF
	Cpd	capacitance	Outputs disabled	1 = 10 MHZ	2	2	2	4	pΓ





TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INI	PUTS	.,	.,		-	.,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	Vcc	≤2.5 ns	V <sub>CC</sub> /2	2×VCC	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\Omega}$  = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# DBV OR DCK PACKAGE (TOP VIEW) OE 1 5 VCC A 2 GND 3 4 Y YEA PACKAGE (BOTTOM VIEW) GND 03 40 Y A 02 OE 01 50 VCC

#### description

This single bus buffer gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G126 is a single line driver with a 3-state output. The output is disabled when the output-enable (OE) input is low.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>	-	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G126YEAR	CN
	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G126DBVR	C26_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G126DCKR	CN_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

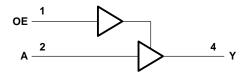
#### **FUNCTION TABLE**

INPU	JTS	OUTPUT
OE	Α	Y
Н	Н	Н
Н	L	L
L	Χ	Z

NanoStar is a trademark of Texas Instruments.

<sup>&</sup>lt;sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$\cdot$ . $-0.5$ V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA package	
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vaa	Supply voltage	Operating	1.65	5.5	V	
VCC	Supply vollage	Data retention only	1.5		l v	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
\/	High lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	riigii-ieveriiiput voitage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		ď	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
٧/	Low level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
$V_{IL}$	High-level input voltage  Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		8.0	ľ	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
٧ <sub>I</sub>	Input voltage		0	5.5	V	
٧o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
		V <sub>CC</sub> = 2.3 V		-8		
loh	High-level output current	V <sub>CC</sub> = 3 V		-16	mA	
	H High-level input voltage  Low-level input voltage  Input voltage Output voltage  H High-level output current  Low-level output current	VCC = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 3 V		16	mA	
		VCC = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYPT MAX	UNIT
	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1		
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2		
VOL  VOL  II A or OE inputs  Ioff  IOZ  ICC  ΔICC	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V
	$I_{OH} = -16 \text{ mA}$	0.14	2.4		V
	$I_{OH} = -24 \text{ mA}$	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V		0.1	0.45
VOL  II A or OE inputs  I off IOZ ICC	I <sub>OL</sub> = 4 mA	1.65 V		0.45	
	I <sub>OL</sub> = 8 mA	2.3 V		0.3	
	I <sub>OL</sub> = 16 mA	2.1/		0.4	v
	I <sub>OL</sub> = 24 mA	3 V			
	I <sub>OL</sub> = 32 mA	4.5 V		0.55	
I <sub>I</sub> A or OE inputs	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V		±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0		±10	μΑ
loz	$V_0 = 0 \text{ to } 5.5 \text{ V}$	3.6 V		10	μΑ
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10	μА
ΔlCC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V		4	pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

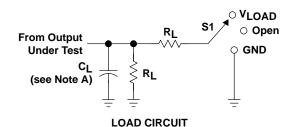
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(1141 01)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	2.6	8	1.1	5.5	1	4.5	1	4	ns
t <sub>en</sub>	OE	Y	2.8	9.4	1.3	6.6	1.2	5.3	1	5	ns
<sup>t</sup> dis	OE	Υ	1.6	9.8	1	5.5	1	5.5	1	4.2	ns

#### operating characteristics, $T_A = 25^{\circ}C$

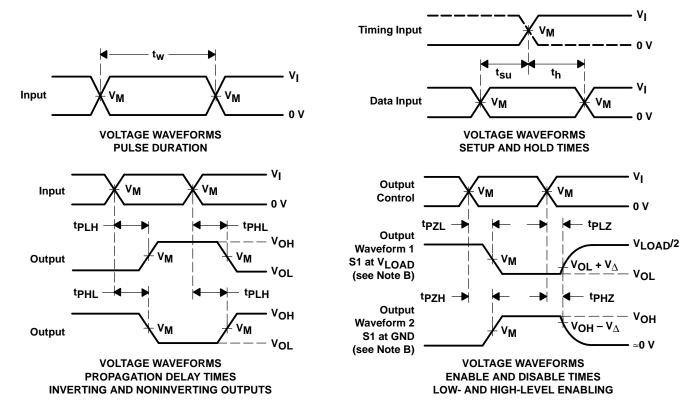
PARAMETER			TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
FARAMETER		TYP		TYP	TYP	TYP			
C <sub>pd</sub>	Power dissipation capacitance	Outputs enabled	f = 10 MHz	19	19	19	21	pF	
		Outputs disabled		2	2	3	4		





TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INPUTS		\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \	V	0	<b>D</b> .	.,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$V_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



SCES305B - JANUARY 2001 - REVISED JULY 2001

- Available in Texas Instruments' NanoStar™
   Package
- Supports 5-V V<sub>CC</sub> Operation
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DBV OR DCK PACKAGE (TOP VIEW) OE 1 5 VCC A 2 GND 3 4 Y YEA PACKAGE (BOTTOM VIEW) GND 3 40 Y A 2 OE 1 50 VCC

## description

This single buffer/driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G240 is a single line driver with a 3-state output. The output is disabled when the output-enable  $(\overline{OE})$  input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### **ORDERING INFORMATION**

TA	PACKAGE	t	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
1000 / 0500	NanoStar WCSP (DSBGA) – YEA	Tape and reel	SN74LVC1G240YEAR	CK_
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74LVC1G240DBVR	C40_
	SOP (SC-70) – DCK	Tape and reel	SN74LVC1G240DCKR	CK_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

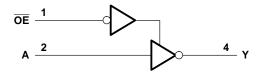
INPU	JTS	OUTPUT
OE	Α	Y
L	Н	L
L	L	Н
Н	Χ	Z

NanoStar is a trademark of Texas Instruments.

<sup>&</sup>lt;sup>‡</sup> DCK/DBV: The actual top-side marking has one additional character that designates the assembly/test site. YEA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.

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## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, V <sub>0</sub>	
	9
(see Note 1)	
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, IO	
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DBV package	
DCK package	252°C/W
YEA package	
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
Vaa	Supply voltage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
\/	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	7IH Tilgii-leveriliput voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		ď	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
٧/	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
V <sub>IL</sub> Lo	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		8.0	ľ	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
٧ <sub>I</sub>	Input voltage		0	5.5	V	
٧o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
		V <sub>CC</sub> = 2.3 V		-8	mA	
loh	High-level output current	V <sub>CC</sub> = 3 V		-16		
		VCC = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 3 V		16	mA	
		VCC = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

F	PARAMETER	TEST CONDITIONS	Vcc	MIN	TYP <sup>†</sup>	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2					
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V		
VOH	l	$I_{OH} = -16 \text{ mA}$	0.1/	2.4			V	
	I <sub>OH</sub> = -24 mA	3 V	2.3					
	I <sub>OH</sub> = -32 mA	4.5 V	3.8					
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
l ,,		I <sub>OL</sub> = 8 mA	2.3 V			0.3	,	
VOL		I <sub>OL</sub> = 16 mA	0.1/	0.4		V		
		I <sub>OL</sub> = 24 mA	3 V			0.55		
	I <sub>OL</sub> = 32 mA	4.5 V			0.55			
IJ	A or OE inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>	-	$V_I$ or $V_O = 5.5 V$	0			±10	μΑ	
loz		V <sub>O</sub> = 0 to 5.5 V	3.6 V			10	μΑ	
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
ΔlCC	<del></del>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ	
Ci		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4		pF	

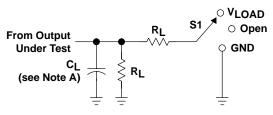
<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER FROM (INPUT)		TO (OUTPUT)	V <sub>CC</sub> =		UNIT						
(INPOT)	(INFOT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	Α	Υ	3	8	1.4	5.5	1.1	4.5	1	4	ns
t <sub>en</sub>	ŌĒ	Y	3.8	9.4	2.1	6.5	1.4	5.4	1.1	5.2	ns
<sup>t</sup> dis	ŌĒ	Υ	2.1	9.4	1	4.9	1.4	5.2	1	4.1	ns

## operating characteristics, $T_A = 25^{\circ}C$

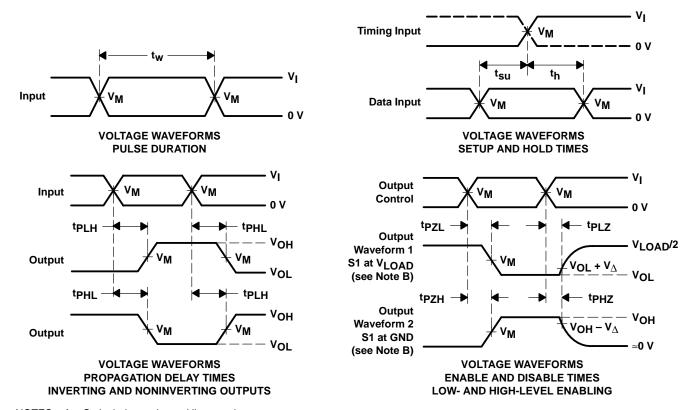
PARAMETER		TEST	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
	PARAMETER		CONDITIONS	TYP	TYP	TYP	TYP	UNIT
Const	Power dissipation	Outputs enabled	f = 10 MHz	17	17	18	20	~F
<sup>Cpd</sup> capacitance	Outputs disabled	1 = 10 MH2	1	1	1	3	p⊦	



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

**LOAD CIRCUIT** 

,,	INPUTS		.,			_	,,
Vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V ± 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

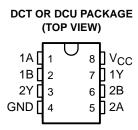


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- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation



## description

This dual 2-input positive-NAND gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G00 performs the Boolean function  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION

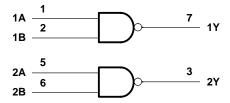
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC2G00DCTR	C00_
-40 C to 85 C	VSOP - DCU	Tape and reel	SN74LVC2G00DCUR	C00_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each gate)

	INPUTS A B		OUTPUT
			Υ
	Н	Н	L
	L	X	Н
	Х	L	Н

## logic diagram (positive logic)



<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or po	ower-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package .	
DCU package .	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of VCC is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
Voo	Supply voltage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
V		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$		
	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		] <sub>v</sub>
VIH	nigh-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		ď
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V/	Low level input valte as	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		0.8	\ \ \
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
	High-level output current	$V_{CC} = 2.3 \text{ V}$		-8	
loh		V = = 2 V		-16	mA
		VCC = 3 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V3V		16	mA
		VCC = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
VOH	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V
		I <sub>OH</sub> = -24 mA	3 V	2.3			
		I <sub>OH</sub> = -32 mA	4.5 V	3.8			
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
<b>.</b> ,		I <sub>OL</sub> = 8 mA	2.3 V			0.3	
VOL		I <sub>OL</sub> = 16 mA	3 V		0.4		V
		I <sub>OL</sub> = 24 mA				0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
Ц	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
loff		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μΑ
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		•	10	μΑ
ΔICC		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V				pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

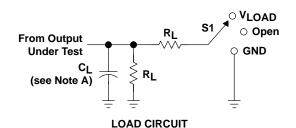
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Y									ns

## operating characteristics, T<sub>A</sub> = 25°C

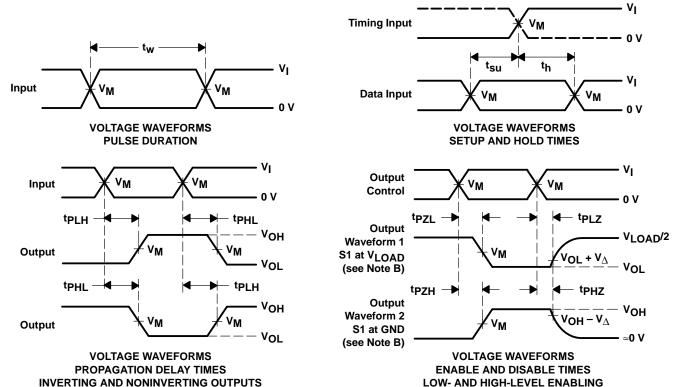
ĺ	PARAMETER		PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
			TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII
I	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
<sup>t</sup> PLH <sup>/t</sup> PHL	Open
<sup>t</sup> PLZ <sup>/t</sup> PZL	V <sub>LOAD</sub>
<sup>t</sup> PHZ <sup>/t</sup> PZH	GND

.,	INPUTS		.,	.,		_	.,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



## Supports 5-V V<sub>CC</sub> Operation

- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation



## description

This dual 2-input positive-NOR gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G02 performs the Boolean function  $Y = \overline{A + B}$  or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC2G02DCTR	C02_
-40 C to 65 C	VSOP – DCU	Tape and reel	SN74LVC2G02DCUR	C02_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each gate)

INP	JTS	OUTPUT
Α	В	Υ
Н	Х	L
Χ	Н	L
L	L	Н

## logic diagram (positive logic)

$$\begin{array}{c|c}
1A & \frac{1}{2} & & 7 \\
1B & \hline
\end{array}$$

$$\begin{array}{c|c}
2A & \frac{5}{6} & & 3 \\
2B & \hline
\end{array}$$

$$\begin{array}{c|c}
3 & 2Y \\
\end{array}$$

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of VCC is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/	Cupply valtage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		]	
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
V	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	nigii-ievei iriput voitage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		]	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		1	
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
\/	Low level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	] `	
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$		
٧ <sub>I</sub>	Input voltage	-	0	5.5	V	
٧o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
	High-level output current	V <sub>CC</sub> = 2.3 V		-8	1	
loh		V 2V		-16	mA	
		VCC = 3 V		-24	1	
		V <sub>CC</sub> = 4.5 V		-32	1	
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8	1	
$I_{OL}$	Low-level output current	V 2V		16	mA	
		V <sub>CC</sub> = 3 V		24	1	
		V <sub>CC</sub> = 4.5 V		32	1	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	10		ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5	1	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/ - · ·		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		I <sub>OH</sub> = -24 mA	3 V	2.3				
		I <sub>OH</sub> = -32 mA	4.5 V	3.8			1	
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
l ,,		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V	
VOL		I <sub>OL</sub> = 16 mA	2.1/			0.4	·	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
lį	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μΑ	
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
ΔlCC		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ	
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V				pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

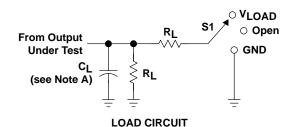
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V	
	(IIII O1)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Υ									ns

## operating characteristics, T<sub>A</sub> = 25°C

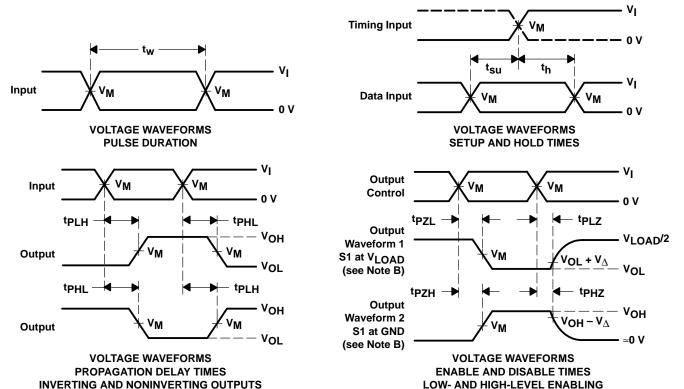
ſ		PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	VCC = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		FARAIVIETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
I	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF	

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	V <sub>LOAD</sub>
tPHZ/tPZH	GND

.,	INF	PUTS	.,				.,
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



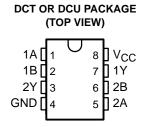
NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation



## description

This dual 2-input positive-AND gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G08 performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### **ORDERING INFORMATION**

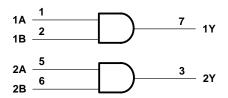
TA	PACK	AGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡	
-40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC2G08DCTR	C08_	
-40 C to 65 C	VSOP - DCU	Tape and reel	SN74LVC2G08DCUR	C08_	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each gate)

	INP	UTS	OUTPUT
	Α	В	Υ
I	Н	Н	Н
l	L	X	L
l	Χ	L	L

## logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or p	ower-off state, V <sub>O</sub>
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>sto</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of VCC is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cupalyyeltogo	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		l v
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
\ <i>/</i> .	Lligh lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		l <sup>v</sup>
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
.,	Lavo lava Canada adha na	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage	•	0	5.5	V
٧o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
ЮН	High-level output current			-16	mA
	$V_{CC} = 2.3 \text{ V}$ $V_{CC} = 3 \text{ V}$		-24		
		V <sub>CC</sub> = 4.5 V	-4 -8 -16	-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current			16	mA
		VCC = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		$V_{CC} = 5 V \pm 0.5 V$		5	
TA	Operating free-air temperature	<u> </u>	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT	
		I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/ - · ·		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		I <sub>OH</sub> = -24 mA	3 V	2.3				
		I <sub>OH</sub> = -32 mA	4.5 V	3.8			1	
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
l ,,		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V	
VOL		I <sub>OL</sub> = 16 mA	2.1/			0.4	·	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
lį	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μΑ	
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
ΔlCC		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ	
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V				pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

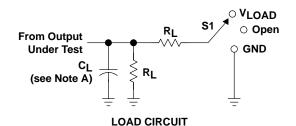
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(INFOT)	(0011 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Y									ns

## operating characteristics, T<sub>A</sub> = 25°C

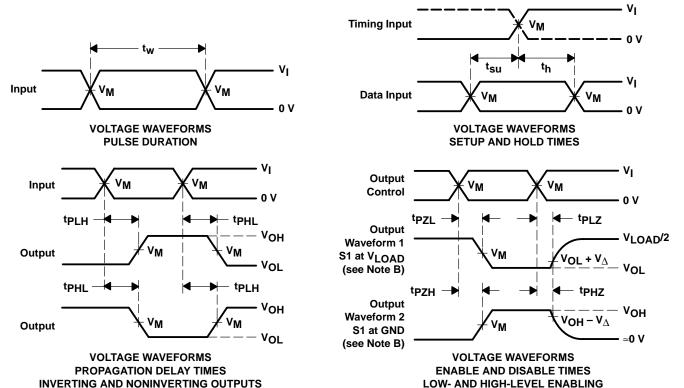
PARAMETER		DADAMETED	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		FARAMETER	TEST CONDITIONS	TYP	TYP TYP TYP		TYP	UNIT	
	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF	

## PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INPUTS		.,	.,		_	.,
Vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation



## description

This dual 2-input positive-OR gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G32 performs the Boolean function Y = A + B or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## **ORDERING INFORMATION**

TA	PACK	AGE <sup>†</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC2G32DCTR	C32_
	VSOP – DCU	Tape and reel	SN74LVC2G32DCUR	C32_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each gate)

INP	JTS	ОИТРИТ
Α	В	Y
Н	Х	Н
Х	Н	Н
L	L	L

## logic diagram (positive logic)

$$\begin{array}{c|c}
1A & \frac{1}{2} & 7 \\
1B & \hline
\end{array}$$

$$\begin{array}{c|c}
2A & \frac{5}{6} \\
2B & \hline
\end{array}$$

$$\begin{array}{c|c}
3 & 2Y \\
\end{array}$$

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, V <sub>O</sub> (see Notes 1 and 2)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of VCC is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/	Cupply valtage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		]	
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
V	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	nigii-ievei iriput voitage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2			
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		1	
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$		
\/	Low level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
VIL	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	] `	
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	1	
٧ <sub>I</sub>	Input voltage	-	0	5.5	V	
٧o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
	High-level output current	V <sub>CC</sub> = 2.3 V		-8	1	
loh		V 2V		-16	mA	
		VCC = 3 V		-24	1	
		V <sub>CC</sub> = 4.5 V		-32	1	
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8	1	
$I_{OL}$	Low-level output current	V 2V		16	mA	
		V <sub>CC</sub> = 3 V		24	1	
		V <sub>CC</sub> = 4.5 V		32	1	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5	1	
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAF	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT	
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/ - · ·		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
VOH		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		I <sub>OH</sub> = -24 mA	3 V	2.3				
		I <sub>OH</sub> = -32 mA	4.5 V	3.8				
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V	
VOL		I <sub>OL</sub> = 16 mA	2.1/			0.4	V	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
IJ	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μΑ	
Icc	•	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
∆lcc		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ	
Ci		$V_I = V_{CC}$ or GND	3.3 V				pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.

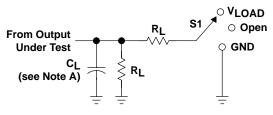
## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> =		V <sub>CC</sub> =		ν <sub>CC</sub> =		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Υ									ns

## operating characteristics, T<sub>A</sub> = 25°C

ſ	PARAMETER		PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
			TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

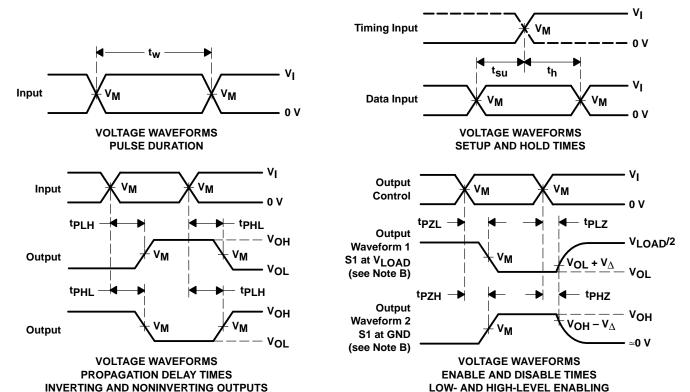
## PARAMETER MEASUREMENT INFORMATION



TEST	<b>S</b> 1
tPLH/tPHL	Open
tPLZ/tPZL	V <sub>LOAD</sub>
tPHZ/tPZH	GND

LOAD CIRCUIT

.,	INPUTS		.,	.,		_	.,
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

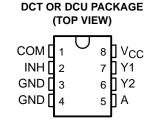
Figure 1. Load Circuit and Voltage Waveforms



## SN74LVC2G53 DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER

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- 1.65-V to 5.5-V V<sub>CC</sub> Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed Typically 0.5 ns (V<sub>CC</sub> = 3 V, C<sub>L</sub> = 50 pF)
- Low On-State Impedance Typically  $\approx$ 6.5  $\Omega$  (V<sub>CC</sub> = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



## description

This dual analog multiplexer/demultiplexer is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G53 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

### ORDERING INFORMATION

TA	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP - DCT	Tape and reel	SN74LVC2G53DCTR	C53_
	VSOP - DCU	Tape and reel	SN74LVC2G53DCUR	C53_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

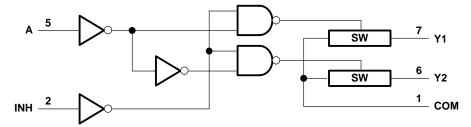
CONT	-	ON CHANNEL			
INH	Α	CHANNEL			
L	L	Y1			
L	Н	Y2			
Н	Χ	None			



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

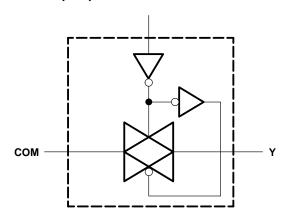
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## logic diagram (positive logic)



NOTE A: For simplicity, the test conditions shown in Figures 1 through 4 and 6 through 10 are for the demultiplexer configuration. Signals may be passed from COM to Y1 (Y2) or from Y1 (Y2) to COM.

## simplified schematic, each switch (SW)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub> (see Note 1)	
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	
Switch I/O voltage range, V <sub>I/O</sub> (see Notes 1, 2, and 3)	0.5 V to V <sub>CC</sub> + 0.5 V
Control input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
I/O port diode current, $I_{IOK}$ ( $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$ )	±50 mA
On-state switch current, $I_T (V_{I/O} = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
  - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 3. This value is limited to 5.5 V maximum.
  - 4. The package thermal impedance is calculated in accordance with JESD 51-7.



## SN74LVC2G53 DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER

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## recommended operating conditions (see Note 5)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	5.5	V	
V <sub>I/O</sub>	I/O port voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V to 1.95 V	V <sub>CC</sub> × 0.65			
\/		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V <sub>CC</sub> × 0.7		V	
VIH High-level input voltage, control input	V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V		
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7		1 1	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$V_{CC} \times 0.35$		
\/	Low-level input voltage, control input	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$	V	
VIL		V <sub>CC</sub> = 3 V to 3.6 V		$V_{CC} \times 0.3$		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$		
VI	Control input voltage		0	5.5	V	
		V <sub>CC</sub> = 1.65 V to 1.95 V		20		
A+/A.,	lanut transition via Mall time	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		20	20/1	
Δt/Δv	Input transition rise/fall time	V <sub>CC</sub> = 3 V to 3.6 V		10	ns/V	
		V <sub>CC</sub> = 4.5 V to 5.5 V		10		
TA	Operating free-air temperature		-40	85	°C	

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDIT	VCC	MIN TYPT	MAX	UNIT	
				$I_S = 4 \text{ mA}$	1.65 V	13	30	
_	On-state switch resistance		$V_I = V_{CC}$ or GND,	$I_S = 8 \text{ mA}$	2.3 V	10	20	Ω
r <sub>on</sub>	On-State Switch resistance		VINH = VIL (see Figures 1 and 2)	I <sub>S</sub> = 24 mA	3 V	8.5	17	52
			,	I <sub>S</sub> = 32 mA	4.5 V	6.5	13	
			$I_S = 4 \text{ mA}$	1.65 V	86.5	120		
<b>.</b>	Book on state registance		$V_I = V_{CC}$ to GND,	$I_S = 8 \text{ mA}$	2.3 V	23	30	Ω
ron(p)	Peak on-state resistance		VINH = VIL (see Figures 1 and 2)	I <sub>S</sub> = 24 mA	3 V	13	20	52
			(*** )*********************************	$I_S = 32 \text{ mA}$	4.5 V	8	15	
			$I_S = 4 \text{ mA}$	1.65 V		7		
	$\Delta r_{\text{ON}}$ Difference of on-state resistance between switches		$V_I = V_{CC}$ to GND,	I <sub>S</sub> = 8 mA	2.3 V			
on b			V <sub>C</sub> = V <sub>IH</sub> (see Figures 1 and 2)	I <sub>S</sub> = 24 mA	3 V		3	Ω
			(*** )*********************************	I <sub>S</sub> = 32 mA	4.5 V		2	
	Off-state switch leakage current		$V_I = V_{CC}$ and $V_O = GND$ or $V_I = GND$ and $V_O = V_{CC}$ , $V_{INH} = V_{IH}$ (see Figure 3)		5.5 V		±1	μΑ
IS(off)							±0.1†	
			V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>INH</sub> = V <sub>IL</sub> , V <sub>O</sub> = Open (see Figure 4)		5.5 V		±1	μΑ
<sup>I</sup> S(on)	On-state switch leakage current						±0.1 <sup>†</sup>	
					5.5.7		±1	
l <sub>l</sub>	Control input current		$V_C = V_{CC}$ or GND		5.5 V		±0.1 <sup>†</sup>	μΑ
loo	Supply current		Vo - Voo or GND		5.5 V		10	μΑ
Icc	C Supply current		$V_C = V_{CC}$ or GND		3.5 V		1 <sup>†</sup>	μΑ
∆lcc	Supply-current change		$V_C = V_{CC} - 0.6 \text{ V}$		5.5 V		500	μΑ
C <sub>ic</sub>	Control input capacitance				5 V	3.5		pF
C	Switch input/output capacitance	Υ			5 V	6.5		
C <sub>io(off)</sub>	Switch input/output capacitance	COM				10		pF
C <sub>io(on)</sub>	Switch input/output capacitance		5 V	19.5		pF		
† T <sub>A</sub> = 25°C								

 $<sup>^{\</sup>dagger}T_{A} = 25^{\circ}C$ 

## switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER	FROM TO (INPUT) (OUTPUT)			V <sub>CC</sub> = 1.8 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT	
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub> ‡	COM or Y	Y or COM		2		1.2		0.8		0.6	ns
t <sub>en</sub> §	INH	COM or Y	3.3	9	2.5	6.1	2.2	5.4	1.8	4.5	no
t <sub>dis</sub> ¶		CONTOL	3.2	10.9	2.3	8.3	2.3	8.1	1.6	8	ns
t <sub>en</sub> §	Α	COMor V	2.9	10.3	2.1	7.2	1.9	5.8	1.3	5.4	no
t <sub>dis</sub> ¶	^	COM or Y	2.1	9.4	1.4	7.9	1.1	7.2	1	5	ns

<sup>‡</sup> tPLH and tPHL are the same as tpd. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).



 $<sup>\</sup>$  tp\_ZL and tpZH are the same as ten.  $\$  tpLZ and tpHZ are the same as tdis.

## analog switch characteristics, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	vcc	TYP	UNIT
				1.65 V	35	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	120	
			f <sub>in</sub> = sine wave (see Figure 6)	3 V	190	
Frequency response†	COM or Y	Y or COM	(000 / 1940 0)	4.5 V	215	MHz
(switch on)	CONTOLL	1 OI COIVI		1.65 V	>300	IVITIZ
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	>300	
			f <sub>in</sub> = sine wave (see Figure 6)	3 V	>300	
			, ,	4.5 V	>300	
				1.65 V	-58	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$ $f_{in} = 1 \text{ MHz (sine wave)}$	2.3 V	-58	
			(see Figure 7)	3 V	-58	
Crosstalk <sup>‡</sup>	COM or Y	Y or COM	, ,	4.5 V	-58	dB
(between switches)	OOM OF 1	1 01 00101		1.65 V	-42	ив
			$C_L = 5 \text{ pF, } R_L = 50 \Omega,$ $f_{\text{in}} = 1 \text{ MHz (sine wave)}$ (see Figure 7)	2.3 V	-42	
				3 V	-42	
			, ,	4.5 V	-42	
	INH	COM or Y	$C_L$ = 50 pF, $R_L$ = 600 $\Omega$ , $f_{in}$ = 1 MHz (square wave) (see Figure 8)	1.65 V	35	mV
Crosstalk				2.3 V	50	
(control input to signal output)				3 V	70	
				4.5 V	100	
		Y or COM	$C_L = 50 \text{ pF}, R_L = 600 \Omega,$ $f_{in} = 1 \text{ MHz (sine wave)}$ (see Figure 9)	1.65 V	-60	dB
				2.3 V	-60	
				3 V	-60	
Feed-through attenuation <sup>‡</sup>	COM or Y		, , ,	4.5 V	-60	
(switch off)	OOM OF 1	1 01 00101		1.65 V	-50	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$ $f_{in} = 1 \text{ MHz (sine wave)}$	2.3 V	-50	
			(see Figure 9)	3 V	-50	
				4.5 V	-50	
				1.65 V	0.1	
			$C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 1 kHz (sine wave)	2.3 V	0.025	
			(see Figure 10)	3 V	0.015	
Sine-wave distortion	COM or Y	Y or COM		4.5 V	0.01	%
C Have dictorner	333. 1	1 0. 00		1.65 V	0.15	,,
			$C_L$ = 50 pF, $R_L$ = 10 kΩ, $f_{in}$ = 10 kHz (sine wave)	2.3 V	0.025	
		Tin =	(see Figure 10)	3 V	0.015	
			, , ,	4.5 V	0.01	

<sup>†</sup> Adjust f<sub>in</sub> voltage to obtain 0 dBm at output. Increase f<sub>in</sub> frequency until dB meter reads –3 dB. ‡ Adjust f<sub>in</sub> voltage to obtain 0 dBm at input.

## operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 10 MHz	9	10	10	12	pF



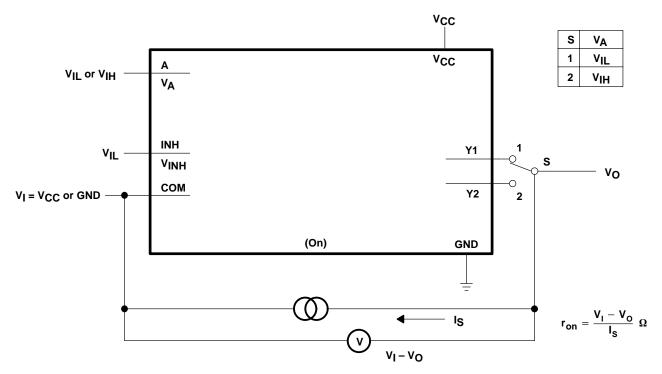


Figure 1. On-State Resistance Test Circuit

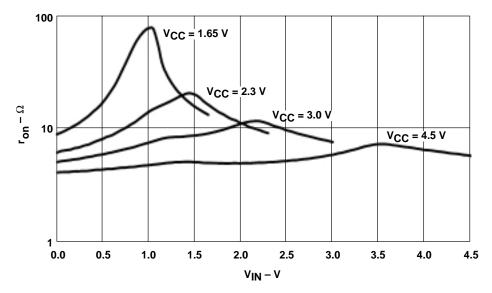


Figure 2. Typical  $r_{on}$  as a Function of Input Voltage (V<sub>I</sub>) for V<sub>I</sub> = 0 to V<sub>CC</sub>

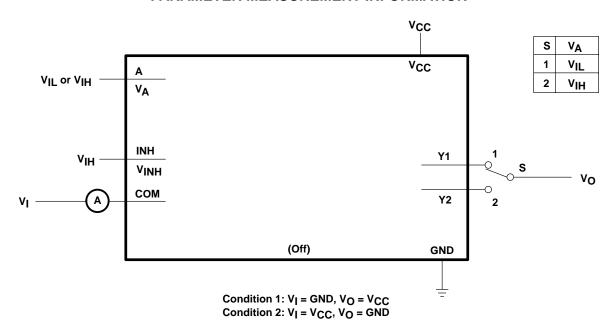


Figure 3. Off-State Switch Leakage-Current Test Circuit

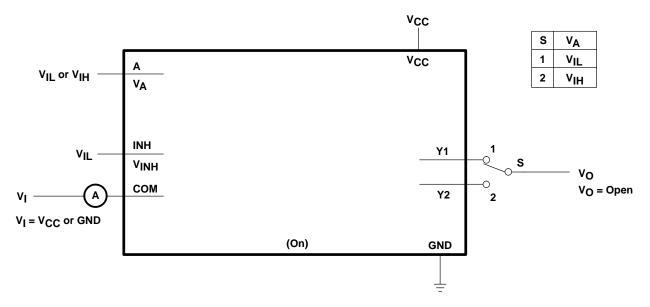
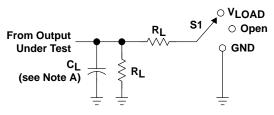


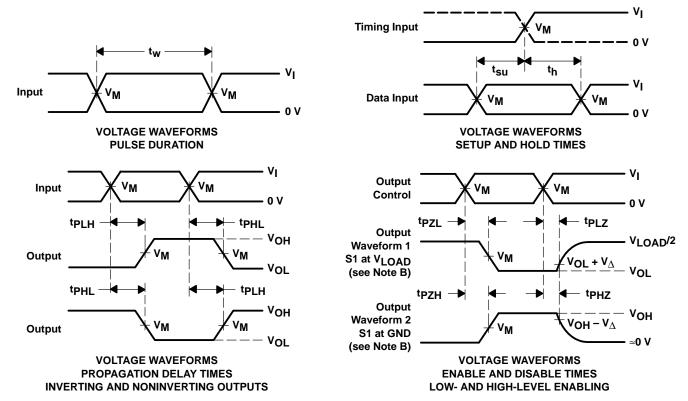
Figure 4. On-State Switch Leakage-Current Test Circuit



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

**LOAD CIRCUIT** 

W	INPUTS		Vaa Vi oan		0	ъ.	V
vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×VCC	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms



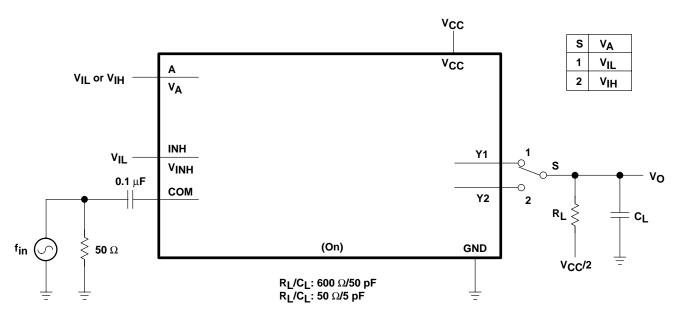


Figure 6. Frequency Response (Switch On)

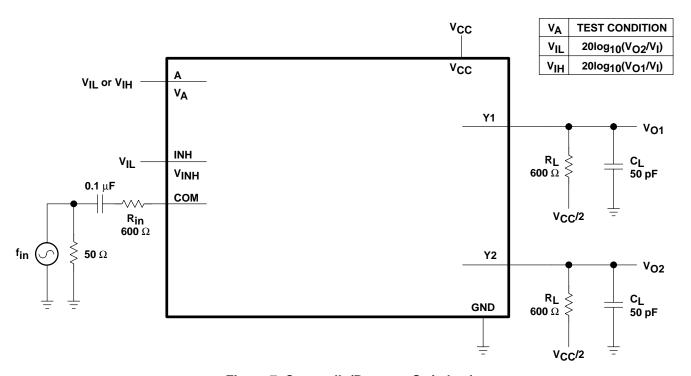


Figure 7. Crosstalk (Between Switches)

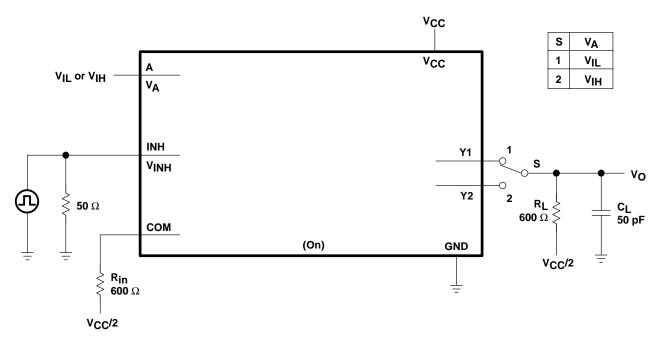


Figure 8. Crosstalk (Control Input, Switch Output)

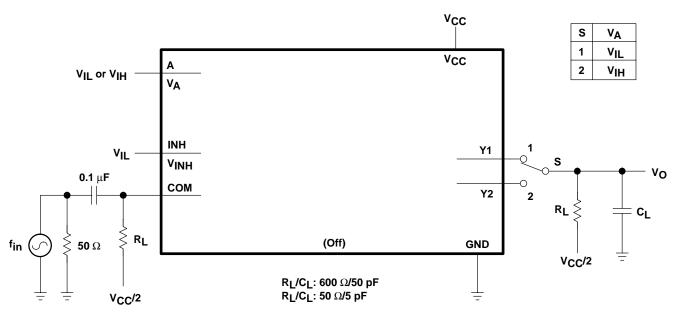


Figure 9. Feed-Through (Switch Off)

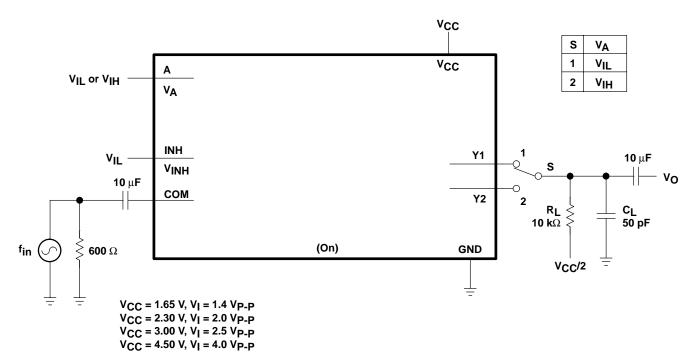


Figure 10. Sine-Wave Distortion

#### SN74LVC2G66 DUAL BILATERAL ANALOG SWITCH

SCES325B - JULY 2001 - REVISED SEPTEMBER 2001

- 1.65-V to 5.5-V V<sub>CC</sub> Operation
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed Typically 0.5 ns (V<sub>CC</sub> = 3 V, C<sub>L</sub> = 50 pF)
- Low On-State Impedance Typically  $\approx$ 6  $\Omega$  (V<sub>CC</sub> = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

# 1A 1 8 V<sub>CC</sub> 1B 2 7 1C 2C 3 6 2B GND 4 5 2A

#### description

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	TSSOP – DCT	Tape and reel	SN74LVC2G66DCTR	C66_
-40 C to 65 C	VSOP - DCU	Tape and reel	SN74LVC2G66DCUR	C66_

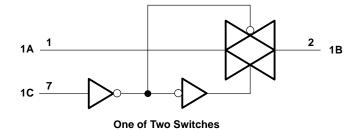
<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each section)

CONTROL INPUT (C)	SWITCH
L	Off
Н	On

<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

#### logic diagram, each switch (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub> (see Note 1)	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Notes 1 and 2)	
Switch I/O voltage range, V <sub>I/O</sub> (see Notes 1, 2, and 3)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Control input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
I/O port diode current, $I_{IOK}$ ( $V_{I/O} < 0$ or $V_{I/O} > V_{CC}$ )	±50 mA
On-state switch current, $I_T (V_{I/O} = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground unless otherwise specified.
  - 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  - 3. This value is limited to 5.5 V maximum.
  - 4. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 5)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	5.5	V	
V <sub>I/O</sub>	I/O port voltage		0	Vcc	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	V <sub>CC</sub> × 0.65			
\ <i>/.</i>	High level input valtage, control input	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V <sub>CC</sub> × 0.7		V	
VIH	High-level input voltage, control input	V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7		V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V <sub>CC</sub> × 0.7			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		$V_{CC} \times 0.35$		
١/	Low-level input voltage, control input	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$	V	
$V_{IL}$		V <sub>CC</sub> = 3 V to 3.6 V		$V_{CC} \times 0.3$	ľ	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		V <sub>CC</sub> ×0.3		
٧ <sub>I</sub>	Control input voltage		0	5.5	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		20		
A+/A>,	Input transition rise/fall time	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		20	no∆/	
Δt/Δν	Input transition rise/fall time	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		10	10 ns/V	
	V <sub>CC</sub> = 4.5 V to 5.5 V			10		
TA	Operating free-air temperature		-40	85	°C	

NOTE 5: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST COND	TEST CONDITIONS			TYP <sup>†</sup>	MAX	UNIT
			$I_S = 4 \text{ mA}$	1.65 V		12.5	30	
_	On-state switch resistance	$V_I = V_{CC}$ or GND,	$I_S = 8 \text{ mA}$	2.3 V		9	20	Ω
r <sub>on</sub>	Ton On-State Switch resistance	VC = VIH (see Figures 1 and 2)	$I_S = 24 \text{ mA}$	3 V		7.5	15	22
		,	$I_S = 32 \text{ mA}$	4.5 V		6	10	
			$I_S = 4 \text{ mA}$	1.65 V		85	120	
, , ,	Peak on-state resistance	$V_I = V_{CC}$ to GND,	$I_S = 8 \text{ mA}$	2.3 V		22	30	Ω
ron(p)	reak on-state resistance	VC = VIH (see Figures 1 and 2)	$I_S = 24 \text{ mA}$	3 V		12	20	52
		) ,	$I_S = 32 \text{ mA}$	4.5 V		7.5	15	
			$I_S = 4 \text{ mA}$	1.65 V			7	
Ar	Difference of on-state resistance between switches	$V_I = V_{CC}$ to GND,	$I_S = 8 \text{ mA}$	2.3 V			5	Ω
∆r <sub>on</sub>		VC = VIH (see Figures 1 and 2)	I <sub>S</sub> = 24 mA	3 V			3	
		, ,	I <sub>S</sub> = 32 mA	4.5 V			2	
		$V_I = V_{CC}$ and $V_O = GND$		> /			±1	
IS(off)	Off-state switch leakage current	$V_I = GND$ and $V_O = V_{CC}$ $V_C = V_{IL}$ (see Figure 3)	,	5.5 V			±0.1†	μΑ
IC(on)	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_C = V_{CC}$	√ <sub>IH</sub> , √ <sub>O</sub> = Open	5.5 V			±1	μΑ
IS(on)	On state switch leakage current	(see Figure 4)		5.5 V			±0.1 <sup>†</sup>	μΑ
l <sub>l</sub>	Control input current	V <sub>C</sub> = V <sub>CC</sub> or GND		5.5 V			±1	μΑ
'1	Common impar carronic	VC = VCC 61 6115		0.0 7			±0.1 <sup>†</sup>	μ.,
<sup>I</sup> CC	Supply current	$V_C = V_{CC}$ or GND		5.5 V		,	10	μΑ
						-	1 <sup>†</sup>	•
∆lcc	Supply-current change	$V_C = V_{CC} - 0.6 V$		5.5 V			500	μΑ
C <sub>ic</sub>	Control input capacitance					3.5		pF
C <sub>io(off)</sub>	Switch input/output capacitance			5 V		6		pF
C <sub>io(on)</sub>	Switch input/output capacitance			5 V		14		pF

<sup>†</sup> T<sub>A</sub> = 25°C

#### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 5)

PARAMETER FROM (INPUT)		TO (OUTPUT)	V <sub>CC</sub> =		UNIT						
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub> ‡	A or B	B or A		2		1.2		8.0		0.6	ns
t <sub>en</sub> §	E A A OF B	A or P	2.3	10	1.6	5.6	1.5	4.4	1.3	3.9	ns
t <sub>dis</sub> ¶		2.5	10.5	1.2	6.9	2	7.2	1.1	6.3	110	

<sup>‡</sup> tPLH and tPHL are the same as tpd. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).



 $<sup>\</sup>$  tp\_ZL and tpZH are the same as ten.  $\$  tpLZ and tpHZ are the same as tdis.

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#### analog switch characteristics, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	vcc	TYP	UNIT
				1.65 V	35	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	120	
			f <sub>in</sub> = sine wave (see Figure 6)	3 V	175	
Frequency response†	A or B	B or A	(555 : .ga. 5 5)	4.5 V	195	MHz
(switch on)	AUID	D OF A		1.65 V	>300	IVITZ
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	>300	
			f <sub>in</sub> = sine wave (see Figure 6)	3 V	>300	
			(**************************************	4.5 V	>300	
				1.65 V	-58	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	-58	
			f <sub>in</sub> = 1 MHz (sine wave) (see Figure 7)	3 V	-58	
Crosstalk <sup>‡</sup>	A = = D	D A	(555 : 19415 : 7	4.5 V	-58	4D
(between switches)	A or B	B or A		1.65 V	-42	dB
			$C_L = 5 \text{ pF, } R_L = 50 \Omega,$ $f_{\text{in}} = 1 \text{ MHz (sine wave)}$ (see Figure 7)	2.3 V	-42	
				3 V	-42	
		(coorigator)	4.5 V	-42		
	С	A or B	$C_L = 50 \text{ pF}, R_L = 600 \Omega,$ $f_{\text{in}} = 1 \text{ MHz} \text{ (square wave)}$ (see Figure 8)	1.65 V	35	mV
Crosstalk				2.3 V	50	
(control input to signal output)				3 V	70	
			(555 : 19415 5)	4.5 V	100	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	1.65 V	-58	dB
				2.3 V	-58	
			f <sub>in</sub> = 1 MHz (sine wave) (see Figure 9)	3 V	-58	
Feed-through attenuation <sup>‡</sup>	A D	D A	(GGG ) iguio G)	4.5 V	-58	
(switch off)	A or B	B or A		1.65 V	-42	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	-42	
			f <sub>in</sub> = 1 MHz (sine wave) (see Figure 9)	3 V	-42	
			(See Figure 5)	4.5 V	-42	
				1.65 V	0.1	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	2.3 V	0.025	
			f <sub>in</sub> = 1 kHz (sine wave) (see Figure 10)	3 V	0.015	
			(See Figure 10)	4.5 V	0.01	
Sine-wave distortion	A or B	B or A		1.65 V	0.15	%
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	2.3 V	0.025	
			f <sub>in</sub> = 10 kHz (sine wave) (see Figure 10)	3 V	0.015	
			(See Figure 10)	4.5 V	0.01	

<sup>†</sup> Adjust f<sub>in</sub> voltage to obtain 0 dBm at output. Increase f<sub>in</sub> frequency until dB meter reads –3 dB. ‡ Adjust f<sub>in</sub> voltage to obtain 0 dBm at input.

#### operating characteristics, $T_A = 25^{\circ}C$

DADAMETED		DADAMETED	PARAMETER TEST CONDITIONS V <sub>CC</sub> = 1.8 V V <sub>CC</sub> = 2.5 V		V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
	PARAMETER		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
С	pd	Power dissipation capacitance	f = 10 MHz	8	9	9.5	11	pF	



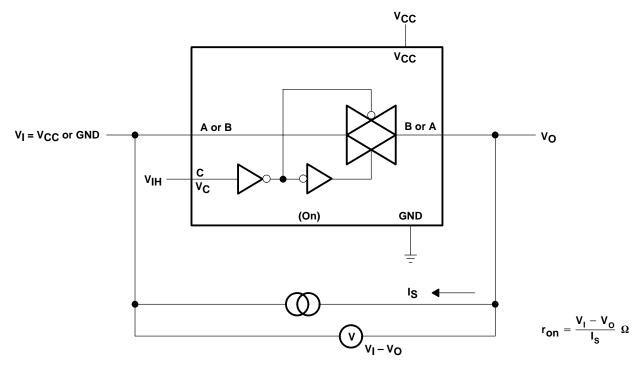


Figure 1. On-State Resistance Test Circuit

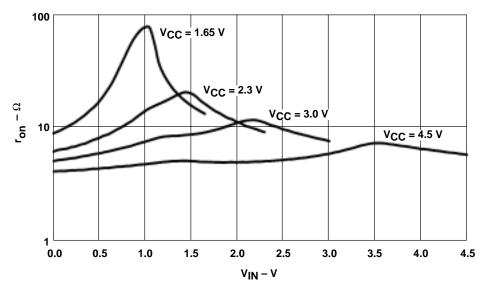


Figure 2. Typical  $r_{on}$  as a Function of Input Voltage (V<sub>I</sub>) for  $V_{I} = 0$  to  $V_{CC}$ 

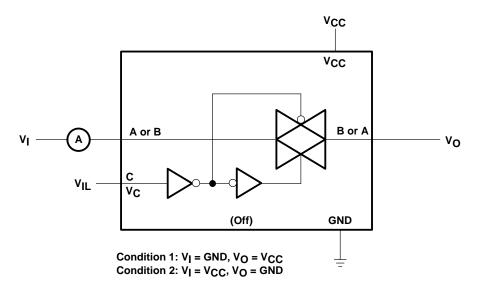


Figure 3. Off-State Switch Leakage-Current Test Circuit

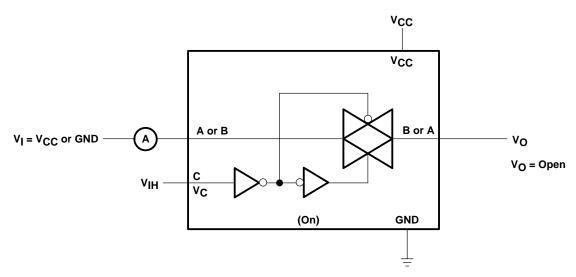
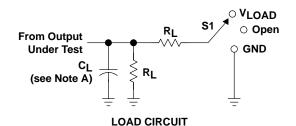
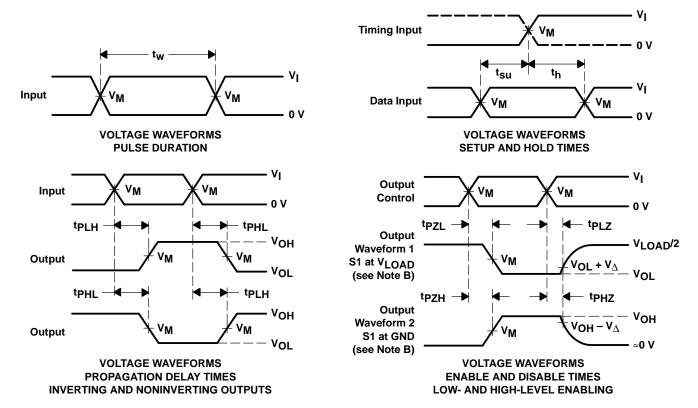


Figure 4. On-State Leakage-Current Test Circuit



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

INPUTS			V	0		\ \ \	
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	RL	$V_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms



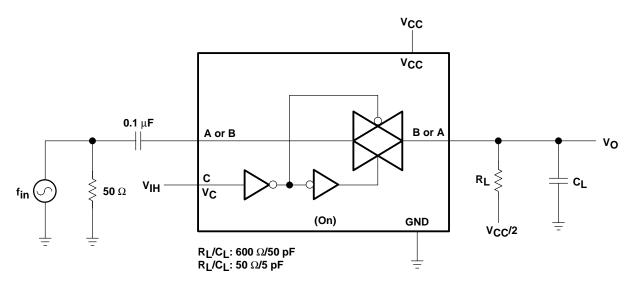


Figure 6. Frequency Response (Switch On)

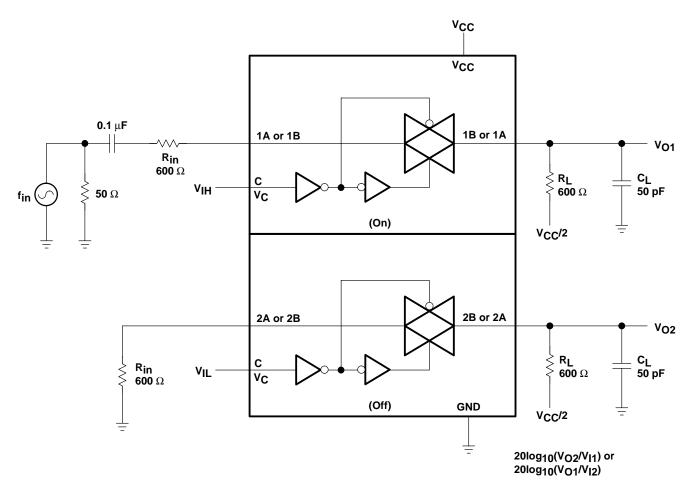


Figure 7. Crosstalk (Between Switches)



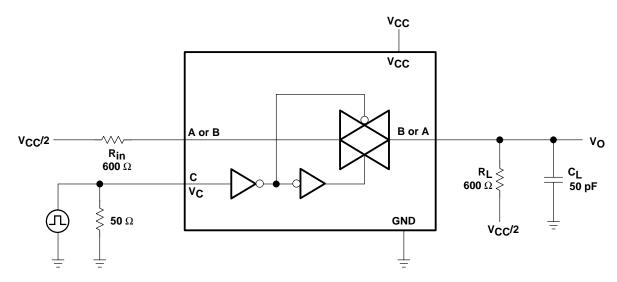


Figure 8. Crosstalk (Control Input, Switch Output)

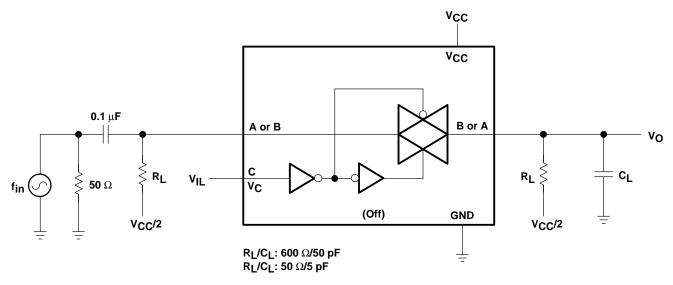


Figure 9. Feed-Through (Switch Off)

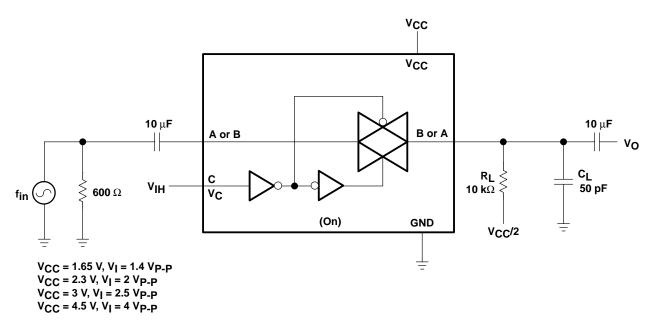
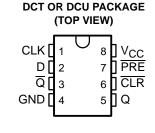


Figure 10. Sine-Wave Distortion

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- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

This single positive-edge-triggered D-type flip-flop is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

A low level at the preset (PRE) or clear (CLR) input sets or resets the outputs, regardless of the levels of the other inputs. When PRE and CLR are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
-40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC2G74DCTR	C74_
-40 C 10 65 C	VSOP – DCU	Tape and reel	SN74LVC2G74DCUR	C74_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

	INP	OUTI	PUTS		
PRE	CLR	CLK	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	Χ	L	Н
L	L	X	Χ	н§	н§
Н	Н	$\uparrow$	Н	Н	L
Н	Н	$\uparrow$	L	L	Н
Н	Н	L	Χ	$Q_0$	$\overline{Q}_0$

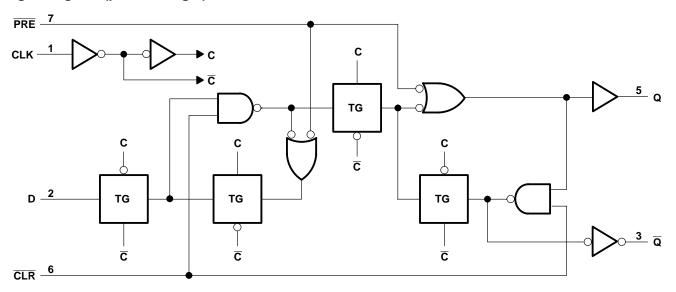
<sup>§</sup> This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



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#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/	Complexion	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
١/	High lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	nigh-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
١/	Low level input valtage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
$V_{IL}$	H High-level input voltage  Low-level input voltage  Input voltage Output voltage  High-level output current  Low-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	
٧ <sub>I</sub>	Input voltage	-	0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	
IOH	High-level output current	V 2V		-16	mA
		VCC = 3 V		-24	
	OH High-level output current	V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
$I_{OL}$	Low-level output current	V 3 V		16	mA
		V <sub>CC</sub> = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
TA	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
Maria		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
Vон		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V
		$I_{OH} = -24 \text{ mA}$	3 V	2.3			
		I <sub>OH</sub> = -32 mA	4.5 V	3.8			
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
\/		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V
VOL		I <sub>OL</sub> = 16 mA	3 V			0.4	V
		I <sub>OL</sub> = 24 mA				0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
II	Control inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
loff		$V_I$ or $V_O = 5.5 V$	0			±10	μΑ
Icc	C $V_I = 5.5 \text{ V or GND}, I_O = 0$		1.65 V to 5.5 V			10	μΑ
∆lcc		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V		5	·	pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		УСС = ± 0.		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
fclock			80		175		175		200	MHz	
	CLK	6.2		2.7		2.7		2			
ιW	t <sub>W</sub> Pulse duration	PRE or CLR low	6.2		2.7		2.7		2		ns
	Catura times In aform CLIVA	Data	2.9		1.7		1.3		1.1		no
t <sub>SU</sub> Setup time, before CLK↑	PRE or CLR inactive	1.9		1.4		1.2		1		ns	
th	Hold time, data after CLK↑	_	0		0.3		1.2	·	0.5		ns

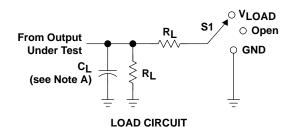
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		= V <sub>CC</sub>		UNIT
	(INPOT)	(INPOT) (OUTPOT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			80		175		175		200		MHz
	01.14	Q	4.8	13.4	2.2	7.1	2.2	5.9	1.4	4.1	
<sup>t</sup> pd	CLK	Q	6	14.4	3	7.7	2.6	6.2	1.6	4.4	ns
	PRE or CLR	Q or $\overline{Q}$	4.4	12.9	2.3	7	1.7	5.9	1.6	4.1	

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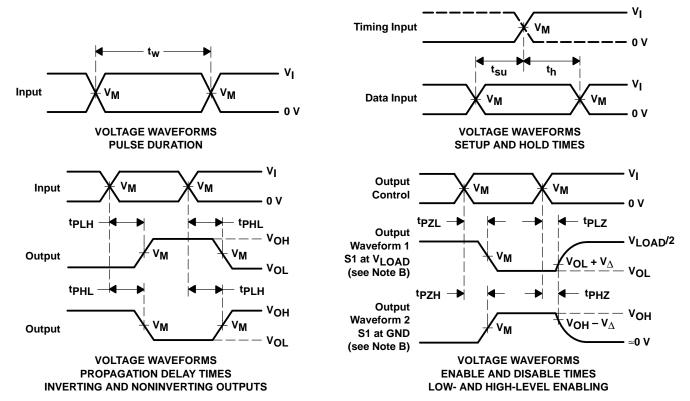
#### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
PARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNII	
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

.,	INF	PUTS	.,			_	.,
vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$v_{\scriptscriptstyle\Delta}$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V

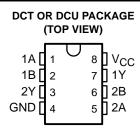


- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation



#### description

This dual 2-input exclusive -OR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G86 performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{AB} + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PAC	(AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	SOT - DCT	Tape and reel	SN74LVC2G86DCTR	C86_
-40 C 10 65 C	SOT - DCU	Tape and reel	SN74LVC2G86DCUR	C86_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## FUNCTION TABLE (each gate)

INP	JTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

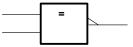
#### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

# 

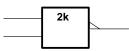
These are five equivalent exclusive-OR symbols valid for an SN74LVC2G86 gate in positive logic; negation may be shown at any two ports.

# LOGIC-IDENTITY ELEMENT



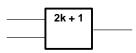
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

#### **EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

#### **ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# PRODUCT PREVIEW

#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/	Cumply voltage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only	1.5		]
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		
V	High lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		1 °
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$		1
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
\	Lava lava Camata adita na	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	1 ,,
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	1
٧ı	Input voltage	•	0	5.5	V
٧o	Output voltage		0	VCC	V
	V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> = 1.65 V		-4	
		V <sub>CC</sub> = 2.3 V		-8	1
ЮН	High-level output current	evel output current		-16	mA
		VCC = 3 V		-24	1
		V <sub>CC</sub> = 4.5 V		-32	1
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	1
loL	Low-level output current			16	mA
		VCC = 3 V		24	1
		V <sub>CC</sub> = 4.5 V		32	1
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
	•	V <sub>CC</sub> = 5 V ± 0.5 V		5	1
TA	Operating free-air temperature	•	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

otherwise noted)

# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless

PARAMETER	TEST CONDITIONS	vcc	MIN	TYP†	MAX	UNIT	
	I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
V	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
vОН	$I_{OH} = -16 \text{ mA}$	0.1/	2.4	-		V	
VOL  II A or B inputs  I off ICC	$I_{OH} = -24 \text{ mA}$	3 V	2.3				
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8				
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	0.45	
V	I <sub>OL</sub> = 8 mA	2.3 V			0.3 V		
VOL	I <sub>OL</sub> = 16 mA	2.1/	0.4		V		
	I <sub>OL</sub> = 24 mA	3 V		0.55			
	I <sub>OL</sub> = 32 mA	4.5 V		-	0.55		
I <sub>I</sub> A or B inpu	uts V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
l <sub>off</sub>	$V_I \text{ or } V_O = 5.5 \text{ V}$	0		-	±10	μΑ	
	$V_I = V_{CC}$ or GND, $I_O = 0$	1.65 V to 5.5 V			10	μΑ	
Δl <sub>CC</sub>	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V			500	μΑ	
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V				pF	

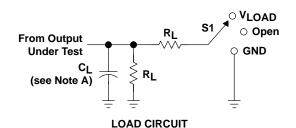
 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		UNIT						
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Y								·	ns

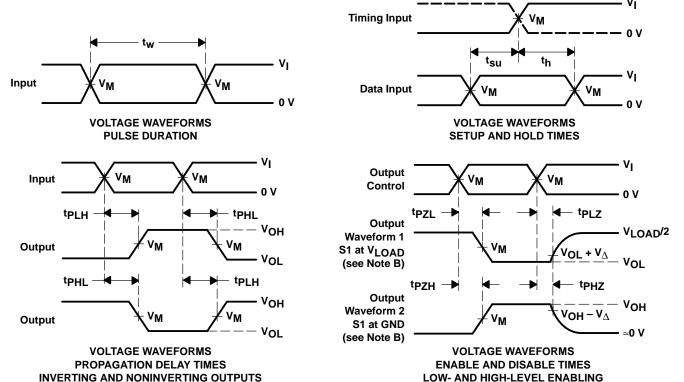
#### operating characteristics, T<sub>A</sub> = 25°C

ſ	PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	CC = 1.8 V V <sub>CC</sub> = 2.5 V		V <sub>CC</sub> = 5 V	UNIT
L			TEST CONDITIONS	TYP TYP		TYP	P TYP	
I	C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	V <sub>LOAD</sub>
tPHZ/tPZH	GND

V <sub>CC</sub> INPUTS		,,	.,		_	.,	
vcc	٧ı	t <sub>r</sub> /t <sub>f</sub>	t <sub>r</sub> /t <sub>f</sub> V <sub>M</sub> V <sub>LOAE</sub>		CL	$R_L$	$oldsymbol{V}_{\Delta}$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	Vcc	≤2.5 ns	Vcc/2	2×Vcc	50 pF	500 $\Omega$	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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] Vcc

20E

2A

6 **∏** 1Y

**DCT OR DCU PACKAGE** 

(TOP VIEW)

1<u>0E</u> [

GND [

1A 🛮

2Y 🛮 3

- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description

This dual bus buffer gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G125 features dual line drivers with 3-state outputs. The outputs are disabled when the associated output-enable  $(\overline{OE})$  input is high.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### **ORDERING INFORMATION**

TA	PACK	AGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC2G125DCTR	C25_
-40 C to 65 C	VSOP - DCU	Tape and reel	SN74LVC2G125DCUR	C25_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

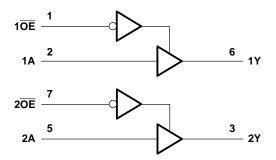
## FUNCTION TABLE (each buffer)

INP	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

- 2. The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT		
\/aa	Cupply voltage	Operating	1.65	5.5	V		
VCC	Supply voltage	Data retention only	1.5		V		
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>				
١/	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V		
VIH	nigri-level iriput voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V		
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$				
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>			
١/	Low level input valtage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	V		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$			
VI	Input voltage		0	5.5	V		
\/-	Output voltage	High or low state	0	VCC	V		
VO	3-state	3-state	0	5.5	V		
		V <sub>CC</sub> = 1.65 V		-4			
		V <sub>CC</sub> = 2.3 V		-8			
IOH	High-level output current			-16	mA		
		VCC = 3 V		-24			
		V <sub>CC</sub> = 4.5 V		-32			
		V <sub>CC</sub> = 1.65 V		4			
		V <sub>CC</sub> = 2.3 V		8			
loL	Low-level output current	V 2V		16	mA		
		VCC = 3 V		24			
		V <sub>CC</sub> = 4.5 V		32			
		V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20			
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V		
		$V_{CC} = 5 V \pm 0.5 V$		5			
TA	Operating free-air temperature		-40	85	°C		

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup> MAX	UNIT			
	$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1					
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2					
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		] ,,			
VOH	$I_{OH} = -16 \text{ mA}$	2.1/	2.4		V			
	$I_{OH} = -24 \text{ mA}$	3 V	2.3					
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8		1			
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V		0.1				
	I <sub>OL</sub> = 4 mA	1.65 V		0.45	0.45 0.3			
	I <sub>OL</sub> = 8 mA	2.3 V		0.3				
VOL	$I_{OL} = 16 \text{ mA}$	2.1/		0.4	]			
	I <sub>OL</sub> = 24 mA	3 V		0.55	1			
	I <sub>OL</sub> = 32 mA	4.5 V		0.55	1			
I <sub>I</sub> A or OE inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±5	μΑ			
l <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		±10	μΑ			
I <sub>OZ</sub>	$V_0 = 0 \text{ to } 5.5 \text{ V}$	3.6 V		10	μА			
ICC	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10	μА			
ΔICC	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V		500	μΑ			
C <sub>i</sub> Data inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5	pF			
Control inputs	A A L = ACC OL GIAD	3.3 V		4	] PF			
Co	$V_O = V_{CC}$ or GND	3.3 V		6.5	pF			

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

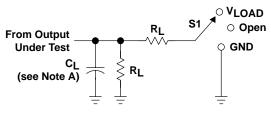
#### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		VCC =		UNIT
	(IIII O1)	(001101)	(001101)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
<sup>t</sup> pd	А	Υ	3.3	9.1	1.5	4.8	1.4	4.3	1	3.7	ns
t <sub>en</sub>	ŌĒ	Υ	4	9.9	1.9	5.6	1.2	4.7	1.2	3.8	ns
<sup>t</sup> dis	ŌĒ	Υ	1.5	11.6	1	5.8	1.4	4.6	1	3.4	ns

#### operating characteristics, $T_A = 25^\circ$

	PARAMETER		TEST	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
			CONDITIONS	TYP	TYP TYP		TYP	UNII
C1	Power dissipation	Outputs enabled	f = 10 MHz	19	19	20	22	pF
Cpd	capacitance	Outputs disabled	1 = 10 10172	2	2	2	3	ρг

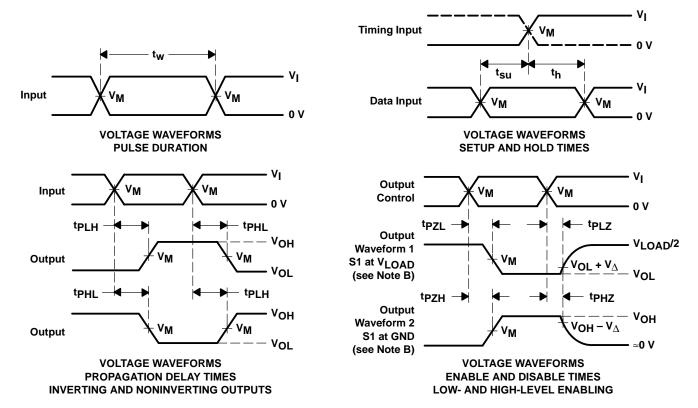




TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

**LOAD CIRCUIT** 

W	INPUTS			V	0	í	\ \ \
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	$R_L$	$V_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V ± 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\Omega}$  = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

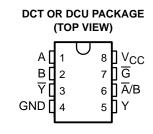
Figure 1. Load Circuit and Voltage Waveforms



#### SN74LVC2G157 SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

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- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)



#### description

This single 2-line to 1-line data selector/multiplexer is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G157 features a common strobe ( $\overline{G}$ ) input. When the strobe is high, Y is low and  $\overline{Y}$  is high. When the strobe is low, a single bit is selected from one of two sources and is routed to the outputs. The device provides true and complementary data.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
40°C to 95°C	TSSOP - DCT	Tape and reel	SN74LVC2G157DCTR	C57_
–40°C to 85°C	VSOP - DCU	Tape and reel	SN74LVC2G157DCUR	C57_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

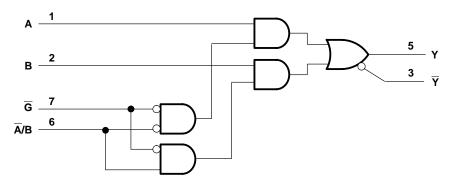
#### **FUNCTION TABLE**

	INPL	OUTI	PUTS		
G	A/B	Α	В	Υ	Ÿ
Н	Х	Χ	Х	L	Н
L	L	L	Х	L	Н
L	L	Н	Х	Н	L
L	Н	Χ	L	L	Н
L	Н	Χ	Н	Н	L

<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$
Voltage range applied to any output in the high-impedance or power-off state, V <sub>O</sub>
(see Note 1)
Voltage range applied to any output in the high or low state, VO
(see Notes 1 and 2)—0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)
Output clamp current, $I_{OK}$ ( $V_O < 0$ )
Continuous output current, IO ±50 mA
Continuous current through V <sub>CC</sub> or GND ±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package
DCU package
Storage temperature range, T <sub>Stg</sub> —65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

  2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74LVC2G157 SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

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#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT			
Voo	Supply voltage	Operating	1.65	5.5	V			
VCC	Supply voltage	Data retention only	1.5		V			
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$					
V	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V			
VIH	nigh-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		ď			
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$					
		V <sub>CC</sub> = 1.65 V to 1.95 V		$0.35 \times V_{CC}$				
V/	Low level input valte as	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V			
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		0.8	ľ			
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$				
٧ <sub>I</sub>	Input voltage		0	5.5	V			
٧o	Output voltage		0	Vcc	V			
		V <sub>CC</sub> = 1.65 V		-4				
	High-level output current	V <sub>CC</sub> = 2.3 V		-8				
loh		V = = 2 V		-16	mA			
		VCC = 3 V		-24				
		V <sub>CC</sub> = 4.5 V		-32				
		V <sub>CC</sub> = 1.65 V		4				
		V <sub>CC</sub> = 2.3 V		8				
$I_{OL}$	Low-level output current	V3V		16	mA			
		VCC = 3 V		24				
		V <sub>CC</sub> = 4.5 V		32				
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20				
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V			
		$V_{CC} = 5 V \pm 0.5 V$		5	1			
TA	Operating free-air temperature		-40	85	°C			

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT	
		$I_{OH} = -100 \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
\/~··		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
VOH		$I_{OH} = -16 \text{ mA}$	3 V	2.4			V	
		$I_{OH} = -24 \text{ mA}$	3 V	2.3				
		I <sub>OH</sub> = -32 mA	4.5 V	3.8				
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V			0.45		
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V	
VOL		I <sub>OL</sub> = 16 mA	2.1/			0.4	V	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
II	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
loff		$V_I$ or $V_O = 5.5 V$	0			±10	μΑ	
ICC		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ	
ΔlCC		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ	
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V		5	·	pF	

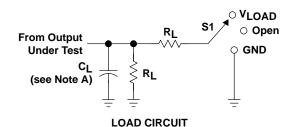
<sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		± 0.5		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Y or ₹	4.4	14	2.1	8	2	6	1.4	4	
	Ā/B		4.9	16	2.5	9	2.1	6	1.6	4	ns
	G		4.2	14	2	8	1.6	6	1.3	4	

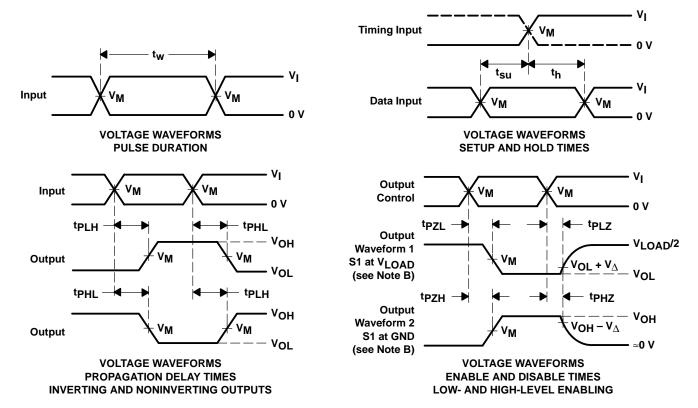
#### operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	35	35	37	40	pF



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INPUTS			V	0	í	, I
VCC	٧ı	t <sub>r</sub> /t <sub>f</sub>	VM VLOAD		CL	$R_L$	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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ην<sub>cc</sub>

120E

] 2A

6 **∏** 1Y

**DCT OR DCU PACKAGE** 

(TOP VIEW)

1OE

GND [

1A ∏

2Y **∏**3

- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



This dual buffer/line driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC2G241 is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74LVC2G241 is organized as two 1-bit line drivers with separate output-enable ( $1\overline{OE}$ , 2OE) inputs. When  $1\overline{OE}$  is low or 2OE is high, the device passes data from the A inputs to the Y outputs. When  $1\overline{OE}$  is high or 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

#### ORDERING INFORMATION

TA	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP - DCT	Tape and reel	SN74LVC2G241DCTR	C41_
	VSOP - DCU	Tape and reel	SN74LVC2G241DCUR	C41_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



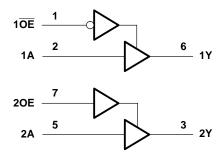
<sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### **Function Tables**

INPUTS		OUTPUT	
1OE	1A	1Y	
L	Н	Н	
L	L	L	
Н	Χ	Z	

INPUTS		OUTPUT
20E	2A	2Y
Н	Н	Н
н	L	L
L	Χ	Z

#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, VO	
(see Notes 1 and 2)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
VCC	Supply voltage	Operating	1.65	5.5	V	
		Data retention only	1.5			
	VIH High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V	
\/		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7			
۷IH		V <sub>CC</sub> = 3 V to 3.6 V	2		v	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V	
\ /	Law laval landsvaltage	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7		
V <sub>IL</sub> Low-level input v	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$		
٧ <sub>I</sub>	Input voltage	-	0	5.5	V	
\/ -	Output valtage	High or low state	0	Vcc	V	
VO	Output voltage	3-state	0	5.5		
		V <sub>CC</sub> = 1.65 V		-4	mA	
		V <sub>CC</sub> = 2.3 V		-8		
ІОН	High-level output current			-16		
		VCC = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4	mA	
		V <sub>CC</sub> = 2.3 V		8		
loL	Low-level output current	V <sub>CC</sub> = 3 V		16		
				24		
		V <sub>CC</sub> = 4.5 V		32		
		V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
	I <sub>OH</sub> = -100 μA	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
Maria	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
VOH	$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V
	I <sub>OH</sub> = -24 mA	3 V	2.3			
	I <sub>OH</sub> = -32 mA	4.5 V	3.8			
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 8 mA	2.3 V			0.3	
V <sub>OL</sub>	I <sub>OL</sub> = 16 mA	2.1/			0.4	V
	I <sub>OL</sub> = 24 mA	3 V			0.55	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub> A or OE/OE inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
l <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μΑ
loz	V <sub>O</sub> = 0 to 5.5 V	3.6 V			10	μΑ
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
∆ICC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5		pF
Co	$V_O = V_{CC}$ or GND	3.3 V		6.5		pF

 $<sup>\</sup>uparrow$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

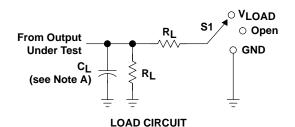
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		± 0.5	= 5 V 5 V	UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	3.3	8.8	1.5	4.8	1.4	4.3	1	3.7	ns
t <sub>en</sub>	ŌĒ	Y	4	9.9	1.9	5.6	1.2	4.7	1.2	3.8	ns
t <sub>dis</sub>	ŌĒ	Υ	1.5	11.6	1	5.8	1.4	4.4	1	3.4	ns
t <sub>en</sub>	OE	Y	3.2	8.8	1.5	4.7	1.6	4.1	1.1	3.3	ns
<sup>t</sup> dis	OE	Υ	1.7	12.5	1	5.2	1	4.2	1	3.3	ns

# operating characteristics, $T_A = 25^\circ$

PARAMETER		TEST	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
C		Outputs enabled	f = 10 MHz	19	19	20	22	pF
F **	d capacitance per buffer/driver	Outputs disabled		2	2	2	3	

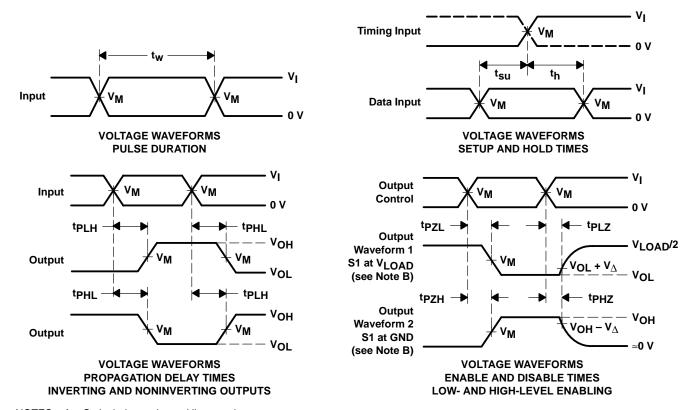


#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

W	INPUTS				6	Г.	.,
VCC	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V $\pm$ 0.15 V	VCC	≤ <b>2</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 $\Omega$	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
5 V + 0.5 V	Voc	<2.5 ns	Voc/2	2 × Voo	50 nF	500 O	03V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\Omega} = 50 \Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

# 1A 1 8 V<sub>CC</sub> 3Y 2 7 1Y 2A 3 6 3A GND 4 5 2Y

## description

This triple inverter is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC3G04 performs the Boolean function  $Y = \overline{A}$ .

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

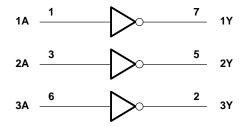
#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡	
–40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC3G04DCTR		
-40 C to 65 C	VSOP – DCU	Tape and reel	SN74LVC3G04DCUR		

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or po	ower-off state, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package .	
DCU package .	
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of VCC is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/	Cupply veltage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		ľ	
		V <sub>CC</sub> = 1.65 V to 1.95 V	$0.65 \times V_{CC}$			
\/	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIН	nigii-level iriput voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	2		]	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$0.7 \times V_{CC}$			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
\ /	Low level input valtage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	] ,,	
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		0.8	V	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$	1	
٧ <sub>I</sub>	Input voltage		0	5.5	V	
٧o	Output voltage		0	Vcc	V	
		V <sub>CC</sub> = 1.65 V		-4		
	High-level output current	V <sub>CC</sub> = 2.3 V		-8		
lOH		V <sub>CC</sub> = 3 V		-16	mA	
		vCC = 2 v		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V 3 V		16	mA	
		V <sub>CC</sub> = 3 V		24	]	
		V <sub>CC</sub> = 4.5 V				
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10		
		$V_{CC} = 5 V \pm 0.5 V$		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP <sup>†</sup>	MAX	UNIT
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
\/a	$I_{OH} = -8 \text{ m},$	2.3 V	1.9			V
Voн	I <sub>OH</sub> = -16 mA	2.1/	2.4			V
	I <sub>OH</sub> = -24 mA	3 V	2.3			
	I <sub>OH</sub> = −32 mA	4.5 V	3.8			
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1	
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
\/	$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	V
VOL	$I_{OL} = 16 \text{ mA}$	2.1/			0.4	V
	I <sub>OL</sub> = 24 mA	3 V			0.55	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55	
lį	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$	0			±10	μΑ
ICC	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
ΔlCC	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V				pF

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

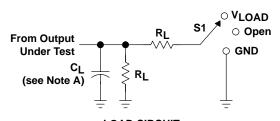
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(1141 01)	(141 01)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	А	Υ									ns

# operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

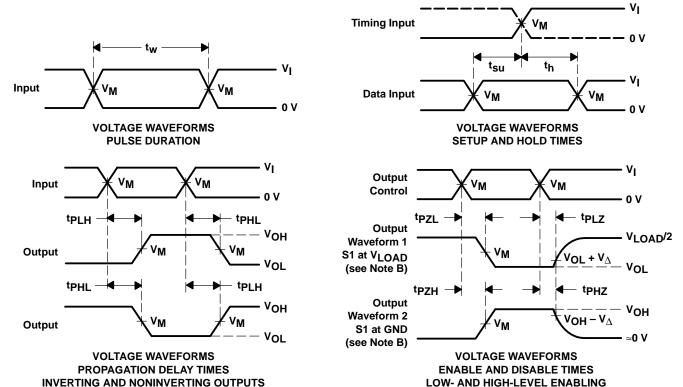
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

LOAD	CIRCUIT	

.,	$\begin{array}{c c} \hline \text{INPUTS} \\ \hline V_{\text{I}} & t_{\text{r}}/t_{\text{f}} \\ \end{array}  V_{\text{M}}  V_{\text{LOA}}$		,,	.,		_	V	
Vcc			VLOAD	CL	RL	$oldsymbol{V}_\Delta$		
1.8 V $\pm$ 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V	
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V	
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V	
5 V ± 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V	



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



# SN74LVC3G06 TRIPLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

SCES364A - AUGUST 2001 - REVISED SEPTEMBER 2001

- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Input and Open-Drain Output Accepts Voltages up to 5.5 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

# 1A 1 8 VCC 3Y 2A 3 6 3A GND 4 5 2Y

# description

This triple inverter buffer/driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The output of the SN74LVC3G06 is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

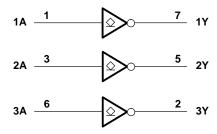
#### ORDERING INFORMATION

TA	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC3G06DCTR	
-40 C 10 65 C	VSOP - DCU	Tape and reel	SN74LVC3G06DCUR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н





<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	–0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)	–0.5 V to 6.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions (see Note 4)

			MIN	MAX	UNIT			
\/	Supply voltage	Operating	1.65	5.5	V			
Vcc	Supply voltage	Data retention only	1.5		V			
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>					
\/	Lligh lovel input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		V			
VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V			
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$					
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>				
V	Low-level input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V						
V <sub>IL</sub>		V <sub>CC</sub> = 3 V to 3.6 V		0.8	V			
		V <sub>CC</sub> = 4.5 V to 5.5 V		$0.3 \times V_{CC}$				
٧ı	Input voltage	-	0	5.5	V			
٧o	Output voltage		0	VCC	V			
		V <sub>CC</sub> = 1.65 V		4				
		V <sub>CC</sub> = 2.3 V		8				
lOL	Low-level output current	V 2 V		16	mA			
		VCC = 3 V		24				
		V <sub>CC</sub> = 4.5 V		32				
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20				
Δt/Δν	Input transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		10	ns/V			
		V <sub>CC</sub> = 5 V ± 0.5 V		5				
T <sub>A</sub>	Operating free-air temperature		-40	85	°C			

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN TYPT MAX	UNIT
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45	
\/ - ·	I <sub>OL</sub> = 8 mA	2.3 V	0.3	\ /
VOL	I <sub>OL</sub> = 16 mA	2.1/	0.4	V
	I <sub>OL</sub> = 24 mA	3 V	0.55	
	I <sub>OL</sub> = 32 mA	4.5 V	0.55	
lį	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	±5	μΑ
loff	$V_I$ or $V_O = 5.5 V$	0	±10	μΑ
lcc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	μΑ
ΔlCC	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V	500	μΑ
Ci	$V_I = V_{CC}$ or GND	3.3 V		pF
Co	$V_O = V_{CC}$ or GND	3.3 V		pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

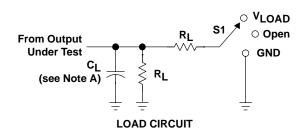
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		UNIT						
	(INFO1) (C	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ									ns

# operating characteristics, $T_A = 25^{\circ}C$

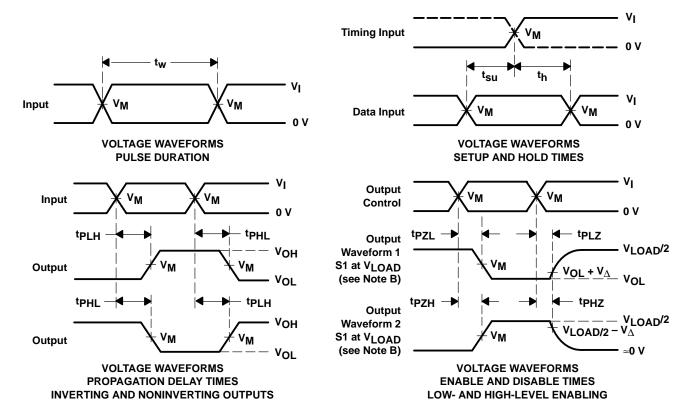
Γ	PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
L	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
	C <sub>pd</sub> Power dissipation capacitance	f = 10 MHz					pF

# PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	<b>S</b> 1
tpZL (see Notes E and F)	V <sub>LOAD</sub>
tpLZ (see Notes E and G)	VLOAD
t <sub>PHZ</sub> /t <sub>PZH</sub>	V <sub>LOAD</sub>

	INPUT						
VCC	VI	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	VCC	≤ <b>2.5</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. Since this device has open-drain outputs,  $t_{PLZ}$  and  $t_{PZL}$  are the same as  $t_{pd}$ .
  - F. tpzL is measured at V<sub>M</sub>.
  - G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Input and Open-Drain Output Accepts Voltages up to 5.5 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

# 1A 1 8 V<sub>CC</sub> 3Y 2 7 1Y 2A 3 6 3A GND 4 5 2Y

### description

This triple buffer/driver is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The output of the SN74LVC3G07 is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

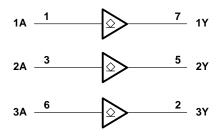
#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
40°C to 95°C	TSSOP - DCT	Tape and reel	SN74LVC3G07DCTR	
–40°C to 85°C	VSOP – DCU	Tape and reel	SN74LVC3G07DCUR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design quidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each buffer/driver)

INPUT A	OUTPUT Y
Н	Н
L	L





<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state	e, V <sub>O</sub>
(see Note 1)	
Output voltage range, VO (see Notes 1 and 2)	
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\hat{\theta}_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V	Cupply voltage	Operating	1.65	5.5	V
VCC	Supply voltage	Data retention only			V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		
V/	Himb lavelingut valtage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
۷IH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V
		V <sub>CC</sub> = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	
.,	Low-level input voltage $V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
VIL		V <sub>CC</sub> = 3 V to 3.6 V		0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>	
٧ı	Input voltage	•	0	5.5	V
۷o	Output voltage		0	Vcc	V
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	
loL	Low-level output current	V 2V		16	mA
		VCC = 3 V		24	
		V <sub>CC</sub> = 4.5 V		32	
		$V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
TA	Operating free-air temperature	•	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC	MIN TYPT MAX	UNIT
	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1	
	I <sub>OL</sub> = 4 mA	1.65 V	0.45	
\/ - ·	I <sub>OL</sub> = 8 mA	2.3 V	0.3	V
VOL	I <sub>OL</sub> = 16 mA	2.1/	0.4	V
	I <sub>OL</sub> = 24 mA	3 V	0.55	
	I <sub>OL</sub> = 32 mA	4.5 V	0.55	
lį	$V_I = 5.5 \text{ V or GND}$	0 to 5.5 V	±5	μΑ
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0	±10	μΑ
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V	10	μΑ
ΔlCC	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND	3 V to 5.5 V	500	μΑ
C <sub>i</sub>	$V_I = V_{CC}$ or GND	3.3 V		pF
Co	$V_O = V_{CC}$ or GND	3.3 V		pF

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

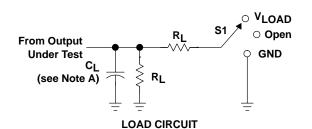
PARAMETER FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT	
	(INPOT) (OUTPO	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ									ns

# operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		PARAMETER TEST CONDITIONS		V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	ONIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

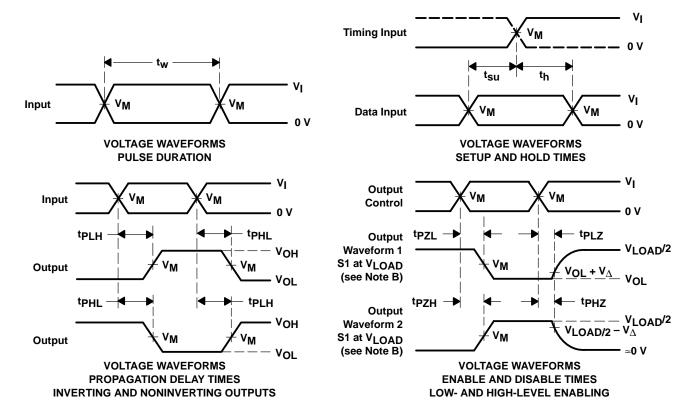
PRODUCT PREVIEW

# PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



TEST	<b>S</b> 1
tpzL (see Notes E and F)	VLOAD
tpLZ (see Notes E and G)	VLOAD
tPHZ/tPZH	VLOAD

	INPUT						
VCC	VI	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	vcc	≤ 2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤ 2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>500</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	VCC	≤ <b>2.5</b> ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



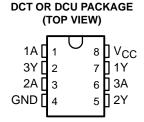
NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω.
- D. The outputs are measured one at a time with one transition per measurement.
- E. Since this device has open-drain outputs, tpLz and tpzL are the same as tpd.
- F. tp71 is measured at V<sub>M</sub>.
- G.  $t_{PLZ}$  is measured at  $V_{OL} + V_{\Delta}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Feature Supports Partial-Power-Down Mode Operation



## description

This triple Schmitt-trigger inverter is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC3G14 contains three inverters and performs the Boolean function  $Y = \overline{A}$ . The device functions as three independent inverters but, because of Schmitt action, it may have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

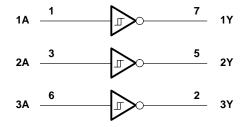
#### ORDERING INFORMATION

TA	PACK	AGET	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	TSSOP - DCT	Tape and reel	SN74LVC3G14DCTR	
–40°C to 85°C	VSOP – DCU	Tape and reel	SN74LVC3G14DCUR	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Voltage range applied to any output in the high-impedance or power-off state, $V_0$	
(see Note 1)	<u> </u>
Output voltage range, VO (see Notes 1 and 2)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	
Continuous output current, IO	±50 mA
Continuous current through V <sub>CC</sub> or GND	
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
\/	Cupply voltage	Operating	1.65	5.5	V
Vcc	Supply voltage	Data retention only	1.5		V
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
	High-level output current	V <sub>CC</sub> = 1.65 V		-4	mA
		V <sub>CC</sub> = 2.3 V		-8	
lOH		V <sub>CC</sub> = 3 V		-16	
				-24	
		V <sub>CC</sub> = 4.5 V		-32	
		V <sub>CC</sub> = 1.65 V		4	
		V <sub>CC</sub> = 2.3 V		8	mA
lOL	Low-level output current	V00 - 3 V		16	
		$V_{CC} = 3 V$		24	
		V <sub>CC</sub> = 4.5 V		32	
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# PRODUCT PREVIEW

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	MIN	TYPT MAX	UNIT	
		1.65 V	0.79	1.16		
V <sub>T+</sub>		2.3 V	1.11	1.56		
Positive-going input threshold voltage		3 V	1.5	1.87	V	
		4.5 V	2.16	2.74		
		5.5 V	2.61	3.33		
		1.65 V	0.39	0.62		
V <sub>T</sub> _		2.3 V	0.58	0.87		
Negative-going input		3 V	0.84	1.14	V	
threshold voltage		4.5 V	1.41	1.79		
		5.5 V	1.87	2.29		
		1.65 V	0.37	0.62		
ΔVT		2.3 V	0.48	0.77		
Hysteresis		3 V	0.56	0.87	V	
(V <sub>T+</sub> – V <sub>T</sub> –)		4.5 V	0.71	1.04		
		5.5 V	0.71	1.11		
	$I_{OH} = -100 \mu\text{A}$	1.65 V to 4.5 V	V <sub>CC</sub> -0.1			
	I <sub>OH</sub> = -4 mA	1.65 V	1.2			
\/a	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9		V	
VOH	$I_{OH} = -16 \text{ mA}$	3 V	2.4		V	
	I <sub>OH</sub> = -24 mA	3 V	2.3			
(V <sub>T+</sub> – V <sub>T</sub> –)  VOH	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
	I <sub>OL</sub> = 100 μA	1.65 V to 4.5 V		0.1		
	I <sub>OL</sub> = 4 mA	1.65 V		0.45		
Val	I <sub>OL</sub> = 8 mA	2.3 V		0.3	V	
VOL	I <sub>OL</sub> = 16 mA	3 V		0.4	V	
	I <sub>OL</sub> = 24 mA	3 V		0.55		
	I <sub>OL</sub> = 32 mA	4.5 V		0.55		
lį	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±5	μΑ	
l <sub>off</sub>	$V_I$ or $V_O = 5.5 V$	0		±10	μΑ	
Icc	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		10	μΑ	
Δl <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V		500	μΑ	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			pF	

 $<sup>\</sup>dagger$  All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =	2.7 V	V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(INPUT)	(INPOT) (O	(INFOI) (OUTFOI)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t <sub>pd</sub>	А	Υ											ns

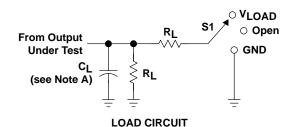
# SN74LVC3G14 TRIPLE SCHMITT-TRIGGER INVERTER

SCES367A - AUGUST 2001 - REVISED SEPTEMBER 2001

# operating characteristics, $T_A = 25^{\circ}C$

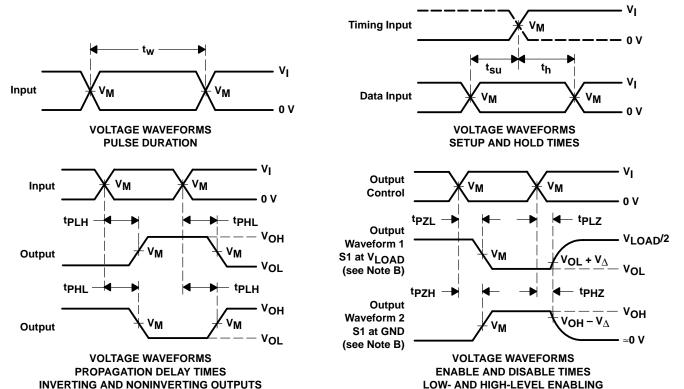
PARAMETER		PARAMETER TEST CONDITIONS V <sub>CC</sub> = 1.8 V V <sub>CC</sub> = 2.5 V		V <sub>CC</sub> = 3.3 V V <sub>CC</sub> = 5 V		UNIT	
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C	od Power dissipation capacitance	f = 10 MHz					pF

#### PARAMETER MEASUREMENT INFORMATION



TEST	<b>S</b> 1
tPLH/tPHL	Open
tPLZ/tPZL	<sup>V</sup> LOAD
tPHZ/tPZH	GND

.,	INPUTS		.,	.,		Ĺ	.,
Vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	V <sub>M</sub>	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



- Supports 5-V V<sub>CC</sub> Operation
- Typical V<sub>OLP</sub> (Output Ground Bounce)
   <0.8 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- Typical V<sub>OHV</sub> (Output V<sub>OH</sub> Undershoot)
   >2 V at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

# 1A 1 8 VCC 3Y 2A 3 6 3A GND 4 5 2Y

## description

This triple buffer gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC3G34 performs the Boolean function Y = A in positive logic.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

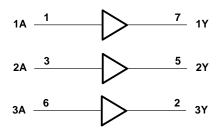
#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 85°C	TSSOP - DCT	Tape and reel	SN74LVC3G34DCTR	
-40°C to 85°C	VSOP – DCU	Tape and reel	SN74LVC3G34DCUR	·

<sup>&</sup>lt;sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

# FUNCTION TABLE (each gate)

	<u> </u>
INPUT	OUTPUT
Α	Y
Н	Н
L	L



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 6.5 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Voltage range applied to any output in the high-impedance or power-off state, VO	
(see Note 1)	0.5 V to 6.5 V
Output voltage range, VO (see Notes 1 and 2)C	$0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ C } < 0)$	–50 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0)	–50 mA
Continuous output current, I <sub>O</sub>	±50 mA
Continuous current through V <sub>CC</sub> or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DCT package	220°C/W
DCU package	227°C/W
Storage temperature range, T <sub>stq</sub>	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The value of V<sub>CC</sub> is provided in the recommended operating conditions table.
  - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

# PRODUCT PREVIEW

# recommended operating conditions (see Note 4)

			MIN	MAX	UNIT	
\/00	Supply voltage	Operating	1.65	5.5	V	
VCC	Supply voltage	Data retention only	1.5		V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$			
\/	High lovel input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V	
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	2		\ \ \	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.7 × V <sub>CC</sub>			
		V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>		
١/	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V	
$V_{IL}$	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$		0.8	ľ	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$0.3 \times V_{CC}$		
٧ <sub>I</sub>	Input voltage		0	5.5	V	
٧o	Output voltage		0	Vcc	V	
	High-level output current	V <sub>CC</sub> = 1.65 V		-4		
		$V_{CC} = 2.3 \text{ V}$		-8		
lOH		V <sub>CC</sub> = 3 V		-16	mA	
		VCC = 3 V		-24		
		V <sub>CC</sub> = 4.5 V		-32		
		V <sub>CC</sub> = 1.65 V		4		
		V <sub>CC</sub> = 2.3 V		8		
$I_{OL}$	Low-level output current	V = = 3 V		16	mA	
		V <sub>CC</sub> = 3 V		24		
		V <sub>CC</sub> = 4.5 V		32		
		$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$		20		
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V	
		$V_{CC} = 5 V \pm 0.5 V$		5		
TA	Operating free-air temperature		-40	85	°C	

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	VCC	MIN	TYP†	MAX	UNIT	
		$I_{OH} = -100 \mu\text{A}$	1.65 V to 5.5 V	V <sub>CC</sub> -0.1				
		$I_{OH} = -4 \text{ mA}$	1.65 V	1.2				
		$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V	
Vон		$I_{OH} = -16 \text{ mA}$	2.1/	2.4			V	
		I <sub>OH</sub> = -24 mA	3 V	2.3				
		I <sub>OH</sub> = -32 mA	4.5 V	3.8				
		I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V			0.1		
		I <sub>OL</sub> = 4 mA	1.65 V		0.45			
<b>.</b> ,		I <sub>OL</sub> = 8 mA	2.3 V			0.3	V	
VOL	I <sub>OL</sub> = 16 mA		2.1/			0.4	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	
		I <sub>OL</sub> = 24 mA	3 V			0.55		
		I <sub>OL</sub> = 32 mA	4.5 V			0.55		
Ц	A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ	
loff		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0			±10	μΑ	
Icc		$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V		•	10	μΑ	
ΔlCC		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	μΑ	
C <sub>i</sub>		$V_I = V_{CC}$ or GND	3.3 V				pF	

<sup>&</sup>lt;sup>†</sup> All typical values are at  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .

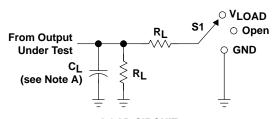
# switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> =		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<sup>t</sup> pd	A or B	Υ									ns

# operating characteristics, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT
		TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz					pF

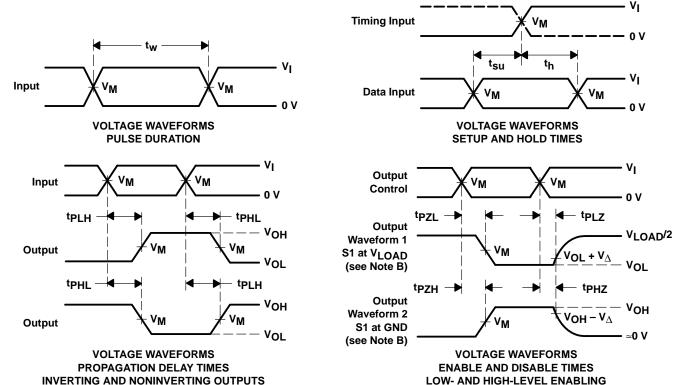
#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VLOAD
tPHZ/tPZH	GND

$I \cap A \Gamma$	$\sim$	Юι	~ 1	ΙІТ
LOAD	, 6	IK!	υ	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,

W	INPUTS			V	0	Б.	V
Vcc	٧ <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>	VM	VLOAD	CL	RL	$oldsymbol{V}_\Delta$
1.8 V ± 0.15 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V $\pm$ 0.2 V	VCC	≤2 ns	V <sub>CC</sub> /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V $\pm$ 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	<b>500</b> Ω	0.3 V
5 V $\pm$ 0.5 V	VCC	≤2.5 ns	V <sub>CC</sub> /2	2×V <sub>CC</sub>	50 pF	500 Ω	0.3 V



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz, Z<sub>O</sub> = 50  $\Omega$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



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- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

# DBV OR DCK PACKAGE (TOP VIEW) OE 1 5 VCC A 2 GND 3 4 B

# description

The SN74CBT1G125 features a single high-speed line switch. The switch is disabled when the output-enable ( $\overline{\text{OE}}$ ) input is high.

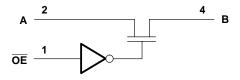
#### **ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74CBT1G125DBVR	S25_
–40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74CBT1G125DCKR	SM_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT OE	FUNCTION			
L	A port = B port			
Н	Disconnect			





<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

SCDS046E - FEBRUARY 1998 - REVISED OCTOBER 2000

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I/O</sub> < 0)	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

# recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		8.0	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT	
VIK		$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA					-1.2	V
II		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$					±1	μΑ
Icc		$V_{CC} = 5.5 \text{ V},$	$I_{O} = 0$ ,	$V_I = V_{CC}$ or $GI$	ND			1	μΑ
Ci	Control input	V <sub>I</sub> = 3 V or 0					3		pF
C <sub>io(O</sub>	FF)	$V_0 = 3 \text{ V or } 0,$	OE = V <sub>CC</sub>				4		pF
r <sub>on</sub> §		$V_{CC} = 4 V$ ,	TYP at $V_{CC} = 4 \text{ V}$ ,	V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		14	20	
			\/ 0	I <sub>I</sub> = 64 mA			5	7	Ω
		V <sub>CC</sub> = 4.5 V	/ V <sub>I</sub> = 0	I <sub>I</sub> = 30 mA			5	7	52
			V <sub>I</sub> = 2.4 V,	l <sub>I</sub> = 15 mA			10	15	

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$  (unless otherwise noted),  $T_A = 25^{\circ}\text{C}$ .

### switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V	V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
	(INFOT)	(0011 01)	MIN MAX	MIN	MAX	
t <sub>pd</sub> ¶	A or B	B or A	0.35		0.25	ns
<sup>t</sup> en	ŌĒ	A or B	5.5	1.6	4.9	ns
<sup>t</sup> dis	ŌĒ	A or B	4.5	1	4.2	ns

<sup>¶</sup>The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



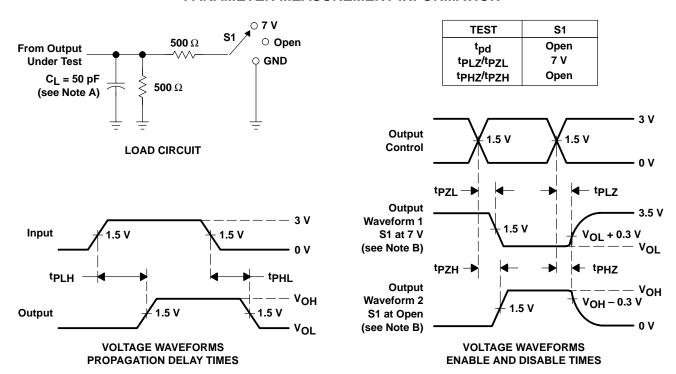
NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

**SN74CBT1G125** 

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCDS063H - JULY 1998 - REVISED JUNE 2001

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

# OE 1 5 VCC A 2 GND 3 4 B

## description

The SN74CBTD1G125 features a single high-speed line switch. The switch is disabled when the output-enable  $(\overline{OE})$  input is high. A diode to  $V_{CC}$  is integrated on the chip to allow for level shifting between 5-V inputs and 3.3-V outputs.

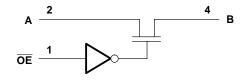
#### ORDERING INFORMATION

TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡	
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74CBTD1G125DBVR	P25_	
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74CBTD1G125DCKR	PM_	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect





<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

SCDS063H - JULY 1998 - REVISED JUNE 2001

# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ )	
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		8.0	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$				-1.2	V
VOН		See Figure 2						
lı		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$				±1	μΑ
Icc		$V_{CC} = 5.5 \text{ V},$	I <sub>O</sub> = 0,	$V_I = V_{CC}$ or GND			1.5	mA
∆lcc§	Control input	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			2.5	mA
Ci	Control input	V <sub>I</sub> = 3 V or 0				2		pF
C <sub>io(OFF)</sub>	)	$V_0 = 3 \text{ V or } 0,$	OE = V <sub>CC</sub>			3.5		pF
r <sub>on</sub> ¶		V. 0	\/ı = 0	$I_I = 64 \text{ mA}$		5	7	
		$V_{CC} = 4.5 V$	V <sub>I</sub> = 0	I <sub>I</sub> = 30 mA		5	7	Ω
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		35	50	

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ}\text{C}$ .



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

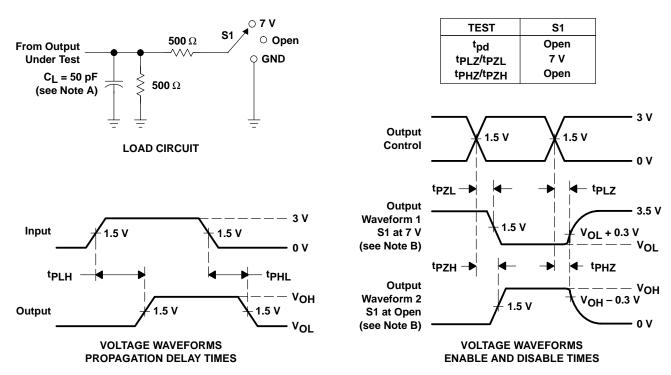
<sup>¶</sup>Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

# switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> †	A or B	B or A		0.25	ns
t <sub>en</sub>	ŌĒ	A or B	2	5.9	ns
t <sub>dis</sub>	ŌĒ	A or B	1	4.7	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## PARAMETER MEASUREMENT INFORMATION

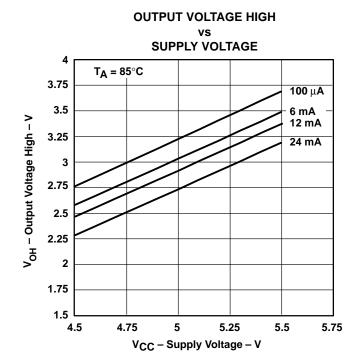


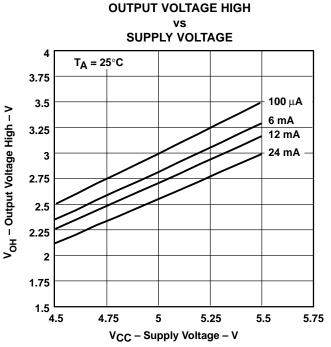
- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. tpl 7 and tpHZ are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



# **TYPICAL CHARACTERISTICS**





### **OUTPUT VOLTAGE HIGH SUPPLY VOLTAGE** $T_A = 0^{\circ}C$ 3.75 3.5 **100** μ**A** V<sub>OH</sub> - Output Voltage High - V 3.25 6 mA 12 mA 3 24 mA 2.75 2.5 2.25 2 1.75 1.5 4.5 4.75 5.25 5.5 5.75 V<sub>CC</sub> - Supply Voltage - V



- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels

### description

The SN74CBT1G384 features a single high-speed line switch. The switch is disabled when the output-enable  $(\overline{OE})$  input is high.

# A 1 1 5 VCC B 2 GND 3 4 OE

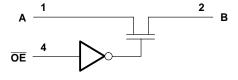
### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74CBT1G384DBVR	S8D_
–40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74CBT1G384DCKR	S8_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

SCDS065D - JULY 1998 - REVISED OCTOBER 2000

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I/O</sub> < 0)	
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
$V_{IH}$	High-level control input voltage	2		V
V <sub>IL</sub>	Low-level control input voltage		8.0	V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER		TEST CONDI	TIONS		MIN	TYP‡	MAX	UNIT
VIK		$V_{CC} = 4.5 \text{ V},$	$I_{I} = -18 \text{ mA}$					-1.2	V
II		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$					±1	μΑ
Icc		$V_{CC} = 5.5 \text{ V},$	$I_{O} = 0$ ,	$V_I = V_{CC}$ or $GN$	ND			1	μΑ
Ci	Control input	V <sub>I</sub> = 3 V or 0					3		pF
C <sub>io(OF</sub>	·F)	$V_{O} = 3 \text{ V or } 0,$	OE = VCC				4		pF
		V <sub>CC</sub> = 4 V,	TYP at $V_{CC} = 4 V$ ,	$V_1 = 2.4 V$ ,	I <sub>I</sub> = 15 mA		14	20	
r <sub>on</sub> §			V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA			5	7	Ω
iona		$V_{CC} = 4.5 \text{ V}$	v1 = 0	I <sub>I</sub> = 30 mA			5	7	52
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA			10	15	

 $<sup>^{\</sup>ddagger}$  All typical values are at V<sub>CC</sub> = 5 V (unless otherwise noted), T<sub>A</sub> = 25°C.

### switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V	V <sub>CC</sub> =	: 5 V 5 V	UNIT
	(1141 01)	(0011 01)	MIN MAX	MIN	MAX	
$t_{pd}\P$	A or B	B or A	0.35		0.25	ns
t <sub>en</sub>	ŌĒ	A or B	5.5	1.6	4.9	ns
<sup>t</sup> dis	ŌĒ	A or B	4.5	1	4.2	ns

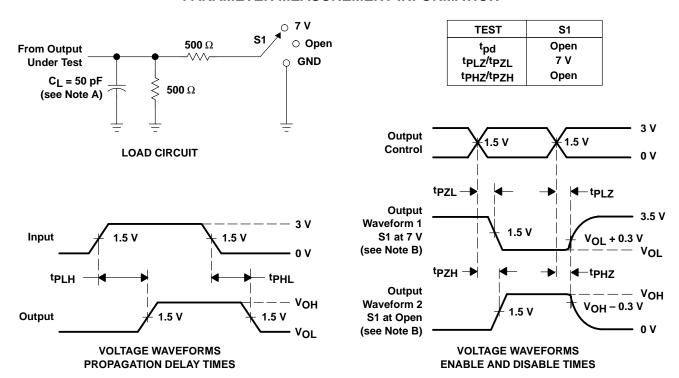
The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \,\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The output is measured with one input transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms

SCDS066G - JULY 1998 - REVISED OCTOBER 2001

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

# DBV OR DCK PACKAGE (TOP VIEW) A [ 1 5 ] V<sub>CC</sub> B [ 2 4 ] $\overline{\text{OE}}$

### description

The SN74CBTD1G384 features a single high-speed line switch. The switch is disabled when the output-enable  $(\overline{OE})$  input is high. A diode to  $V_{CC}$  is integrated on the chip to allow for level shifting between 5-V inputs and 3.3-V outputs.

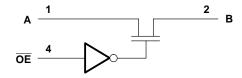
### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
10°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74CBTD1G384DBVR	P8D_
−40°C to 85°C	SOP (SC-70) - DCK	Tape and reel	SN74CBTD1G384DCKR	P8_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT OE	FUNCTION		
L	A port = B port		
Н	Disconnect		



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I/O</sub> < 0)	–50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level control input voltage	2		V
VIL	Low-level control input voltage		8.0	V
TA	Operating free-air temperature	-40	85	°C

In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

NOTE 3: All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.	ARAMETER		TEST CONDIT	TIONS	MIN	TYP‡	MAX	UNIT
٧ <sub>IK</sub>		$V_{CC} = 4.5 \text{ V},$	I <sub>I</sub> = -18 mA				-1.2	V
Vон		See Figure 2						
lį		$V_{CC} = 5.5 \text{ V},$	$V_I = 5.5 \text{ V or GND}$				±1	μΑ
ICC		$V_{CC} = 5.5 \text{ V},$	$I_{O} = 0$ ,	$V_I = V_{CC}$ or GND			1.5	mA
∆lCC§	Control input	$V_{CC} = 5.5 \text{ V},$	One input at 3.4 V,	Other inputs at V <sub>CC</sub> or GND			2.5	mA
Ci	Control input	V <sub>I</sub> = 3 V or 0				2		pF
C <sub>io(OFF</sub>	=)	$V_{O} = 3 \text{ V or } 0,$	OE = V <sub>CC</sub>			3.5		pF
			V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA		5	7	
$r_{on}\P$		V <sub>CC</sub> = 4.5 V	v   = 0	I <sub>I</sub> = 30 mA		5	7	Ω
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		35	50	

 $<sup>^{\</sup>ddagger}$  All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_{A} = 25^{\circ}\text{C}$ .



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.

Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

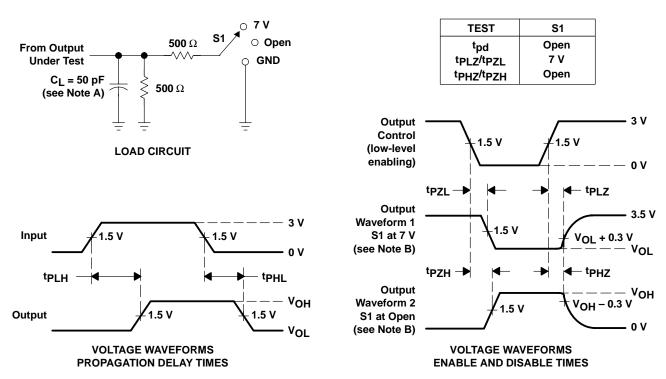
SCDS066G - JULY 1998 - REVISED OCTOBER 2001

### switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>pd</sub> †	A or B	B or A		0.25	ns
<sup>t</sup> en	ŌĒ	A or B	2	5.9	ns
<sup>t</sup> dis	ŌĒ	A or B	1	4.7	ns

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

#### PARAMETER MEASUREMENT INFORMATION

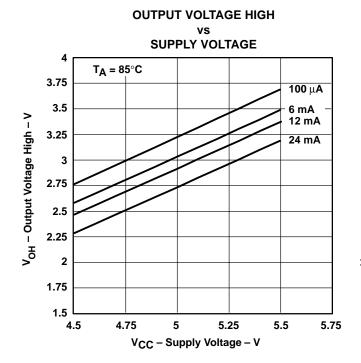


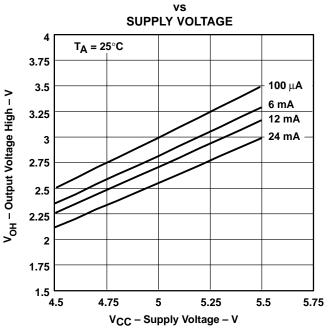
- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_f \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
  - D. The output is measured with one input transition per measurement.
  - E. tpLz and tpHz are the same as tdis.
  - F. tpzL and tpzH are the same as ten.
  - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



### TYPICAL CHARACTERISTICS





**OUTPUT VOLTAGE HIGH** 

### **OUTPUT VOLTAGE HIGH**

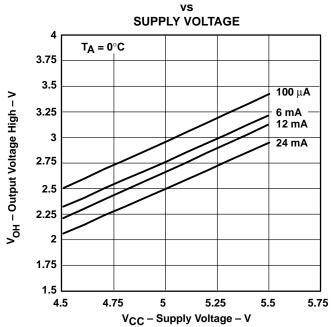


Figure 2. V<sub>OH</sub> Values



General Information	1
AUC Single Gates	2
LVC Single Gates	3
LVC Dual Gates	4
LVC Triple Gates	5
CBT Single Gates	6
CBTLV Single Gates	7
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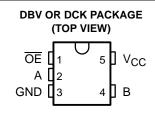
	Comonic	Page
SN74CBTLV1G125	Low-Voltage Single FET Bus Switch	7–3

SCDS057E - MARCH 1998 - REVISED MARCH 2001

- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions

### description

The SN74CBTLV1G125 features a single high-speed line switch. The switch is disabled when the output-enable (OE) input is high.



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### **ORDERING INFORMATION**

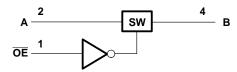
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74CBTLV1G125DBVR	V25_
-40 C to 65 C	SOP (SC-70) – DCK	Tape and reel	SN74CBTLV1G125DCKR	VM_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

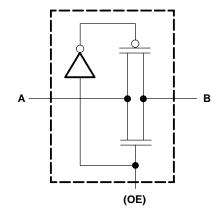
### **FUNCTION TABLE**

INPUT OE	FUNCTION
L	A port = B port
Н	Disconnect

### logic diagram (positive logic)



### simplified schematic, each FET switch





<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

SCDS057E - MARCH 1998 - REVISED MARCH 2001

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Continuous channel current	128 mA
Input clamp current, I <sub>IK</sub> (V <sub>I/O</sub> < 0)	
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DBV package	
DCK package	) 252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MAX	UNIT
Vcc	V <sub>CC</sub> Supply voltage		3.6	V
\/	High-level control input voltage	1.7		V
VIH	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		\ \ \
\/	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.7	V
VIL	Low-level control input voltage $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	V
T <sub>A</sub> Operating free-air temperature		-40	85	°C

NOTE 3: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PAI	RAMETER		TEST CONDITION	ONS	MIN	TYP‡	MAX	UNIT
VIK		V <sub>CC</sub> = 3 V,	I <sub>I</sub> = -18 mA				-1.2	V
II		V <sub>CC</sub> = 3.6 V,	$V_I = V_{CC}$ or GND				±1	μΑ
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_{I}$ or $V_{O} = 0$ to 3.6	V			10	μΑ
ICC		$V_{CC} = 3.6 \text{ V},$	I <sub>O</sub> = 0,	$V_I = V_{CC}$ or GND			10	μΑ
∆lcc§	Control inputs	V <sub>CC</sub> = 3.6 V,	One input at 3 V,	Other inputs at V <sub>CC</sub> or GND			300	μΑ
Ci	Control inputs	V <sub>I</sub> = 3 V or 0				2.5		pF
C <sub>io(OFF</sub>	F)	$V_{O} = 3 \text{ V or } 0,$	OE = V <sub>CC</sub>			7		pF
		.,	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA		7	10	
		$V_{CC} = 2.3 \text{ V},$ TYP at $V_{CC} = 2.5 \text{ V}$	V   = 0	I <sub>I</sub> = 24 mA		7	10	
r <sub>on</sub> ¶		111 di vec = 2.0 v	V <sub>I</sub> = 1.7 V,	I <sub>I</sub> = 15 mA		15	25	Ω
'on"			V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA		5	7	22
	V <sub>CC</sub> = 3 V	V <sub>CC</sub> = 3 V	v <sub>1</sub> = 0	I <sub>I</sub> = 24 mA		5	7	
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA		10	15	

<sup>‡</sup> All typical values are at  $V_{CC}$  = 3.3 V (unless otherwise noted),  $T_A$  = 25°C.



NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

<sup>§</sup> This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

<sup>¶</sup>Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

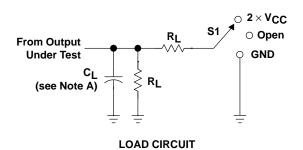
### SN74CBTLV1G125 LOW-VOLTAGE SINGLE FET BUS SWITCH

SCDS057E - MARCH 1998 - REVISED MARCH 2001

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

I DADAMETED I	FROM (INPUT)	·	V <sub>CC</sub> =		V <sub>CC</sub> =		UNIT
	(1141 01)		MIN	MAX	MIN	MAX	
t <sub>pd</sub> †	A or B	B or A		0.15		0.25	ns
t <sub>en</sub>	ŌĒ	A or B	1	4	1	4	ns
<sup>t</sup> dis	ŌĒ	A or B	1	5	1	4.1	ns

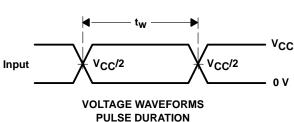
<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

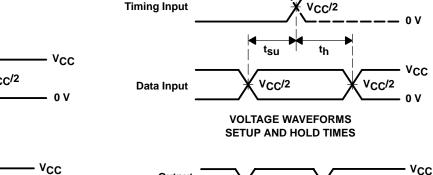


TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2×V <sub>CC</sub>
tPHZ/tPZH	GND

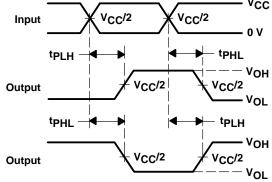
VCC	CL	RL	$oldsymbol{V}_\Delta$
2.5 V ±0.2 V	30 pF	<b>500</b> Ω	0.15 V
3.3 V $\pm$ 0.3 V	50 pF	500 Ω	0.3 V

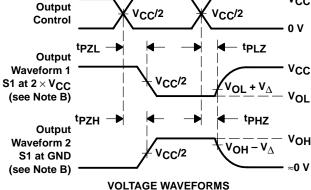
VCC





**Timing Input** 





**VOLTAGE WAVEFORMS** PROPAGATION DELAY TIMES **INVERTING AND NONINVERTING OUTPUTS** 

**ENABLE AND DISABLE TIMES** LOW- AND HIGH-LEVEL ENABLING

NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{O}$  = 50  $\Omega$ ,  $t_{f} \leq$  2 ns,  $t_{f} \leq$  2 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



General Information	1
AUC Single Gates	2
LVC Single Gates	3
LVC Dual Gates	4
LVC Triple Gates	5
CBT Single Gates	6
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SN74AHC1G08	Single 2-Input Positive-AND Gate	. 8–19
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SN74AHC1G32	Single 2-Input Positive-OR Gate	. 8–27
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SCLS313H - MARCH 1996 - REVISED JULY 2001

- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### DBV OR DCK PACKAGE (TOP VIEW)



### description

The SN74AHC1G00 performs the Boolean function  $Y = \overline{A \bullet B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

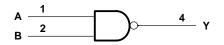
### **ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G00DBVR	A00_
–40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AHC1G00DCKR	AA_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INF	PUTS	OUTPUT
Α	В	Y
Н	Н	L
L	X	Н
Х	L	Н



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

SCLS313H - MARCH 1996 - REVISED JULY 2001

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sto</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{\text{IH}}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
	High-level input voltage  Low-level input voltage  Input voltage  Output voltage  High-level output current  Low-level output current	V <sub>CC</sub> = 5.5 V	3.85		
V <sub>I</sub> Input voltage	V <sub>CC</sub> = 2 V		0.5		
	Low-level input voltage V <sub>CC</sub> = 3 V	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
lOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		2 5.5 1.5 2.1 .85 0.5 0.9 1.65 0 5.5 0 VCC -50 -4 -8 50 4 8 100 20	ША
		V <sub>CC</sub> = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		$V_{CC} = 5 V \pm 0.5 V$		8	ША
Δt/Δν	Input transition rice or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	ns/V
ΔΨΔΨ	input transition rise or fail rate	$V_{CC} = 5 V \pm 0.5 V$		20	115/ V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	4 = 25°C	;	MIN	MAX	UNIT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	WAX	UNIT	
		2 V	1.9	2		1.9			
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9			
∨он		4.5 V	4.4	4.5		4.4		V	
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8			
	Ι <sub>ΟL</sub> = 50 μΑ	2 V			0.1		0.1		
		3 V			0.1		0.1		
VoL		4.5 V			0.1		0.1	V	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		
lı	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ	
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

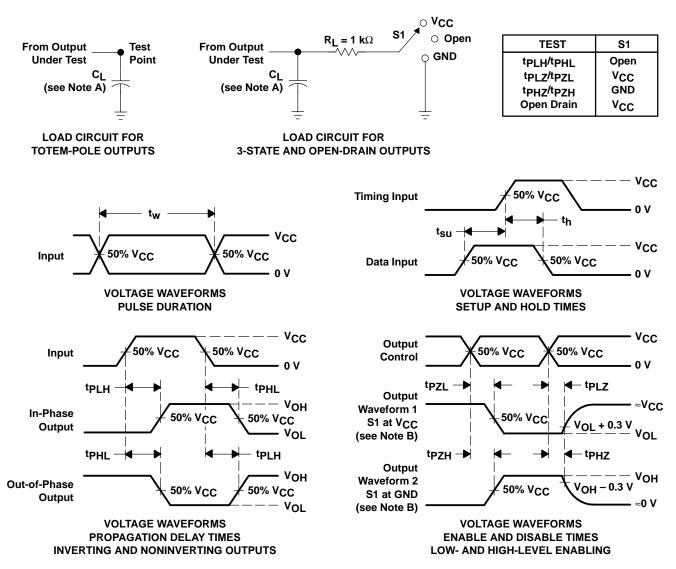
PARAMETER	FROM	то	LOAD	T,	չ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	ONII
<sup>t</sup> PLH	A or B	V	C <sub>L</sub> = 15 pF		5.5	7.9	1	9.5	no
t <sub>PHL</sub>	AUIB	Ť			5.5	7.9	1	9.5	ns
tPLH	A or D	V	Y C <sub>L</sub> = 50 pF		8	11.4	1	13	
tPHL	A or B	ĭ			8	11.4	1	13	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

	RAMETER	FROM	TO LOAD		T,	ղ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT	
	<sup>t</sup> PLH	A or P	V	C: _ 15 pF		3.7	5.5	1	6.5	no
	<sup>t</sup> PHL	A or B	Ť	C <sub>L</sub> = 15 pF		3.7	5.5	1	6.5	ns
	<sup>t</sup> PLH	A or B	V	C <sub>L</sub> = 50 pF		5.2	7.5	1	8.5	no
	<sup>t</sup> PHL	AUID	ſ			5.2	7.5	1	8.5	ns

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	9.5	pF



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### DBV OR DCK PACKAGE (TOP VIEW)



### description

This device contains a single 2-input NOR gate that performs the Boolean function  $Y = \overline{A} \bullet \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G02DBVR	A02_
–40°C to 85°C	SOP (SC-70) - DCK	Tape and reel	SN74AHC1G02DCKR	AB_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Y
Н	Х	L
Х	Н	L
L	L	Н

$$\begin{array}{c|c} A & \hline \\ B & \hline \end{array}$$

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
VCC	Supply voltage		2	5.5	V	
		V <sub>CC</sub> = 2 V	1.5			
$V_{\text{IH}}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V	
	digh-level input voltage	3.85				
		V <sub>CC</sub> = 2 V		0.5		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V	
V <sub>I</sub>		V <sub>CC</sub> = 5.5 V		1.65		
VI	Input voltage		0	5.5	V	
۷o	Output voltage		0	VCC	V	
		V <sub>CC</sub> = 2 V		-50	μΑ	
V <sub>O</sub>	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	^	
		$V_{CC} = 5 V \pm 0.5 V$		2 5.5 1.5 2.1 3.85 0.5 0.9 1.65 0 5.5 0 VCC -50	mA	
		V <sub>CC</sub> = 2 V		50	μΑ	
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A	
		V <sub>CC</sub> = 5 V ± 0.5 V		8	mA	
A # / A	land the selfine with an fall mate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	//	
Δt/Δν	input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20	ns/V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETED	TEST CONDITIONS	Vaa	T,	4 = 25°C	;	MINI	MAY	LINUT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	UNIT	
		2 V	1.9	2		1.9			
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9			
VOH		4.5 V	4.4	4.5		4.4		V	
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48			
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8			
	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1		
		3 V			0.1		0.1		
V <sub>OL</sub>		4.5 V			0.1		0.1	V	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		
Ι <sub>Ι</sub>	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μА	
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

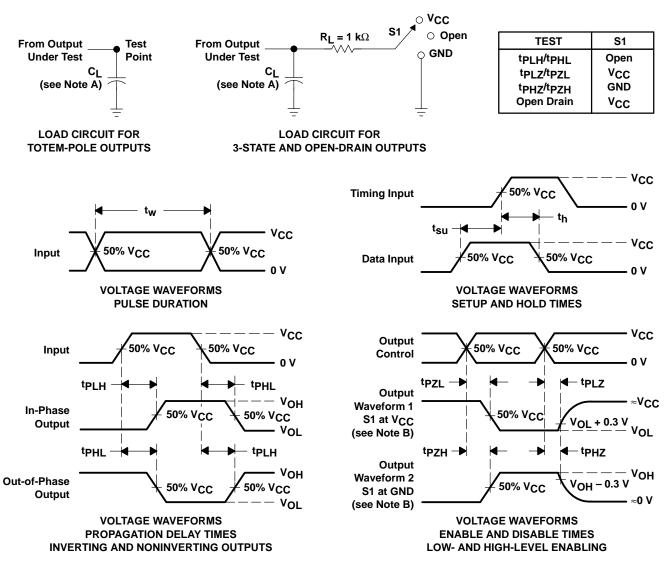
PARAMETER	FROM	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
	(INPUT)			MIN	TYP	MAX	IVIIIV	WAA	ONIT
<sup>t</sup> PLH	A or B	Y	C <sub>L</sub> = 15 pF		5.6	7.9	1	9.5	no
t <sub>PHL</sub>	AUIB				5.6	7.9	1	9.5	ns
t <sub>PLH</sub>	A or B	Υ	C <sub>L</sub> = 50 pF		8.1	11.4	1	13	no
<sup>t</sup> PHL	AUID				8.1	11.4	1	13	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

DAD	DAMETER	FROM	то	LOAD	T,	չ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT	
	<sup>t</sup> PLH	A or B	Y	C <sub>L</sub> = 15 pF		3.6	5.5	1	6.5	20
	tPHL	AUIB				3.6	5.5	1	6.5	ns
	<sup>t</sup> PLH	A or B	Y	C <sub>L</sub> = 50 pF		5.1	7.5	1	8.5	20
	tPHL	AUID				5.1	7.5	1	8.5	ns

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	15	pF



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

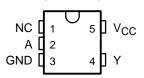


- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17

### description

The SN74AHC1G04 contains one inverter gate. The device performs the Boolean function  $Y = \overline{A}$ .

### DBV OR DCK PACKAGES (TOP VIEW)



NC - No internal connection

### **ORDERING INFORMATION**

TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡	
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G04DBVR	A04_	
-40 C 10 65 C	SOP (SC-70) – DCK	Tape and reel	SN74AHC1G04DCKR	AC_	

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н



<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

O and alternative V	0.51/1.71/
Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{ K }(V_{ I } < 0)$	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sto</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{\text{IH}}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
lOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA
		V <sub>CC</sub> = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		$V_{CC} = 5 V \pm 0.5 V$		8	IIIA
Δt/Δν	Input transition rice or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	ns/V
ΔΨΔΨ	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20	115/ V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	λ = 25°C	;	MIN	MAX	UNIT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	WAX	UNIT	
		2 V	1.9	2		1.9			
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9			
∨он		4.5 V	4.4	4.5		4.4		V	
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48			
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8			
		2 V			0.1		0.1		
	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1		
VOL		4.5 V			0.1		0.1	V	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	1	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		
lį	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

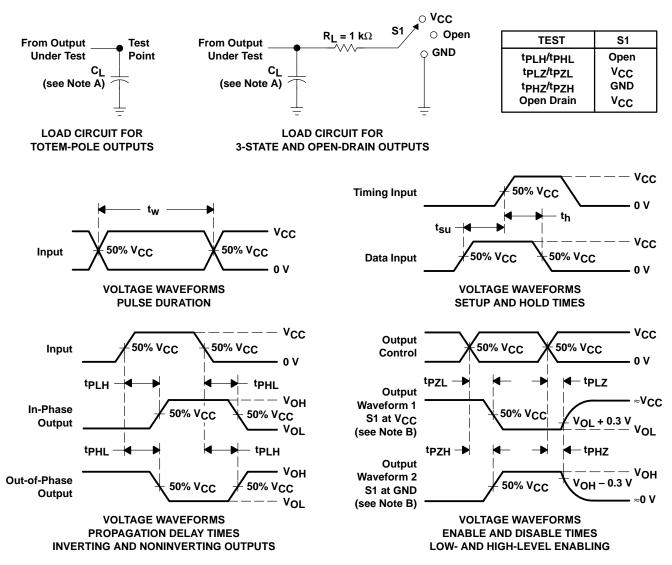
PARAMETER	FROM	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
	(INPUT)			MIN	TYP	MAX	IVIIIV	WAA	ONII
<sup>t</sup> PLH	۸	A Y	C <sub>L</sub> = 15 pF		5	8.9	1	10.5	no
tPHL	A				5	8.9	1	10.5	ns
tPLH	Δ.	Y	C <sub>L</sub> = 50 pF		7.5	11.4	1	13	20
tPHL	А				7.5	11.4	1	13	ns

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
t <sub>PLH</sub>	_	V	C <sub>L</sub> = 15 pF		3.8	5.5	1	6.5	20
t <sub>PHL</sub>	A	ĭ			3.8	5.5	1	6.5	ns
t <sub>PLH</sub>	_	V	V 0 50 5		5.3	7.5	1	8.5	20
t <sub>PHL</sub>	A	Y C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	ns	

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	12	pF



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- **Unbuffered Output**
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### **DBV OR DCK PACKAGE** (TOP VIEW) NC Vcc АΓ GND

NC - No internal connection

### description

The SN74AHC1GU04 contains a single inverter gate. The device performs the Boolean function  $Y = \overline{A}$ . Internal circuitry consists of a single-stage inverter that can be used in analog applications, such as crystal oscillators.

### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1GU04DBVR	U04_
-40°C to 85°C	SOP (SC-70) - DCK	Tape and reel	SN74AHC1GU04DCKR	AD_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.7		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.4		V
VIH VIL VI		V <sub>CC</sub> = 5.5 V	4.4		
		V <sub>CC</sub> = 2 V		0.3	
$V_{IL}$	Low-level input voltage $ \frac{\text{V}_{\text{CC}} = 3 \text{ V}}{\text{V}_{\text{CC}} = 5.5 \text{ V}} $	V <sub>CC</sub> = 3 V		0.6	V
		V <sub>CC</sub> = 5.5 V		1.1	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
$I_{OH}$	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	MA
		V <sub>CC</sub> = 2 V		50	μΑ
IOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		8	IIIA
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	գ = 25°C	;	MIN	MAX	UNIT	
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	WAX	UNII	
		2 V	1.8	2		1.8			
	I <sub>OH</sub> = -50 μA	3 V	2.7	3		2.7			
∨он		4.5 V	4	4.5		4		V	
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		1	
	ΙΟL = 50 μΑ	2 V			0.2		0.2		
		3 V			0.3		0.3		
VoL		4.5 V			0.5		0.5	V	
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44		
	$VOH \begin{tabular}{lllllllllllllllllllllllllllllllllll$	0.44							
Ι <sub>Ι</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ	
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}=3.3~V\pm0.3~V$ (unless otherwise noted) (see Figure 1)

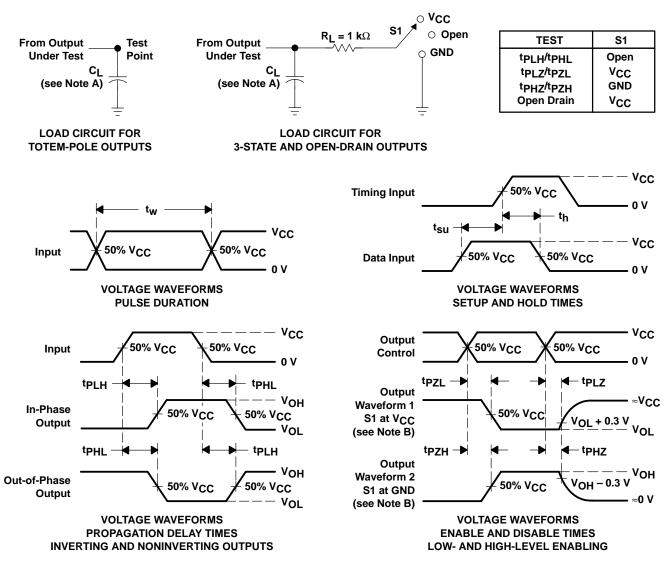
PARAMETER	FROM	то	то оитрит		T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	JTPUT) CAPACITANCE	MIN	TYP	MAX	IVIIIN	WAA	ONII	
tPLH	^	Y	C <sub>L</sub> = 15 pF		5	7.1	1	8.5	20	
t <sub>PHL</sub>	A				5	7.1	1	8.5	ns	
<sup>t</sup> PLH	^	Y	C <sub>L</sub> = 50 pF		7.5	10.6	1	12	20	
tPHL	Α				7.5	10.6	1	12	ns	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V\pm0.5~V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то оитрит		T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)	PUT) (OUTPUT)	CAPACITANCE	MIN	TYP	MAX	]	IVIAA	CIVIT
tpLH	^	Y	Y C <sub>L</sub> = 15 pF		3.5	5.5	1	6	20
tpHL	А				3.5	5.5	1	6	ns
tpLH	^	· ·	0 50 - 5		5	7	1	8	no
tPHL	tPHL A Y	$C_L = 50 \text{ pF}$		5	7	1	8	ns	

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST CONDITIONS		UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	7.3	pF



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 

### description

The SN74AHC1G08 is a single 2-input positive-AND gate. The device performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

### **ORDERING INFORMATION**

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G08DBVR	A08_
	SOP (SC-70) – DCK	Tape and reel	SN74AHC1G08DCKR	AE_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

ı	INP	UTS	OUTPUT
	Α	В	Υ
	Н	Н	Н
	L	X	L
	Х	L	L





<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sta</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT	
Vcc	Supply voltage		2	5.5	V	
		V <sub>CC</sub> = 2 V	1.5			
$V_{\text{IH}}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V	
		V <sub>CC</sub> = 5.5 V	3.85			
		V <sub>CC</sub> = 2 V		0.5		
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V	
		V <sub>CC</sub> = 5.5 V		1.65		
٧ <sub>I</sub>	Input voltage		0	5.5	V	
٧o	Output voltage		0	VCC	V	
		V <sub>CC</sub> = 2 V		-50	μΑ	
lOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA	
		$V_{CC} = 5 V \pm 0.5 V$		-8	ША	
		V <sub>CC</sub> = 2 V		50	μΑ	
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			mA	
		$V_{CC} = 5 V \pm 0.5 V$		8	ША	
Δt/Δν	Input transition rice or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	ns/V	
ΔΨΔΨ	Input transition rise or fall rate	$V_{CC} = 5 V \pm 0.5 V$		20	115/ V	
TA	Operating free-air temperature		-40	85	°C	

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	IVIIIV	WAX	UNII	
		2 V	1.9	2		1.9		V	
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9			
∨он		4.5 V	4.4	4.5		4.4			
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8			
	I <sub>OL</sub> = 50 μA	2 V			0.1		0.1	V	
		3 V			0.1		0.1		
VoL		4.5 V			0.1		0.1		
		3 V			0.36		0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44		
Ι <sub>Ι</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ	
Ci	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

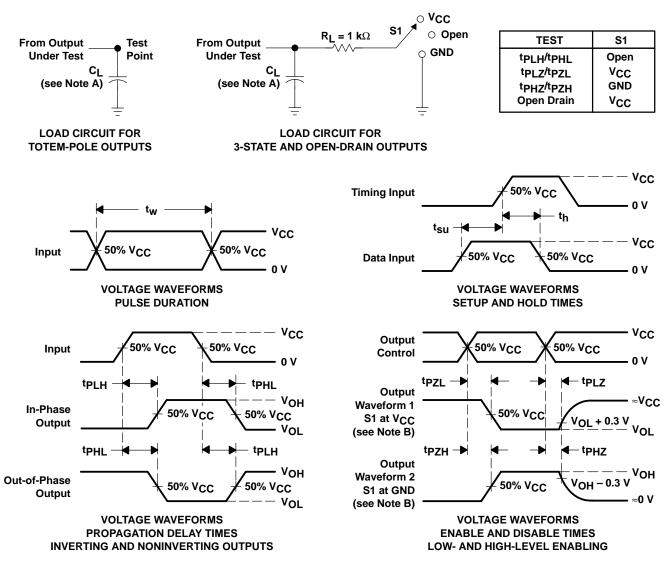
PARAMETER	FROM	то	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)		MIN	TYP	MAX	IVIIIN	WAA	UNIT	
<sup>t</sup> PLH	A or B	V	$C_1 = 15  pF$		6.2	8.8	1	10.5	ne	
<sup>t</sup> PHL	AUIB	ı	OL = 15 pr		6.2	8.8	1	10.5	ns	
<sup>t</sup> PLH	A or B Y	Y	C. F0.pF	0 50 = 5		8.7	12.3	1	14	20
t <sub>PHL</sub>			Y	Ť	C <sub>L</sub> = 50 pF		8.7	12.3	1	14

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	OUTPUT CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)		MIN	TYP	MAX	IVIIIN	WAX	ONT
<sup>t</sup> PLH	A or B	V	C: _ 15 pF		4.3	5.9	1	7	20
<sup>t</sup> PHL	AUID	Ť	C <sub>L</sub> = 15 pF		4.3	5.9	1	7	ns
<sup>t</sup> PLH	A or B	Y	V C 50 nF		5.8	7.9	1	9	20
<sup>t</sup> PHL	AUIB			5.8	7.9	1	9	ns	

### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	18	pF



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17

### description

The SN74AHC1G14 contains one inverter gate. The device performs the Boolean function  $Y = \overline{A}$ .

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive-  $(V_{T+})$  and negative-going  $(V_{T-})$  signals.

# DBV OR DCK PACKAGE (TOP VIEW) NC 1 5 VCC A 2 GND 3 4 Y

NC - No internal connection

### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		PACKAGET ORDERABLE PART NUMBER	
–40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G14DBVR	A14_
-40 C 10 65°C	SOP (SC-70) – DCK	Tape and reel	SN74AHC1G14DCKR	AF_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2	5.5	V
٧ı	Input voltage		0	5.5	V
Vo	Output voltage		0	VCC	V
	V	CC = 2 V		-50	μΑ
IOH	High-level output current	CC = 3.3 V ± 0.3 V		-4	mA
	V	CC = 5 V ± 0.5 V		-8	IIIA
	V	CC = 2 V		50	μΑ
lOL	Low-level output current	CC = 3.3 V ± 0.3 V		4	mA
	V	CC = 5 V ± 0.5 V		8	IIIA
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	4 = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	WAX	Olviii
V <sub>T+</sub>		3 V	1.2		2.2	1.2	2.2	
Positive-going		4.5 V	1.75		3.15	1.75	3.15	V
input threshold voltage		5.5 V	2.15		3.85	2.15	3.85	
V <sub>T</sub> _		3 V	0.9		1.9	0.9	1.9	
Negative-going		4.5 V	1.35		2.75	1.35	2.75	V
input threshold voltage		5.5 V	1.65		3.35	1.65	3.35	
$\Delta V_T$ Hysteresis ( $V_{T+} - V_{T-}$ )		3 V	0.3		1.2	0.3	1.2	
		4.5 V	0.4		1.4	0.4	1.4	V
		5.5 V	0.5		1.6	0.5	1.6	
		2 V	1.9	2		1.9		
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		
VOH		4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1	
V <sub>OL</sub>		4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
lį	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT	
t <sub>PLH</sub>	۸	V	C <sub>L</sub> = 15 pF		8.3	12.8	1	15	ne	
<sup>t</sup> PHL	А	ī			8.3	12.8	1	15	ns	
<sup>t</sup> PLH	۸	Υ	C: _ 50 pE		10.8	16.3	1	18.5	no	
<sup>t</sup> PHL	A		Y	A Y	C <sub>L</sub> = 50 pF		10.8	16.3	1	18.5

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

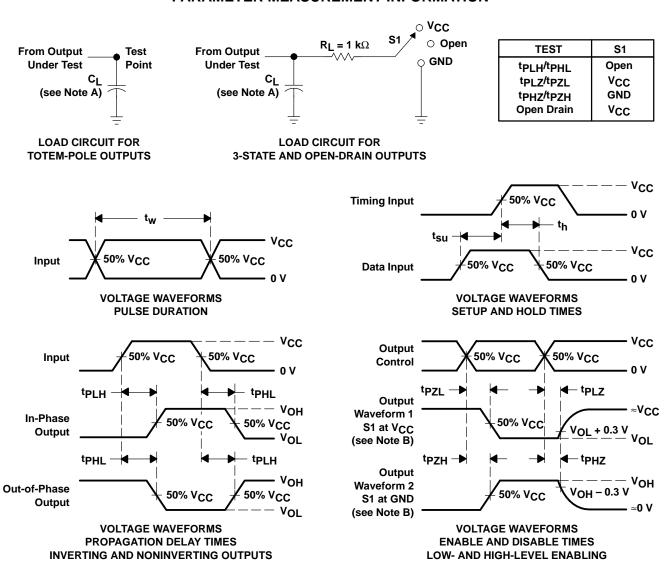
PARAMETER	FROM	то	LOAD	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
tPLH	۸	V	C: 15 pF		5.5	8.6	1	10	20
t <sub>PHL</sub>	A	ī	C <sub>L</sub> = 15 pF		5.5	8.6	1	10	ns
t <sub>PLH</sub>	^	V	C: F0 = F		7	10.6	1	12	20
tpHL	А	ĭ	C <sub>L</sub> = 50 pF		7	10.6	1	12	ns

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#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	9	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

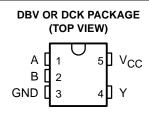
Figure 1. Load Circuit and Voltage Waveforms



- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17

#### description

The SN74AHC1G32 is a single 2-input positive-OR gate. The device performs the Boolean function Y = A + B or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.



#### **ORDERING INFORMATION**

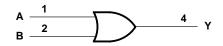
TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G32DBVR	A32_
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AHC1G32DCKR	AG_

<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

IN	PUTS	OUTPUT
Α	В	Υ
Н	Х	Н
Х	Н	Н
L	L	L

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
Vcc	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
	Input voltage	V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
VO	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
IOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	ША
		V <sub>CC</sub> = 2 V		50	μΑ
IOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		8	ША
A+/A>,	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	ns/V
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20 ns/\	
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	գ = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN		UNIT
		2 V	1.9	2		1.9		
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		
∨он		4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1	
VoL		4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
lı	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

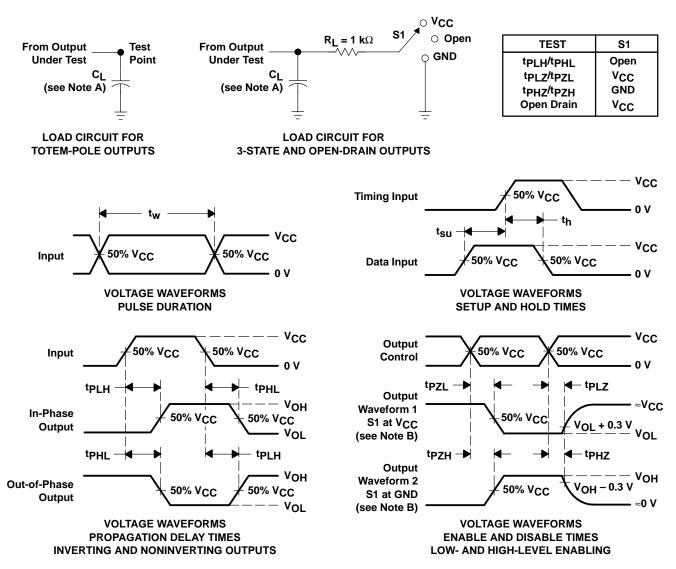
PARAMETER	FROM TO L		LOAD	T <sub>A</sub> = 25°C			MIN	MAX	UNIT				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	WAX	UNIT				
<sup>t</sup> PLH	A or B	Y	C: 15 pF	C: 15 pF		5.5	7.9	1	9.5	20			
tPHL	AUID		C <sub>L</sub> = 15 pF		5.5	7.9	1	9.5	ns				
<sup>t</sup> PLH	A or P	Y	Y	Y	Y	Y	A or B $\qquad \qquad $		8	11.4	1	13	20
tPHL	AUID							CL = 50 pr		8	11.4	1	13

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO LOAD		T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	(OUTPUT) CAPACITANCE		TYP	MAX	IVIIIN	IVIAA	UNIT	
t <sub>PLH</sub>	A or B	V	C <sub>I</sub> = 15 pF		3.8	5.5	1	6.5	ns	
tpHL	AOIB	ı	CL = 15 pr	OL = 15 pi		3.8	5.5	1	6.5	115
t <sub>PLH</sub>	A or B	V	$C_{1} = 50 \text{ pF}$		5.3	7.5	1	8.5	ns	
<sup>t</sup> PHL	AOIB	ı	OL = 30 pr		5.3	7.5	1	8.5	115	

#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		TEST C	ONDITIONS	TYP	UNIT
ſ	C <sub>pd</sub> Power dissipation capacitance		No load,	f = 1 MHz	14	pF



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# DBV OR DCK PACKAGE (TOP VIEW) A [ 1 5 ] V<sub>CC</sub> B [ 2 4 ] Y

#### description

The SN74AHC1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{AB} + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

#### ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G86DBVR	A86_
-40 C to 65 C	SOP (SC-70) – DCK	Tape and reel	SN74AHC1G86DCKR	AH_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	JTS	OUTPUT
Α	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

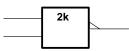
## 

These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86 gate in positive logic; negation may be shown at any two ports.

## 

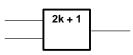
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

#### **EVEN-PARITY ELEMENT**



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

#### **ODD-PARITY ELEMENT**



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ Input voltage range, $V_{I}$ (see Note 1) Output voltage range, $V_{O}$ (see Note 1) Input clamp current, $I_{IK}$ ( $V_{I}$ < 0) Output clamp current, $I_{OK}$ ( $V_{O}$ < 0 or $V_{O}$ > $V_{CC}$ ) Continuous output current, $I_{O}$ ( $V_{O}$ = 0 to $V_{CC}$ ) Continuous current through $V_{CC}$ or GND	$\begin{array}{llllllllllllllllllllllllllllllllllll$
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	
DCK package  Storage temperature range, T <sub>stq</sub>	
ullet	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{\text{IH}}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
loh	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	IIIA
		V <sub>CC</sub> = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	A
		$V_{CC} = 5 V \pm 0.5 V$		8	mA
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	ns/V
ΔυΔν	Input transition rise or fall rate	$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		20	HS/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	ղ = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	IVIIIV	IVIAA	UNII
		2 V	1.9	2		1.9		
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		
VOH		4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1	
VoL		4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
l <sub>l</sub>	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Ci	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

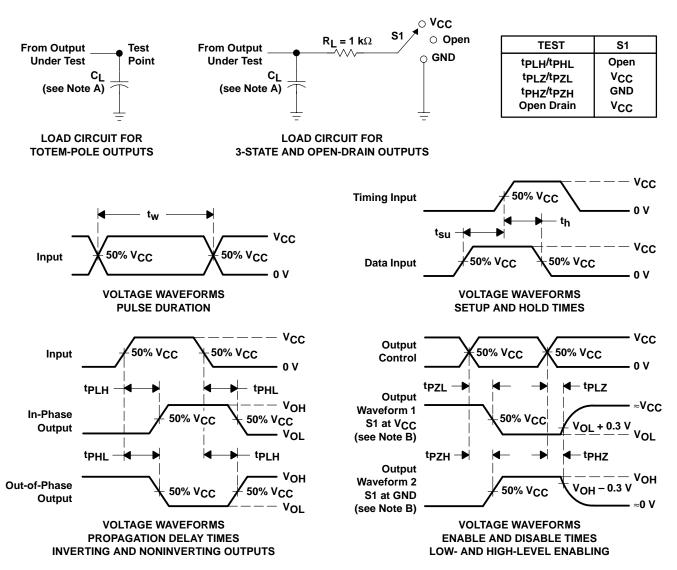
PARAMETER	FROM	то	LOAD		λ = 25°C	;	MIN	MAX	UNIT											
PARAMETER	(INPUT)	(OUTPUT) CAPACITANCE		MIN	TYP	MAX	IVIIIV	IVIAA	ONII											
<sup>t</sup> PLH	A or B	V	C: _ 15 pF		7	11	1	13	no											
t <sub>PHL</sub>	AUIB	I	I	ı	1	'	'	ı	'		1 OL = 13 P	$C_L = 15 pF$	о[ – 13 рі	OL = 19 pi		7	11	1	13	ns
<sup>t</sup> PLH	A or P	V	C: _ 50 pF		9.5	14.5	1	16.5	no											
t <sub>PHL</sub>	A or B	ſ	C <sub>L</sub> = 50 pF		9.5	14.5	1	16.5	ns											

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD		λ = 25°C	;	MIN	MAX	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
<sup>t</sup> PLH	A or B	V	C: _ 15 pF		4.8	6.8	1	8	no
tPHL	AUID	ī	C <sub>L</sub> = 15 pF		4.8	6.8	1	8	ns
<sup>t</sup> PLH	A or B	V	C: _ 50 pF		6.3	8.8	1	10	no
t <sub>PHL</sub>	AUIB	ī	C <sub>L</sub> = 50 pF		6.3	8.8	1	10	ns

#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CO	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	18	pF



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

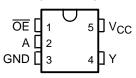
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#### Operating Range 2-V to 5.5-V V<sub>CC</sub>

#### description

The SN74AHC1G125 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable  $(\overline{OE})$  input is high. When  $\overline{OE}$  is low, true data is passed from the A input to the Y output.

### DBV OR DCK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### **ORDERING INFORMATION**

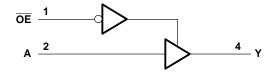
TA	PACKAGET		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G125DBVR	A25_
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AHC1G125DCKR	AM_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPU	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
lOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	mA
		$V_{CC} = 5 V \pm 0.5 V$		-8	ША
		V <sub>CC</sub> = 2 V		50	μΑ
IOL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mΛ
		$V_{CC} = 5 V \pm 0.5 V$	8		mA
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		100	ns/V
Δι/Δν	input transition rise or fail rate	$V_{CC} = 5 V \pm 0.5 V$		20	115/ V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vas	T,	4 = 25°C	;	MINI	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN		UNIT
		2 V	1.9	2		1.9		
	$I_{OH} = -50 \mu A$	3 V	2.9	3		2.9		
Voн		4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	I <sub>OL</sub> = 50 μA	3 V			0.1		0.1	
V <sub>OL</sub>		4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
loz	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF
Co	$V_O = V_{CC}$ or GND	5 V		10				pF

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	TA	= 25°C		MIN	MAX	UNIT												
PARAWETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT												
<sup>t</sup> PLH	А	Υ	C <sub>L</sub> = 15 pF		5.6	8	1	9.5	ns												
<sup>t</sup> PHL	A	ı	OL = 15 pr		5.6	8	1	9.5	110												
<sup>t</sup> PZH	ŌĒ	Υ	C <sub>I</sub> = 15 pF		5.4	8	1	9.5	ns												
<sup>t</sup> PZL	OE	ı	C[ = 15 pr		5.4	8	1	9.5	115												
<sup>t</sup> PHZ	ŌĒ	Υ	C <sub>L</sub> = 15 pF		7	9.7	1	11.5	ns												
<sup>t</sup> PLZ	OE	1	ı	ı	ı	ı	1	•	ı	•	•		•	ı	CL = 15 pr		7	9.7	1	11.5	115
<sup>t</sup> PLH	А	Y	C <sub>I</sub> = 50 pF		8.1	11.5	1	13	ns												
<sup>t</sup> PHL	A	, OL-	CL = 50 pr	OL = 30 bi	о_ = 30 рі	OL = 30 pi		8.1	11.5	1	13	110									
<sup>t</sup> PZH	ŌĒ	Y	C <sub>L</sub> = 50 pF		7.9	11.5	1	13	ns												
tPZL	OE	ī	OL = 50 pr		7.9	11.5	1	13	110												
<sup>t</sup> PHZ	ŌĒ	Y	C <sub>L</sub> = 50 pF		9.5	13.2	1	15	no												
t <sub>PLZ</sub>	OE .	ſ	CL = 50 pr		9.5	13.2	1	15	ns												

#### SN74AHC1G125 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

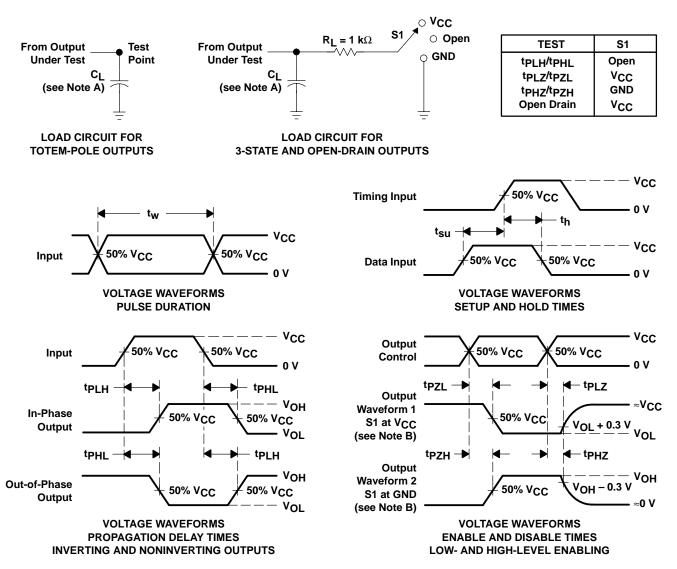
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## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	FROM TO LOAD TA = 25°C		;	MIN	MAV	UNIT																				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	MAX	UNIT																		
<sup>t</sup> PLH	۸	Υ	C <sub>I</sub> = 15 pF		3.8	5.5	1	6.5	ns																		
<sup>t</sup> PHL	Α	ı	OL = 13 pr		3.8	5.5	1	6.5	115																		
<sup>t</sup> PZH	ŌĒ	Y	C <sub>L</sub> = 15 pF		3.6	5.1	1	6	ns																		
t <sub>PZL</sub>	OE	ı	CL = 15 pr		3.6	5.1	1	6	115																		
<sup>t</sup> PHZ	ŌĒ	Y	C <sub>L</sub> = 15 pF		4.6	6.8	1	8	ns																		
<sup>t</sup> PLZ	OE	ī	OL = 15 pr		4.6	6.8	1	8	115																		
<sup>t</sup> PLH	А	Y	C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	no																		
<sup>t</sup> PHL	A	ī	OL = 50 pr		5.3	7.5	1	8.5	ns																		
<sup>t</sup> PZH	ŌĒ	Y	C: - 50 pF		5.1	7.1	1	8	20																		
<sup>t</sup> PZL	OE	Ť	ī	ī		ī	ř	Ť	Ĭ	ď	Ť	Ť	ĭ	Ť	Ť	Ť	Ĭ	Ť	Y	Y CL = 5	C <sub>L</sub> = 50 pF		5.1	7.1	1	8	ns
<sup>t</sup> PHZ	ŌĒ	Y	C: - 50 pF		6.1	8.8	1	10	ns																		
tPLZ	OE .	ſ	$C_L = 50 pF$		6.1	8.8	1	10	115																		

#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	14	pF



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Operating Range 2-V to 5.5-V V<sub>CC</sub>
- Latch-Up Performance Exceeds 250 mA Per JESD 17

#### description

The SN74AHC1G126 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

OE 1 5 VCC

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### **ORDERING INFORMATION**

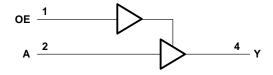
TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHC1G126DBVR	A26_
-40 C to 65 C	SOP (SC-70) - DCK	Tape and reel	SN74AHC1G126DCKR	AN_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	JTS	OUTPUT
OE	Α	Υ
Н	Н	Н
Н	L	L
L	Χ	Z

#### logic diagram (positive logic)





<sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sto</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  - 2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
VCC	Supply voltage		2	5.5	V
		V <sub>CC</sub> = 2 V	1.5		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 3 V	2.1		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 2 V		0.5	
$V_{IL}$	Low-level input voltage	V <sub>CC</sub> = 3 V		0.9	V
		V <sub>CC</sub> = 5.5 V		1.65	
٧ <sub>I</sub>	Input voltage		0	5.5	V
٧o	Output voltage		0	VCC	V
		V <sub>CC</sub> = 2 V		-50	μΑ
IOH	High-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		-4	A
		$V_{CC} = 5 V \pm 0.5 V$		-8	mA
		V <sub>CC</sub> = 2 V		50	μΑ
loL	Low-level output current	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		4	mA
		$V_{CC} = 5 V \pm 0.5 V$		8	MA
A+/A.,	lanut transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	20/1
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 5 V ± 0.5 V		20	ns/V
TA	Operating free-air temperature		-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	4 = 25°C	;	MINI	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN		UNIT
		2 V	1.9	2		1.9		
	I <sub>OH</sub> = -50 μA	3 V	2.9	3		2.9		
Voн		4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
		2 V			0.1		0.1	
	$I_{OL} = 50 \mu A$	3 V			0.1		0.1	
V <sub>OL</sub>		4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 4 mA	3 V			0.36		0.44	
	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
loz	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Ci	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		10	pF
Co	$V_O = V_{CC}$ or GND	5 V		10				pF

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	TΔ	_ = 25°C	;	MIN	MAX	UNIT													
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT													
tPLH	А	Y	C <sub>L</sub> = 15 pF		5.6	8	1	9.5	ns													
<sup>t</sup> PHL	٨	ı	OL = 15 pr		5.6	8	1	9.5	115													
<sup>t</sup> PZH	OE	Υ	C: _ 15 pE		5.4	8	1	9.5	ns													
tpZL	OE	ı	$C_L = 15 pF$	CL = 15 pr		5.4	8	1	9.5	115												
<sup>t</sup> PHZ	OE	V	C <sub>L</sub> = 15 pF		7	9.7	1	11.5	no													
<sup>t</sup> PLZ	OL	Y	1	I	ı	ı	ı	'	'	1	ı	ı	•	•	•	OL = 15 pr		7	9.7	1	11.5	ns
t <sub>PLH</sub>	А	Y	C <sub>I</sub> = 50 pF		8.1	11.5	1	13	ne													
t <sub>PHL</sub>	A	ť	ſ	Ĭ	Ĭ	r C	1 CL = 50 pF		8.1	11.5	1	13	ns									
<sup>t</sup> PZH	OE	Υ	C <sub>L</sub> = 50 pF		7.9	11.5	1	13	ns													
t <sub>PZL</sub>	OE	ĭ	ī	ı	ı	ı	1 CL = 50 pr	OE   1		7.9	11.5	1	13	115								
<sup>t</sup> PHZ	OE	V	C: - 50 pF		9.5	13.2	1	15	ns													
t <sub>PLZ</sub>	OL .	Y	Y	Y	Y C <sub>L</sub> = 50 pF		9.5	13.2	1	15	115											

#### SN74AHC1G126 SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

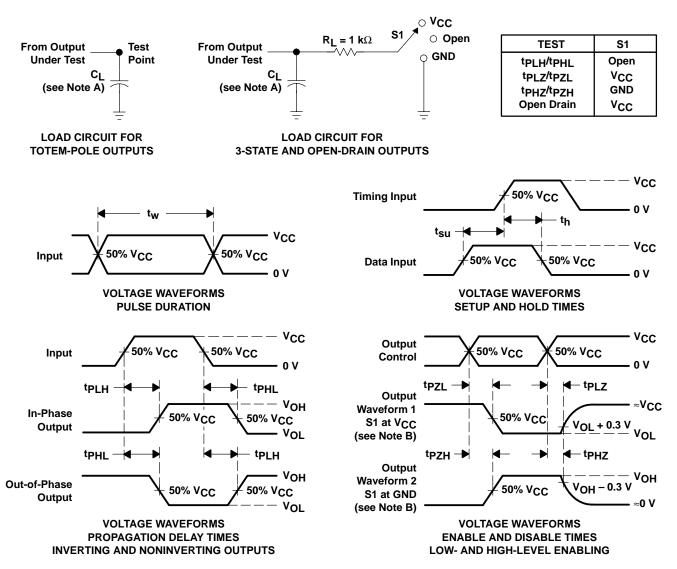
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## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	չ = 25°C	;	MIN	MAX	UNIT								
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	WAX	UNIT								
<sup>t</sup> PLH	А	Υ	C <sub>I</sub> = 15 pF		3.8	5.5	1	6.5	ns								
t <sub>PHL</sub>	٨	•	OL = 13 pr		3.8	5.5	1	6.5	115								
<sup>t</sup> PZH	OE	Υ	C <sub>L</sub> = 15 pF		3.6	5.1	1	6	ns								
t <sub>PZL</sub>	OE	1	ı	1	ı	ı	1	ſ	T	1	OL = 13 pr		3.6	5.1	1	6	115
<sup>t</sup> PHZ	OE	V	Y C <sub>L</sub> = 15 pF		4.6	6.8	1	8	ns								
<sup>t</sup> PLZ		'	OL = 13 pr		4.6	6.8	1	8	115								
<sup>t</sup> PLH		Y	C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	no								
<sup>t</sup> PHL	А	ī	OL = 50 pr		5.3	7.5	1	8.5	ns								
<sup>t</sup> PZH	OE	Y	C <sub>L</sub> = 50 pF		5.1	7.1	1	8	no								
<sup>t</sup> PZL		ī	OL = 50 pr		5.1	7.1	1	8	ns								
<sup>t</sup> PHZ	OE	Y	C: - 50 pF		6.1	8.8	1	10	nc								
tPLZ	) DE	ſ	C <sub>L</sub> = 50 pF		6.1	8.8	1	10	ns								

#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	14	pF



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_f \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DBV OR DCK PACKAGE (TOP VIEW) A 1 5 VCC B 2 GND 3 4 Y

#### description

The SN74AHCT1G00 performs the Boolean function  $Y = \overline{A \cdot B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### **ORDERING INFORMATION**

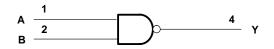
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G00DBVR	B00_
–40°C to 85°C	SOP (SC-70) - DCK	Tape and reel	SN74AHCT1G00DCKR	BA_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

	INPUT	OUTPUT	
	4	В	Y
	1	Н	L
	L	Х	Н
)	X	L	Н

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
ІОН	High-level output current		-8	mA
l <sub>OL</sub>	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
Vou	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		· v
VOH	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
\/-·	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1	V
VOL	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	
lj	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
∆l <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

 $<sup>\</sup>ddagger$  This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74AHCT1G00 SINGLE 2-INPUT POSITIVE-NAND GATE

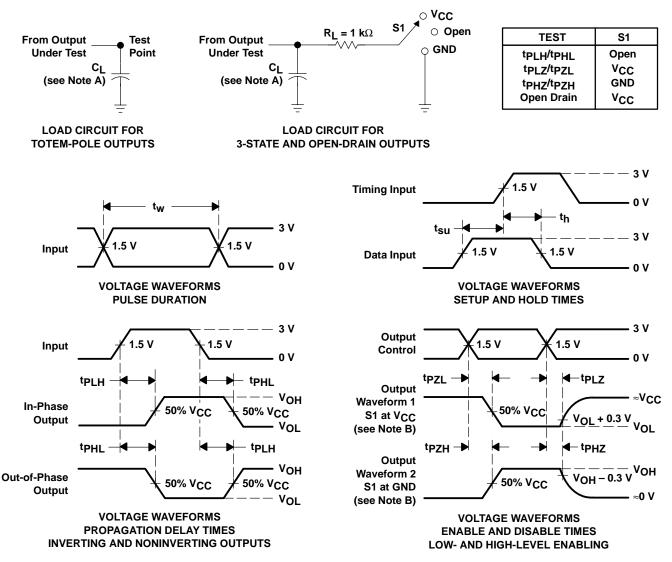
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## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	չ = 25°C	;	MIN	MAX	UNIT				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	ONII				
<sup>t</sup> PLH	A or B	Y	V	C: _ 15 pE		5	6.2	1	7.1	no			
t <sub>PHL</sub>			C <sub>L</sub> = 15 pF		5	6.2	1	7.1	ns				
<sup>t</sup> PLH	A or B Y	V	C: _ 50 pF		5.5	7.9	1	9	no				
tPHL		Y	ř	Ť	Ť	Ť	Y	C <sub>L</sub> = 50 pF		5.5	7.9	1	9

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load, f = 1 MHz	10.5	pF



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 3$  ns,  $t_f \leq 3$  ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

# DBV OR DCK PACKAGE (TOP VIEW) A 1 5 V<sub>CC</sub> B 2 GND 3 4 Y

#### description

This device contains a single 2-input NOR gate that performs the Boolean function  $Y = \overline{A} \bullet \overline{B}$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

#### ORDERING INFORMATION

TA	PACKAGI	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G02DBVR	B02_
-40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AHCT1G02DCKR	BB_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

### FUNCTION TABLE (each gate)

ĺ	INP	JTS	OUTPUT
I	Α	В	Y
ĺ	Н	Х	L
ı	Χ	Н	L
I	L	L	Н

#### logic diagram (positive logic)





<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	٧
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
ЮН	High-level output current		-8	mA
lOL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	<u> </u> = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT
Vou	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		V
Voн	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
\/o.	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1	V
VOL	$I_{OL} = 8 \text{ mA}$	4.5 V	+.5 V	0.36		0.44	V	
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
ΔlCC <sup>‡</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

<sup>‡</sup>This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74AHCT1G02 SINGLE 2-INPUT POSITIVE-NOR GATE

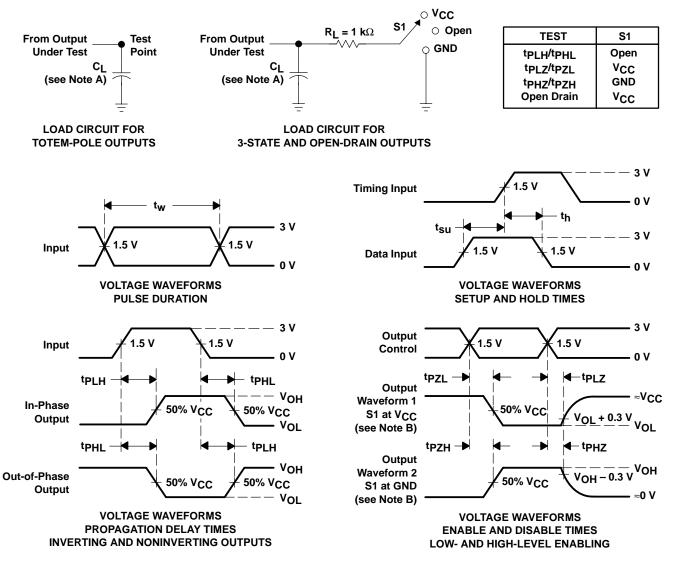
SCLS341I - APRIL 1996 - REVISED JULY 2001

## switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V\pm0.5~V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM TO LOAD		<b>T</b> <sub>A</sub> = 25°C			MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT
<sup>t</sup> PLH	A or B	Υ	C <sub>L</sub> = 15 pF		2.4	5.5	1	6.5	20
t <sub>PHL</sub>					3.5	5.5	1	6.5	ns
<sup>t</sup> PLH	A = = D	V	C <sub>L</sub> = 50 pF		3.4	7.5	1	8.5	20
tPHL	A or B	I			4.5	7.5	1	8.5	ns

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

PARAMETER		TEST C	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	17	pF



NOTES: A. C<sub>I</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

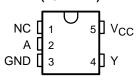


- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

#### description

The SN74AHCT1G04 contains one gate. The device performs the Boolean function  $Y = \overline{A}$ .

### DBV OR DCK PACKAGE (TOP VIEW)



NC - No internal connection

#### **ORDERING INFORMATION**

TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G04DBVR	B04_
-40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AHCT1G04DCKR	BC_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPUT A	OUTPUT Y
Н	L
L	Н

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

SCLS319L - MARCH 1996 - REVISED OCTOBER 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>sto</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	٧
VIH	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
ЮН	High-level output current		-8	mA
lOL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vac	T,	<b>Վ</b> = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	WAA	UNIT
Vari	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		· v
VOH	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
Val	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
VOL	$I_{OL} = 8 \text{ mA}$				0.36		0.44	V
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Δl <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
Ci	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

 $<sup>\</sup>ddagger$  This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

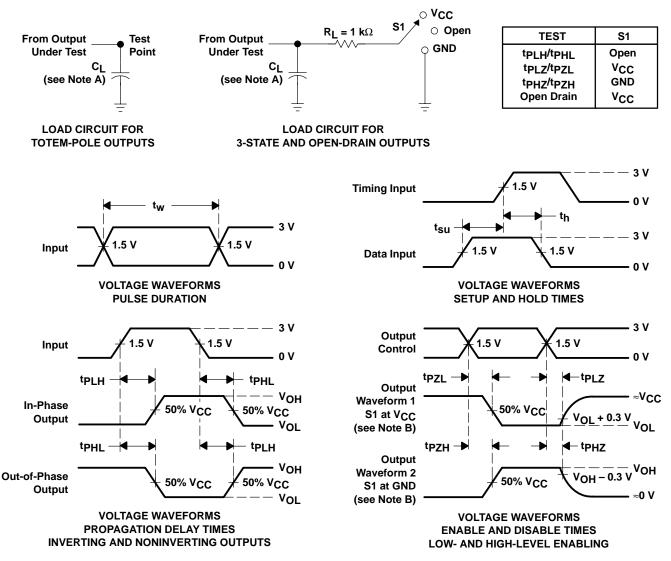
SCLS319L - MARCH 1996 - REVISED OCTOBER 2001

## switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V\pm0.5~V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	LOAD	LOAD T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	(INPUT)		CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	CINIT
t <sub>PLH</sub>	^	Y	C <sub>L</sub> = 15 pF		4.7	6.7	1	7.5	20
t <sub>PHL</sub>	A				4.7	6.7	1	7.5	ns
<sup>t</sup> PLH	^	V	C <sub>L</sub> = 50 pF		5.5	7.7	1	8.5	20
t <sub>PHL</sub>	A	ı			5.5	7.7	1	8.5	ns

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	14	pF



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns.  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



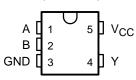
SCLS315K - MARCH 1996 - REVISED AUGUST 2001

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

#### description

The SN74AHCT1G08 is a single 2-input positive-AND gate. The device performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{\overline{A} + \overline{B}}$  in positive logic.

### DBV OR DCK PACKAGE (TOP VIEW)



#### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G08DBVR	B08_
	SOP (SC-70) - DCK	Tape and reel	SN74AHCT1G08DCKR	BE_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	UTS	OUTPUT
Α	В	Υ
Н	Н	Н
L	X	L
Х	L	L

#### logic diagram (positive logic)





<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

SCLS315K - MARCH 1996 - REVISED AUGUST 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
٧ <sub>IH</sub>	High-level input voltage	2		V
VIL	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
ІОН	High-level output current		-8	mA
l <sub>OL</sub>	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT
Vari	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		V
Voн	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		٧
Vol	$I_{OL} = 50 \mu A$				0.1		0.1	V
V <sub>OL</sub>	I <sub>OL</sub> = 8 mA		0.44	'				
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
∆l <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

 $<sup>\</sup>ddagger$  This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74AHCT1G08 SINGLE 2-INPUT POSITIVE-AND GATE

SCLS315K - MARCH 1996 - REVISED AUGUST 2001

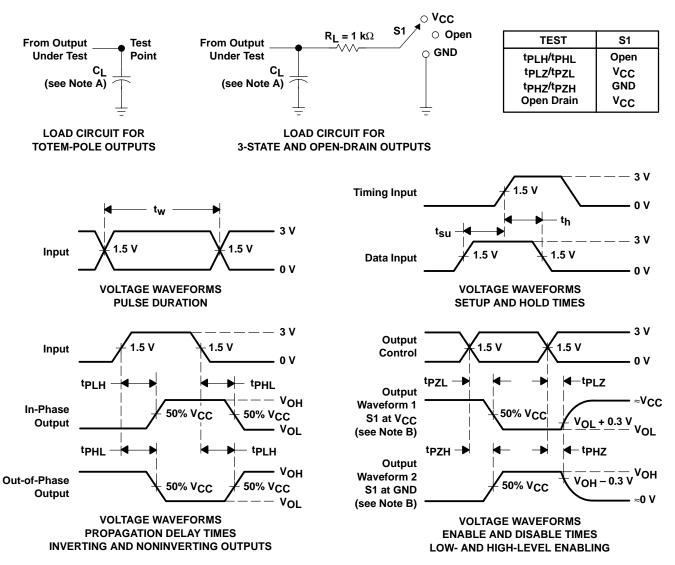
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	չ = 25°C	;	MIN	MAX	UNIT	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIV	IVIAA	CIVII	
<sup>t</sup> PLH	A or P	Y	Y		5	6.2	1	7.1	no	
t <sub>PHL</sub>	A or B				5	6.2	1	7.1	ns	
<sup>t</sup> PLH	A = = D	tPLH A P	V	0. 50.55		5.5	7.9	1	9	no
tPHL	A or B	ſ	Y $C_L = 50 \text{ pF}$		5.5	7.9	1	9	ns	

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

PARAMETER		TEST C	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	18	pF

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SCLS322M - MARCH 1996 - REVISED OCTOBER 2001

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

#### description

The SN74AHCT1G14 contains a single inverter gate. The device performs the Boolean function  $Y = \overline{A}$ .

## NC 1 5 V<sub>CC</sub>

NC - No internal connection

The device functions as an independent inverter gate, but because of the Schmitt action, gates may have different input threshold levels for positive-  $(V_{T+})$  and negative-going  $(V_{T-})$  signals.

#### ORDERING INFORMATION

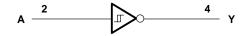
TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G14DBVR	B14_
-40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AHCT1G14DCKR	BF_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

	INPUT A	OUTPUT Y
Г	Н	L
	L	Н

#### logic diagram (positive logic)



<sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

SCLS322M - MARCH 1996 - REVISED OCTOBER 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, V <sub>O</sub> (see Note 1)	V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, I <sub>O</sub> (V <sub>O</sub> = 0 to V <sub>CC</sub> )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	
Storage temperature range, T <sub>stg</sub>	. −65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
ЮН	High-level output current		-8	mA
loL	Low-level output current		8	mA
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	<u> Վ</u> = 25°C	;	MIN N	MAX	UNIT
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
V <sub>T+</sub>		4.5 V	0.9		2	0.9	2	<b>\</b>
Positive-going input threshold voltage		5.5 V	1.1		2	1.1	2	V
V <sub>T</sub> _		4.5 V	0.5		1.6	0.5	1.6	V
Negative-going input threshold voltage		5.5 V	0.6		1.5	0.6	1.5	V
$\Delta V_{T}$		4.5 V	0.4		1.4	0.4	1.4	V
Hysteresis (V <sub>T+</sub> – V <sub>T</sub> )		5.5 V	0.5		1.6	0.4	1.6	٧
Vari	I <sub>OH</sub> = -50 μA	451/	4.4	4.5		4.4		
VOH	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8	V	V
V	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	V
VOL	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	٧
lį	V <sub>I</sub> = V <sub>CC</sub> or GND	0 V to 5.5 V			±0.1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2	10		10	pF



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74AHCT1G14 SINGLE SCHMITT-TRIGGER INVERTER GATE

SCLS322M - MARCH 1996 - REVISED OCTOBER 2001

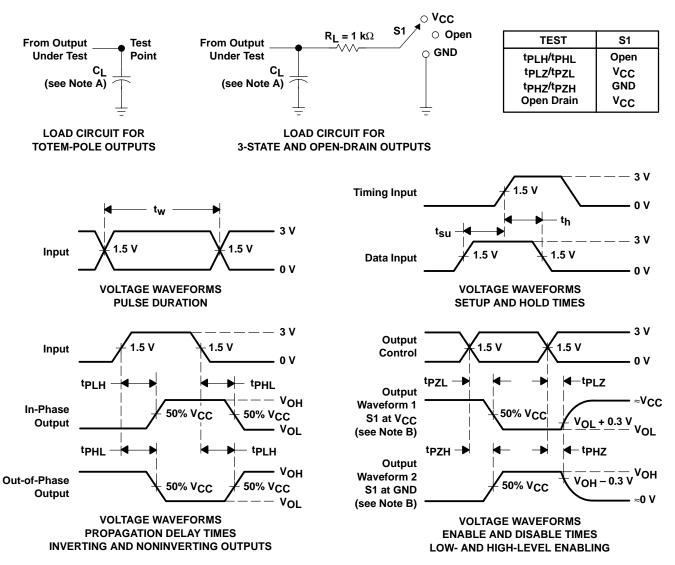
## switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V\pm0.5~V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD T <sub>A</sub> = 25°C		MIN	MAX	UNIT									
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	WIAA	UNII							
<sup>t</sup> PLH	۸	V	C 15 pF		4	7	1	8	no							
<sup>t</sup> PHL	А	,	ı	·	'	1	Ι ΟΕ – 13 βΙ	$C_L = 15 pF$	C[ = 15 pr	OL = 13 pr		4	7	1	8	ns
<sup>t</sup> PLH	۸	V	C: - 50 pF		5.5	8	1	9	no							
<sup>t</sup> PHL	A	T I	ľ	ı	ī	I I	C <sub>L</sub> = 50 pF		5.5	8	1	9	ns			

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER		ONDITIONS	TYP	UNIT
Ср	Power dissipation capacitance	No load,	f = 1 MHz	12	pF

#### PARAMETER MEASUREMENT INFORMATION



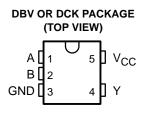
- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



SCLS320J - MARCH 1996 - REVISED JULY 2001

- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



#### description

The SN74AHCT1G32 is a single 2-input positive-OR gate. The device performs the Boolean function Y = A + B or  $Y = \overline{A} \bullet \overline{B}$  in positive logic.

#### **ORDERING INFORMATION**

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>‡</sup>
40°C to 95°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G32DBVR	B32_
–40°C to 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AHCT1G32DCKR	BG_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

	INPUT	OUTPUT	
	4	В	Υ
H	1	Χ	Н
)	<b>X</b>	Н	Н
	L	L	L

#### logic diagram (positive logic)





<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

SCLS320J - MARCH 1996 - REVISED JULY 2001

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
VI	Input voltage	0	5.5	V
VO	Output voltage	0	VCC	V
ІОН	High-level output current		-8	mA
l <sub>OL</sub>	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	WAA	UNIT
Vou	$I_{OH} = -50 \mu A$	4.5 V	4.4	4.5		4.4		V
Vон	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		ľ
\/o.	I <sub>OL</sub> = 50 μA	4.5 V			0.1		0.1	<b>V</b>
VOL	$I_{OL} = 8 \text{ mA}$	4.5 V			0.36		0.44	V
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
∆l <sub>CC</sub> ‡	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		2	10		10	pF

 $<sup>\</sup>ddagger$  This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V $_{
m CC}$ .



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

#### SN74AHCT1G32 SINGLE 2-INPUT POSITIVE-OR GATE

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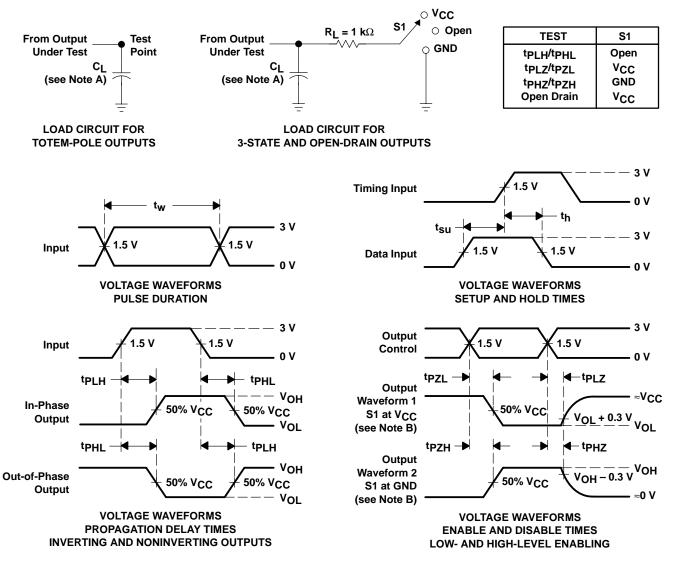
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD $T_A = 25^{\circ}C$		MIN	MAX	UNIT											
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIA	IVIAA	ONIT									
<sup>t</sup> PLH	A or B	Y	Y	Y C <sub>L</sub> = 15 pF	C: 15 pF		5	6.9	1	8	20							
<sup>t</sup> PHL	AUIB				'	1	- ομ - 10 βι	C[ = 15 pr	OL = 13 pr	G[ = 13 pr		5	6.9	1	8	ns		
<sup>t</sup> PLH	A or B	Y	C. F0.pF		5.5	7.9	1	9	20									
tPHL	AUID		l '	ī	ī	ī	T .	T I	Y	Y	i CL	C <sub>L</sub> = 50 pF	CL = 50 pr		5.5	7.9	1	9

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TEST CO	NDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	11.5	pF

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### **DBV OR DCK PACKAGE** (TOP VIEW) 5 V<sub>CC</sub> в [ GND [ 3

#### description

The SN74AHCT1G86 is a single 2-input exclusive-OR gate. The device performs the Boolean function  $Y = A \oplus B$  or  $Y = \overline{AB} + A\overline{B}$  in positive logic.

#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G86DBVR	B86_
-40 C 10 65°C	SOP (SC-70) – DCK	Tape and reel	SN74AHCT1G86DCKR	BH_

<sup>†</sup>Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INP	UTS	OUTPUT		
Α	В	Υ		
L	L	L		
L	Н	Н		
Н	L	Н		
Н	Н	L		

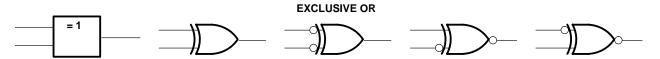
9-27

<sup>&</sup>lt;sup>‡</sup>The actual top-side marking has one additional character that designates the assembly/test site.

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#### exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



These five equivalent exclusive-OR symbols are valid for an SN74AHCT1G86 gate in positive logic; negation may be shown at any two ports.

# The output is active (low) if all inputs stand at the same logic level (i.e., A = B). EVEN-PARITY ELEMENT 2k The output is active (low) if an even number of inputs (i.e., only 1 of the 2) are active.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V <sub>CC</sub>	0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	
Output voltage range, V <sub>O</sub> (see Note 1)	$\dots$ -0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{ K }(V_{ C } < 0)$	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stq</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
Іон	High-level output current		-8	mA
loL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	<b>∆</b> = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT
Vou	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		<b>&gt;</b>
Voн	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		V
Voi	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1	٧
VOL	$I_{OL} = 8 \text{ mA}$				0.36		0.44	V
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Δlcc†	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V			1.35		1.5	mA
Ci	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.

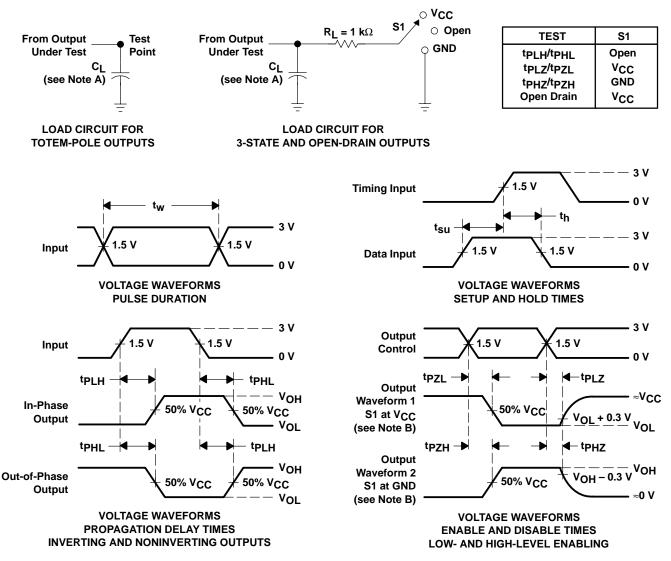
## switching characteristics over recommended operating free-air temperature range, $V_{CC}=5~V\pm0.5~V$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T,	Δ = 25°C	;	MIN	MAX	UNIT				
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	IVIIIN	IVIAA	UNIT				
<sup>t</sup> PLH	A or B	V	C15 pF		5	6.9	1	8	ne				
<sup>t</sup> PHL	AUIB	ī	C <sub>L</sub> = 15 pF		5	6.9	1	8	ns				
<sup>t</sup> PLH	A or B	V	C 50 pF		5.5	7.9	1	9	20				
tPHL	AUID	ř	Ť	Y	Y	Ť	Y C <sub>L</sub> = 50 pF		5.5	7.9	1	9	ns

#### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER		ONDITIONS	TYP	UNIT
C <sub>pd</sub>	C <sub>pd</sub> Power dissipation capacitance		f = 1 MHz	18	pF

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17

## DBV OR DCK PACKAGE (TOP VIEW) OE 1 5 VCC A 2 GND 3 4 Y

#### description

The SN74AHCT1G125 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable  $(\overline{OE})$  input is high. When  $\overline{OE}$  is low, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

#### ORDERING INFORMATION

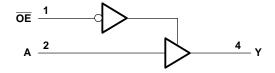
TA	PACKAGI	ʆ	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
400C to 050C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G125DBVR	B25_
–40°C to 85°C	SOP (SC-70) - DCK	Tape and reel	SN74AHCT1G125DCKR	BM_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPU	JTS	OUTPUT
OE	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

#### logic diagram (positive logic)



<sup>&</sup>lt;sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
Іон	High-level output current		-8	mA
loL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Voc	T,	չ = 25°C	;	MIN	MAX	UNIT
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	IVIIIV	IVIAA	UNIT
Voн	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		V
VOH	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		V
Vol	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1	V
V <sub>OL</sub>	I <sub>OL</sub> = 8 mA	4.5 V			0.36		0.44	V
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Δl <sub>CC</sub> ‡	One input at 3.4 V, Other input at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
Co	$V_O = V_{CC}$ or GND	5 V		10				pF

<sup>‡</sup>This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

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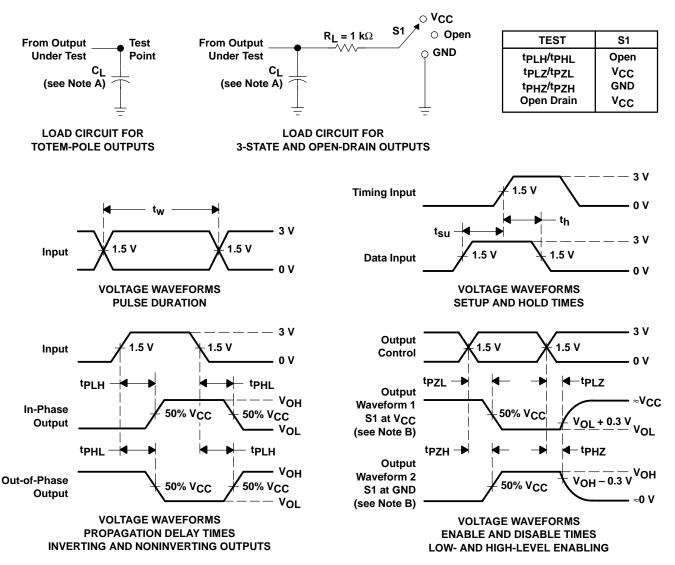
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T	չ = 25°C	;	MIN	MAX	UNIT				
PARAMETER	(INPUT)		(OUTPUT) CAPACITANCE		TYP	MAX	IVIIIN	IVIAA	UNIT				
t <sub>PLH</sub>	А	Y	C <sub>I</sub> = 15 pF		3.8	5.5	1	6.5	ns				
tPHL	A	ı	OL = 13 pr		3.8	5.5	1	6.5	115				
<sup>t</sup> PZH	ŌĒ	Υ	C <sub>L</sub> = 15 pF		3.6	5.1	1	6	ns				
<sup>t</sup> PZL	OE	T	ı	1	1	ľ	OL = 13 pr		3.6	5.1	1	6	115
<sup>t</sup> PHZ	ŌĒ	Y	C <sub>L</sub> = 15 pF		4.6	6.8	1	8	ns				
t <sub>PLZ</sub>	OL		OL = 13 pr		4.6	6.8	1	8	115				
<sup>t</sup> PLH	А	Y	C: 50 pF		5.3	7.5	1	8.5	20				
t <sub>PHL</sub>	A	ī	C <sub>L</sub> = 50 pF		5.3	7.5	1	8.5	ns				
<sup>t</sup> PZH	<u></u>	Y	V 0: 50 = 5		5.1	7.1	1	8	no				
<sup>t</sup> PZL	ŌĒ	Y C <sub>L</sub> = 50 pF		5.1	7.1	1	8	ns					
<sup>t</sup> PHZ	ŌĒ	Y	C: _ 50 pF		6.1	8.8	1	10	ne				
t <sub>PLZ</sub>	OE .	ſ	C <sub>L</sub> = 50 pF		6.1	8.8	1	10	ns				

#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER		TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load, f = 1 MHz	14	pF

#### PARAMETER MEASUREMENT INFORMATION



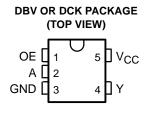
- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



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- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)



#### description

The SN74AHCT1G126 is a single bus buffer gate/line driver with 3-state output. The output is disabled when the output-enable (OE) input is low. When OE is high, true data is passed from the A input to the Y output.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### ORDERING INFORMATION

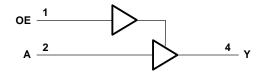
TA	PACKAGE	<u>:</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
-40°C to 85°C	SOP (SOT-23) – DBV	Tape and reel	SN74AHCT1G126DBVR	B26_
-40 C 10 85°C	SOP (SC-70) – DCK	Tape and reel	SN74AHCT1G126DCKR	BN_

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### **FUNCTION TABLE**

INPU	JTS	OUTPUT
OE	Α	Y
Н	Н	Н
Н	L	L
L	Χ	Z

#### logic diagram (positive logic)



<sup>‡</sup> The actual top-side marking has one additional character that designates the assembly/test site.

#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 7 V
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to 7 V
Output voltage range, VO (see Note 1)	0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±25 mA
Continuous current through V <sub>CC</sub> or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T <sub>stg</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	V
٧o	Output voltage	0	VCC	V
ІОН	High-level output current		-8	mA
loL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	vcc	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
	TEST CONDITIONS		MIN	TYP	MAX	IVIIIN	WAX	UNIT
Voн	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		٧
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V	4.5.\/		0.1		0.1	V
	$I_{OL} = 8 \text{ mA}$	4.5 V			0.36		0.44	ı v
lį	$V_I = V_{CC}$ or GND	0 V to 5.5 V			±0.1		±1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			±0.25		±2.5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10	μΑ
Δl <sub>CC</sub> ‡	One input at 3.4 V, Other input at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	$V_I = V_{CC}$ or GND	5 V		4	10		10	pF
Co	$V_O = V_{CC}$ or GND	5 V		10				pF

This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

SCLS380G - AUGUST 1997 - REVISED JULY 2001

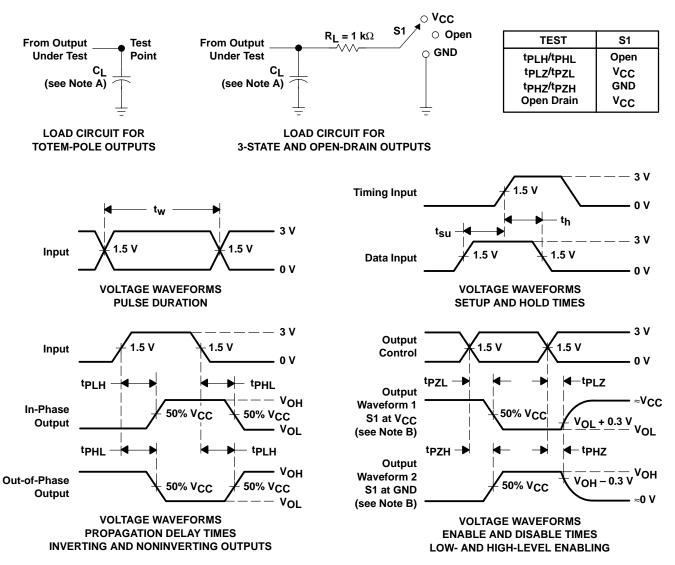
## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT	
PARAMETER	(INPUT)			MIN	TYP	MAX	IVIIIA	WAX	UNII	
t <sub>PLH</sub>	А	Y	C <sub>I</sub> = 15 pF		3.8	5.5	1	6.5	nc	
tPHL	A		T CL = 15 PF		3.8	5.5	1	6.5	ns	
<sup>t</sup> PZH	0.5	Y	C <sub>L</sub> = 15 pF		3.6	5.1	1	6	ns	
<sup>t</sup> PZL	OE		OL = 13 pr		3.6	5.1	1	6	115	
<sup>t</sup> PHZ	- OE	Y	C <sub>L</sub> = 15 pF		4.6	6.8	1	8	ns	
t <sub>PLZ</sub>		OL	'	OL = 13 pr		4.6	6.8	1	8	115
<sup>t</sup> PLH	Δ	Y C <sub>L</sub> =	Y C <sub>L</sub> = 50 pF	C: 50 pF		5.3	7.5	1	8.5	20
t <sub>PHL</sub>	А			CL = 50 pr		5.3	7.5	1	8.5	ns
<sup>t</sup> PZH	OE	Y C <sub>L</sub> = 50 pF		5.1	7.1	1	8	no		
t <sub>PZL</sub>	OE		CL = 50 pF	CL = 50 pr		5.1	7.1	1	8	ns
<sup>t</sup> PHZ	OE	Y C <sub>L</sub> = 50 pF	0 50-5		6.1	8.8	1	10	ne	
t <sub>PLZ</sub>				6.1	8.8	1	10	ns		

#### operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST CO	NDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

#### PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C<sub>I</sub> includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq$  3 ns,  $t_f \leq$  3 ns.
  - D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



General Information	1
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## PicoGate Logic

SCAT007 September 1997



## APPLICATION NOTE

September 1997

## **PicoGate Logic**





Let's make things better.

Philips Semiconductors and Texas Instruments now offer the smallest single gate 5V logic family available, PicoGate Logic. Consisting of single gate functions packaged in a 5 pin SOT353 package, PicoGate Logic reduces board space requirements 10 times over the conventional 14 pin SO package.

Driven by applications with a very small circuit board mounting area, the PicoGate Logic family offers the most popular logic functions for space-constrained systems such as cellular phones, pagers, and portable consumer products (CD players, VCR's, cameras, hard disks, notebook computers, PC cards, CD ROM's, and Personal Digital Assistants). They can also be used as simple glue/repair logic to implement last minute design changes or to eliminate dependence on intricate line layout patterns and simplify routing.

Philips Semiconductors offers PicoGate Logic in the HC and HCT families. Texas Instruments provides the same functions in the AHC and AHCT families respectively. The package used is a major breakthrough in IC packaging concepts, using the same package as leading edge discrete semiconductor components. Space savings can be compared in Figure 1.

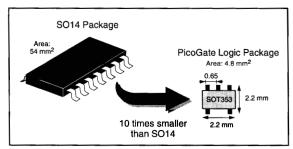


Figure 1. SO14 package comparison to 5-pin SOT353

This publication includes details on package specifications and soldering guidelines to assist you in your board design. Following you will find package dimensions, solder land guidelines, and soldering guidelines.

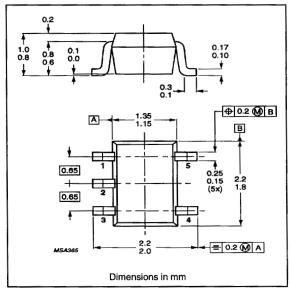


Figure 2. SOT353 package dimensions

#### Footprint design

The footprint design of a component for surface mounting is influenced by many factors:

- Features of the component, its dimensions, and tolerances
- Circuit board manufacturing processes
- Desired component density
- Minimum spacing between components
- · Circuit tracks under the component
- Component orientation (if wave soldering)
- · Positional accuracy of solder resist to solder lands
- Positional accuracy of solder paste to solder lands (if reflow soldering)
- Component placement accuracy
- Soldering process parameters
- Solder joint reliability parameters

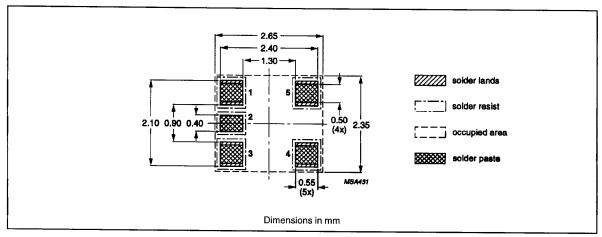


Figure 3. Reflow soldering footprint

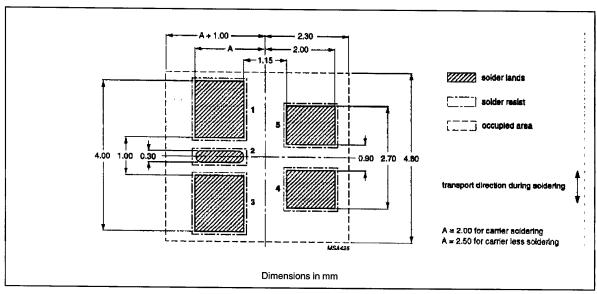


Figure 4. Wave soldering footprint for SOT353

#### **SOLDERING**

#### Reflow soldering

#### **REFLOW TECHNIQUES**

#### Thermal conduction

The prepared substrates are carried on a conveyor belt, first through a preheating stage and then through a soldering stage. Heat is transferred to the substrate by conduction through the belt. Figure 5 shows a theoretical time/temperature relationship for thermal conduction reflow soldering. This method is particularly suited to thick film substrates and is often combined with infrared heating.

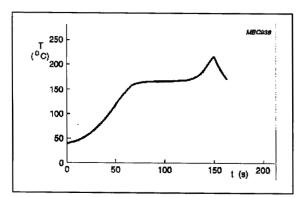


Figure 5. Theoretical time/temperature curve for a typical thermal conductive reflow cycle

#### Infrared

An infrared oven has several heating elements giving a broad spectrum of infrared radiation, normally above and below a closed loop belt system. There are separate zones for preheating, soldering, and cooling. Dwell time in the soldering zone is kept as short as possible to prevent damage to components and substrate. A typcial heating profile is shown in Figure 6. This reflow method is often applied in double-sided prints.

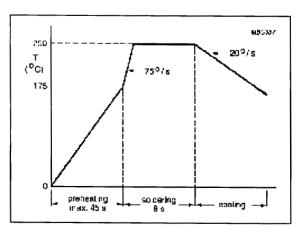


Figure 6. Typical temperature profile of an infrared oven operating at a belt speed of 0.41 mm/min.

September 1997

#### Vapor phase

A substrate is immersed in vapors of a suitable boiling liquid. The vapors transfer latent heat of condensation to the substrate and solder reflow takes place. Temperature is controlled precisely by the boiling point of the liquid at a given pressure. Some systems employ two vapor zones, one above the other. An elevator tray, suspended from a hoist mechanism passes the substrate vertically through the first vapor zone into the secondary soldering zone and then hoists it out of the vapor to be cooled. A theoretical time/temperature relationship for this method is shown in Figure 7.

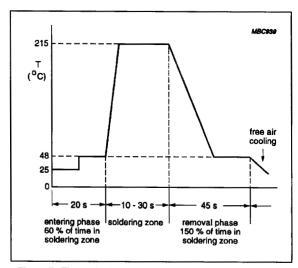


Figure 7. Theoretical time/temperature curve relationship for dual vapor reflow soldering

#### Wave soldering

Wave soldering is usually the best method to use when high throughput rates are required. The single wave soldering principle (see Figure 8) is the most straightforward method and can be used on simple substrates with two-terminal SMD components. More complex substrates with increased circuit density and closer spacing of conductors can pose he problem of nonwetting (dry joints) and solder bridging. Bridging can occur across the closely spaced leads of multi-leaded devices as well as across adjacent leads on neighboring components. Nonwetting is usually caused by components with plastic bodies. The plastic is not wetted by solder and creates a depression in the solder wave, which is augmented by surface tension. This can cause a shadow behind the component and prevent solder from reaching the joint surfaces. A smooth laminar solder wave is required to avoid bridging and a high pressure wave is needed to completely cover the areas that are difficult to wet. These conflicting demands are difficult to attain in a single wave, but dual wave techniques go a long way in overcoming

In a dual wave machine (see Figure 9), the substrate first come into contact with a turbulent wave which has a high vertical velocity. This ensures good solder contact with both edges of the components and prevents joints from being missed. The second smooth laminar wave completes the formation of the solder fillet, removes excess solder, and prevents bridging. Figure 10 indicates the time/temperature relationship measured at the soldering site in dual wave soldering.

New methods for wave soldering are developing continually. For example, Omega System is a single wave agitated by pulses, which combines the functions smoothness and turbulence. In another, a lambda wave injects air bubbles in the final part of the wave. A further innovation is the hollow jet wave in which the solder wave flows in the opposite direction to the substrate.

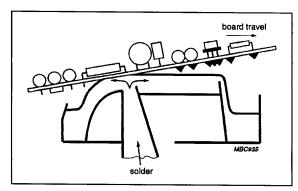


Figure 8. Single wave soldering principle

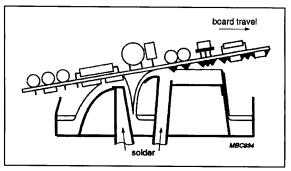


Figure 9. Double wave soldering principle

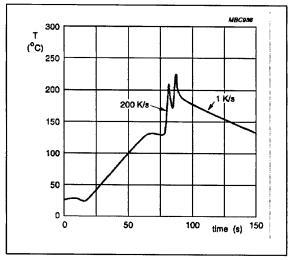


Figure 10. Typical time/temperature curve measured at the soldering site

**NOTES** 

**NOTES** 

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Home Page: www.philipslogic.com

**Product Information** 

Phone: 1-800-447-1500, ext. 1430 FAX: 1-800-943-0087 (in U.S.A)

or

1-512-434-1568 (rest of world)

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Product

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9397 750 02862 SCAT007

## Design Summary for NanoStar™ Little Logic

www.ti.com/sc/nanostar

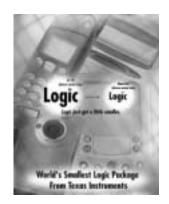
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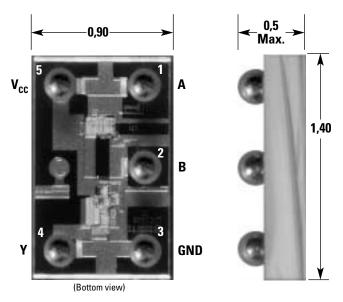
## **Design Summary for NanoStar™ Little Logic**

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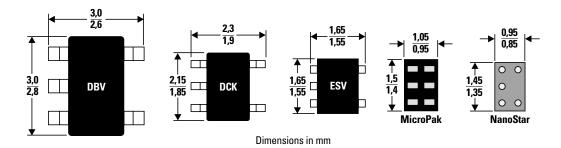


#### **Introduction to NanoStar Little Logic**

Texas Instruments (TI) now offers the smallest single gate logic family available. NanoStar Little Logic consists of single gate logic functions packaged in a chip scaled package. NanoStar Little Logic reduces board space requirements several times over the conventional 5-pin package. This micro scale technology is driven by applications requiring a very small circuit board mounting area. The NanoStar Little Logic family offers the most popular logic functions for space-constrained systems such as cellular phones, pagers, and portable consumer products (Cellular, DVD/CD ROMs, MD/MP3/CD players, VCRs, DVC, Digital STB, DSC, notebook computers, PC cards, and Personal Digital Assistants). They can also be used as simple glue/repair logic to implement last minute design changes or to eliminate dependence on intricate line layout patterns and simplify routing. TI provides Little Logic functions in the LVC, AHC and AHCT families. The technology used is a major breakthrough in IC packaging concepts, using the die as the package. Space savings can be compared below.



Dimensions in millimeters (mm)



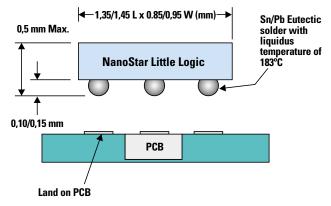
	SOT-23 (DBV) (TI)	SC-70 (DCK) (TI)	ESV	MicroPak™	NanoStar™ (YEA)
Length (mm)	2,90 ± 0,1	2,00 ± 0,15	1,60 ± 0,05	1,45 ± 0,05	1,40 ± 0,05
Width (mm)	2,80 ± 0,2	2,10 ± 0,2	1,60 ± 0,05	1,00 ± 0,05	0,90 ± 0,05
Height (mm)	1,20	0,95	0,55	0,55	0,50
Footprint Area (mm²)	8,12	4,20	2,56	1,45	1,26
Weight (gm)	0,0135	0,006	≥ 0,003	≥ 0,001	≤ 0,001

#### **PCB Design Guidelines**

#### **Solder Ball Composition**

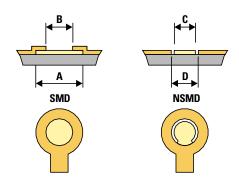
# Protective Overcoat (Al/NiV/CU) Nitride

#### Package Area Configuration (0,5-mm Ball Pitch)

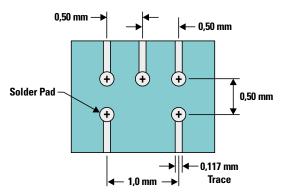


Note: Self-planarizing package.

#### **Solder Mask and Non-Solder Mask**

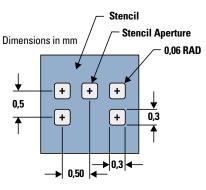


Solder Mask Defined (SMD) Pad		Non-Solder Mask Defined (NSMD) Pad Preferred		
Copper Pad	Solder Mask Opening	Copper Pad	Solder Mask Opening	
"A"	"B"	"C"	"D"	
0,350 mm	0,25 mm	0,28 mm	0,33 mm	
+0,01 -0,0	±0,05	±0,05	±0,02	
(14 mils)	(10 mils)	(11 mils)	(13 mils)	



The PCB layout assumes 0,117-mm (4.6-mil) trace width and 1-oz. copper layer thickness.

#### **Stencil Vitals**



Stencil Thickness = 0,10 mm

#### **Solder Paste**

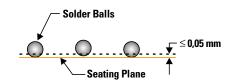
TI recommends the use of type 3 or finer solder paste when mounting the NanoStar package. The use of paste offers the following advantages:

- It acts as a flux to aid wetting of the solder ball to the PCB land.
- The adhesive properties of the paste will hold the component in place during reflow.
- Paste contributes to the final volume of solder in the joint, and thus allows this volume to be varied to give an optimum joint.
- Paste selection is normally driven by overall system assembly requirements. In general, the "no clean" compositions are preferred due to the difficulty in cleaning under the mounted components.

#### **Geometric Dimensional Tolerances**

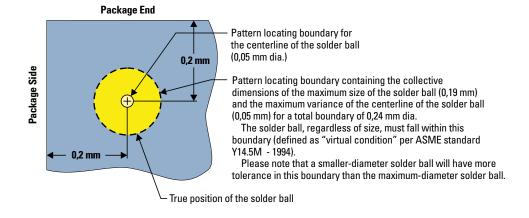
#### Coplanarity

This package meets a coplanarity of 0,05 mm as shown. Coplanarity is defined as a unilateral tolerance zone measured upward from the seating plane. (Reference ASME Y14.5M - 1994)



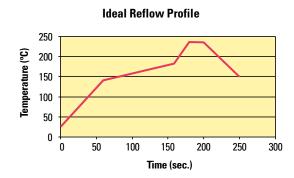
#### **Position Tolerance**

A graphic representation is shown below for the top, left solder ball of the NanoStar package.



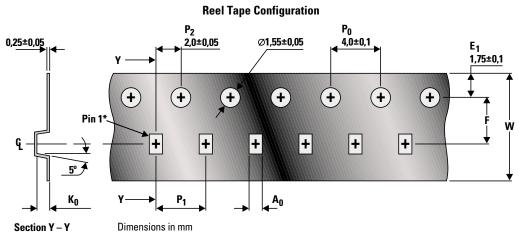
#### **IR Reflow Profile**

Ideal (1st and 2nd) Reflow Profile				
RT to 140°C	60 – 90 sec.			
140°C to 180°C	60 – 120 sec.			
Time Above 183°C	60 – 150 sec.			
Peak Temp.	220°C ±5°C			
Time Within 5°C Peak Temp.	10 – 20 sec.			
Ramp Down Rate	6°sec. Max.			



Note: This is an ideal profile, and actual conditions obtained in any specified reflow oven will vary. This profile is based on convection or RF plus forced convection heating.

#### **Packaging Tape and Reel**



\*Pin 1 location is in the upper left-hand corner of the cavity. Units shipped with bumps down.

Cover Tape Width (W)	Pocket Pitch (P <sub>1</sub> )	Reel Width	Reel Dia.	Pocket Width (A <sub>0</sub> )	Pocket Length (B <sub>0</sub> )	Pocket Depth (K <sub>0</sub> )	Hole to Pocket CL (P <sub>2</sub> )	Hole to Pocket CL (F)	Sprocket Hole Pitch (P <sub>0</sub> )
$8,00 \pm 0,3$	$4,00 \pm 0,1$	8,0 +2,0/-0	330 max	0,99 ± 0,1	1,48 ± 0,1	0,57 ± 0,1	$2,0 \pm 0,1$	$3.5 \pm 0.1$	$4,0 \pm 0,1$

#### **Sockets**

#### Socket & Socket Manufacturer (Ordering Information)

Socket Number: 02-9023 Everett Charles Technologies 4837 White Bear Parkway St. Paul, MN 55110

Ph: 651-407-7777 FAX: 651-407-7290

Web Address: www.ectinfo.com

#### **Electrical Characteristics**

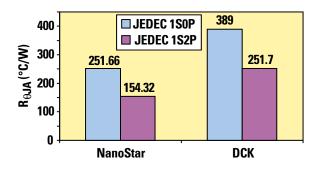
	R (ohms)	L (nH)	C (pF)
Min.	0.001	0.021	0.045
Mean	0.001	0.021	0.046
Max.	0.001	0.021	0.047

Note: Electrical package parasitic was achieved through PACED electrical modeling and is based on a 3D model. Actual electrical data may differ slightly from simulated results

Parameter Name	LVC1GxxYEA
Voltage Nodes (V)	5, 3.3, 2.5, 1.8
V <sub>cc</sub> Range (V)	1.65 to 5.5
Input Level	CMOS
Output Level	CMOS
Output Drive (mA)	(-4/4, -8/8, -16/16, -24/24, -32/32)
No. of Gates	1
Static Current (mA)	0.01
t <sub>pd</sub> (max) (ns)	9.9

#### **Thermal Characteristics**

#### **Comparison of NanoStar and DCK Thermal Impedance**



IEDEO 400D	Airflow (linear ft/minute)					
JEDEC 1S2P	0	150	250	500		
NanoStar						
R <sub>OJA</sub> (°C/W)	154.32	152.05	150.73	148.72		
R <sub>eJC</sub> (°C/W)	18.72					
DCK						
R <sub>OJA</sub> (°C/W)	251.7	250.1	247.2	242.7		
R <sub>OJC</sub> (°C/W)	21.4					

#### **Board Level Reliability Data**

Board Level Reliability N <sub>f</sub> (cycles to 1.0% failure)	
NanoStar 1150 cycles	

Note: Board level reliability data was achieved through Finite Element Modeling of actual package construction and is based on the PCB pad finish being Copper (OSP). Actual reliability data may differ slightly from simulated results.

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Indonesia	001-801-10	-800-800-1450
Korea	080-551-2804	_
Malaysia	1-800-800-011	-800-800-1450
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Philippines	105-11	-800-800-1450
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## Flexible Voltage-Level Translation With CBT Family Devices

SCDA006 July 1999



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#### **Abstract**

Voltage translation between buses with incompatible logic levels can be accomplished using Texas Instruments (TI™) translation-voltage clamps (TVC) or standard crossbar technology (CBT) devices. CBT devices in this application offer flexibility in designs, protection of circuits that are sensitive to high-state voltage-level overshoots, and cost efficiency.

#### Introduction

In designing electronics systems, proper interfaces between buses with incompatible logic levels must be provided. Voltage-level translation is necessary to allow the interconnection with flexibility to provide a future migration path to lower-voltage input/output (I/O) levels (see Figure 1). TI offers I/O voltage translation solutions with two device families.

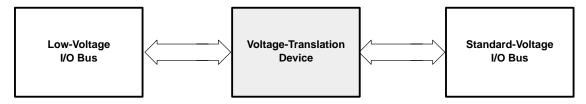


Figure 1. Flexible Voltage-Translation Application

One possible solution for flexible voltage translation is the TI translation-voltage clamp (TVC) family that has been designed specifically for protecting sensitive I/Os (see Figure 2). The information in the data sheet for each TVC-family device describes the I/O protection application of the TVC family and should enable the design engineer to successfully implement an I/O protection circuit utilizing the TI TVC solution.

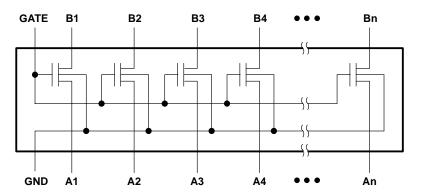


Figure 2. Simplified Schematic of a Typical TVC-Family Device

A comparable solution, allowing cost-effective and flexible voltage translation implemented with standard crossbar technology (CBT) family devices is described in this application report.

#### **Device Description**

The CBT family of devices provides an array of n-type metal-oxide semiconductor (NMOS) field-effect transistors (FETs) with the gates cascaded together to a control circuit (see Figure 3). Within a CBT device, all of the transistors are fabricated at the same time on one integrated die. This leads to a very small fabrication-process variation in the characteristics of the transistors. Because, within the device, the characteristics from transistor-to-transistor are the same, there is minimal deviation from one output to another. This is a large benefit of the CBT solution over discrete devices.

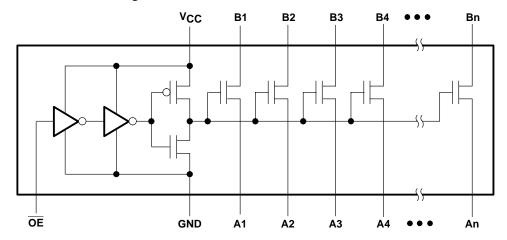


Figure 3. Simplified Schematic of a Typical CBT-Family Device

A CBT device can be used as a voltage limiter or voltage translator by connecting one of the FETs as a reference transistor, and the remainder as pass transistors. The most positive voltage on the low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. All of the transistors in the array have the same electrical characteristics; therefore, any one of them can be used as the reference transistor. Because the transistors are fabricated symmetrically and the I/O signals are bidirectional through each FET, either port connection of each bit can be used as the low-voltage side.

#### **Application**

When the active-low, output-enable  $(\overline{OE})$  input is connected directly to ground, the gate of the p-channel FET in the final inverter of the control circuitry is grounded. This saturates the p-channel, turning the FET on hard, and effectively connects the  $V_{CC}$  input directly to the gates of the n-channel pass transistors, thus providing external control of the gate voltage.

For the example in Figure 4, the ASIC has an open-drain interface that is sensitive to high-state voltages. For the voltage-limiting configuration, the CBT  $\overline{OE}$  input must be grounded. The  $V_{CC}$  input must be connected to one side (A or B) of any one of the transistors. This connection determines the  $V_{BIAS}$  input of the reference transistor. The  $V_{BIAS}$  input is connected through a pullup resistor (typically 200 k $\Omega$ ) to the  $V_{DD}$  supply. A filter capacitor on  $V_{BIAS}$  is recommended. The opposite side is used as the reference voltage ( $V_{REF}$ ) connection. The  $V_{REF}$  input must be less than  $V_{BIAS}-1$  V to bias the reference transistor into conduction. The reference transistor regulates the  $V_{BIAS}$ , thus gate voltage ( $V_{G}$ ) of all the pass transistors. The gate voltage is determined by the characteristic gate-to-source voltage difference ( $V_{GS}$ ) because  $V_{G} = V_{REF} + V_{GS}$ . The low-voltage side of the pass transistors has a high-level voltage limited to a maximum of  $V_{G} - V_{GS}$ , or  $V_{REF}$ . A weak pulldown resistor on open-drain outputs ensures that when the output switches off (logic high), overshoots do not cause the voltage to exceed the maximum voltage rating.

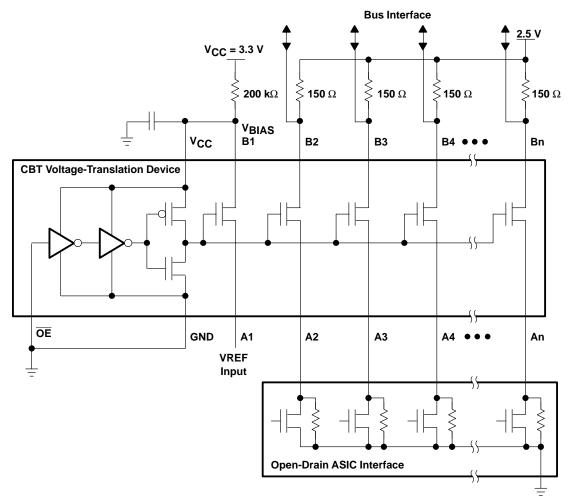


Figure 4. Typical Application of CBT as a Voltage-Translation Device

#### Conclusion

TI offers a line of CBT devices, including standard, Widebus $^{TM}$ , dual-bit, and single-bit functions. The flexibility of CBT enables a low-voltage migration path for advanced designs to align with existing industry standards. The TI CBT family provides the designer with a solution for voltage-level translation and protection of circuits with I/Os that are sensitive to high-state-voltage-level overshoots.

#### Acknowledgment

The authors of this application report are Thomas V. McCaughey, Stephen M. Nolan, and John D. Pietrzak.

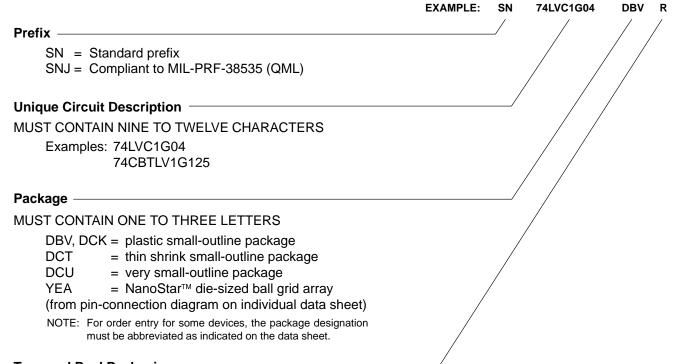
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Electrical characteristics presented in this data book, unless otherwise noted, apply for the circuit type(s) listed in the page heading regardless of package. The availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a four-part type number as explained in the following example.



#### Tape and Reel Packaging

Valid for surface-mount packages only. All orders for tape and reel must be for whole reels.

#### MUST CONTAIN ONE LETTER

R = Standard tape and reel (required for DBV, DCK, DCT, DCU, and YEA packages)

Table 1. N	Normal Dimen	sions of Pa	acking Materials
------------	--------------	-------------	------------------

CARRIER-TAPE WIDTH (mm)	COVER-TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
8	5.4	9.0	178
12	9.2	12.4	330
16	13.3	16.4	330
24	21.0	24.4	330
32	25.5	32.4	330
44	37.5	44.4	330
56	49.5	56.4	330

All material meets or exceeds industry guidelines for ESD protection.

Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1,2,3.

Common dimensions of particular interest to the end user are carrier-tape width, pocket pitch, and quantity per reel (see Figure 1 and Table 2).

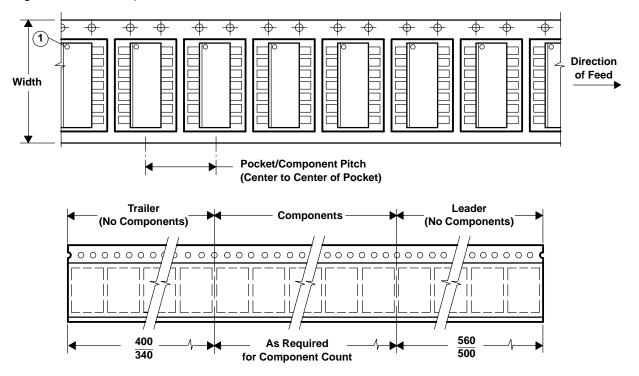


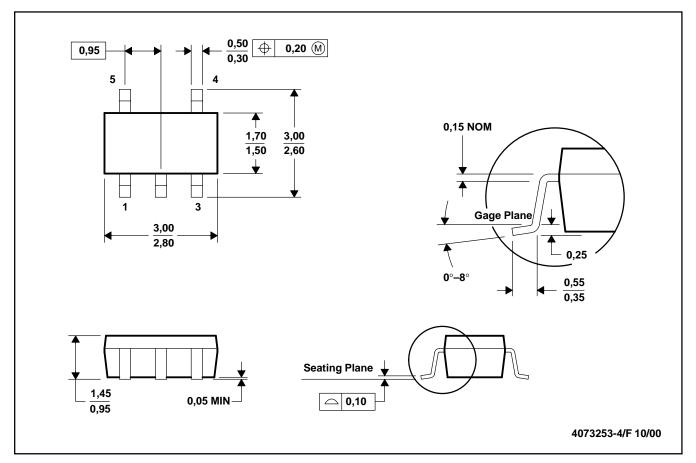
Figure 2. Typical Carrier-Tape Design

**Table 2. Selected Tape-and-Reel Specifications** 

PACKAGE		NO. OF PINS	CARRIER-TAPE WIDTH (mm)	POCKET PITCH (mm)	QTY/REEL
SOP	DBV	5	8.00	4.00	3000
301	DCK	5	8.00	4.00	3000
TSSOP	DCT	8	8.00	4.00	3000
VSOP	DCU	8	8.00	4.00	3000
DSBGA-WCSP	YEA	5	8.00	4.00	3000

#### DBV (R-PDSO-G5)

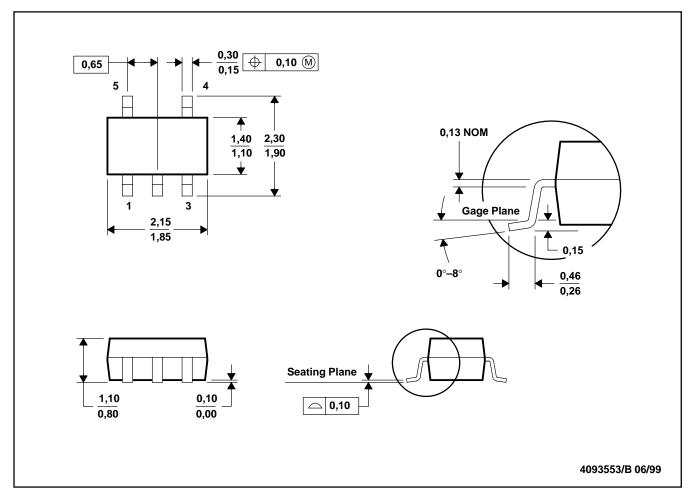
#### **PLASTIC SMALL-OUTLINE**



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-178

#### DCK (R-PDSO-G5)

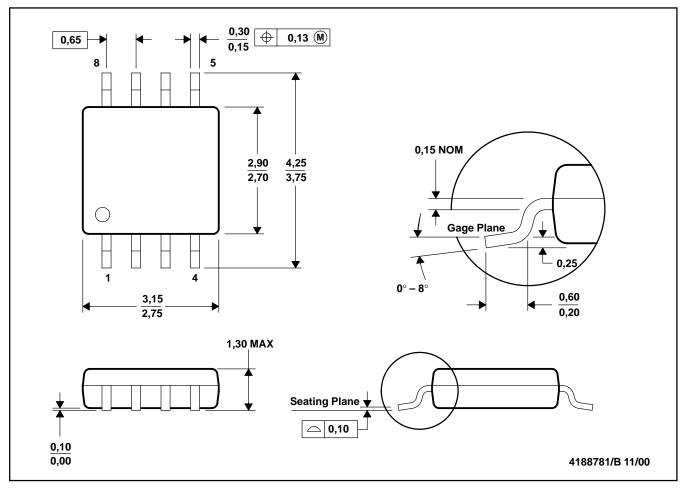
#### **PLASTIC SMALL-OUTLINE**



- B. This drawing is subject to change without notice.C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-203

#### DCT (R-PDSO-G8)

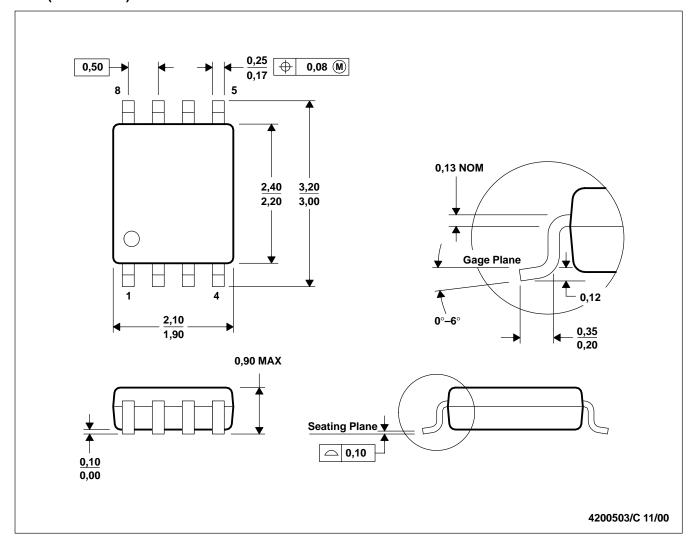
#### PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187

#### DCU (R-PDSO-G8)

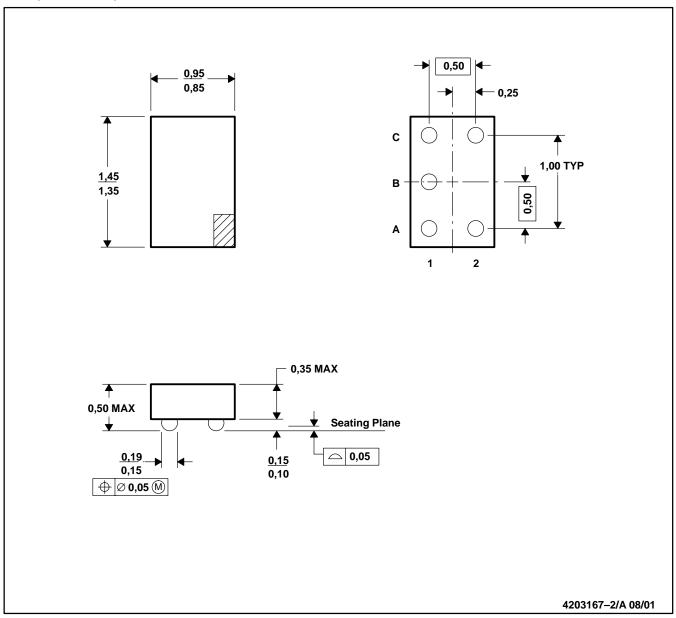
#### PLASTIC SMALL-OUTLINE PACKAGE



- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-187

#### YEA (R-XBGA-N5)

#### **DIE-SIZE BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Wafer Chip Scale Package configuration.