

# **FEB146-001 User's Guide FIN24AC $\mu$ SerDes™ 22-Bit Bi-Directional Serializer/Deserializer Evaluation Board**

**Featured Fairchild Product: FIN24AC**

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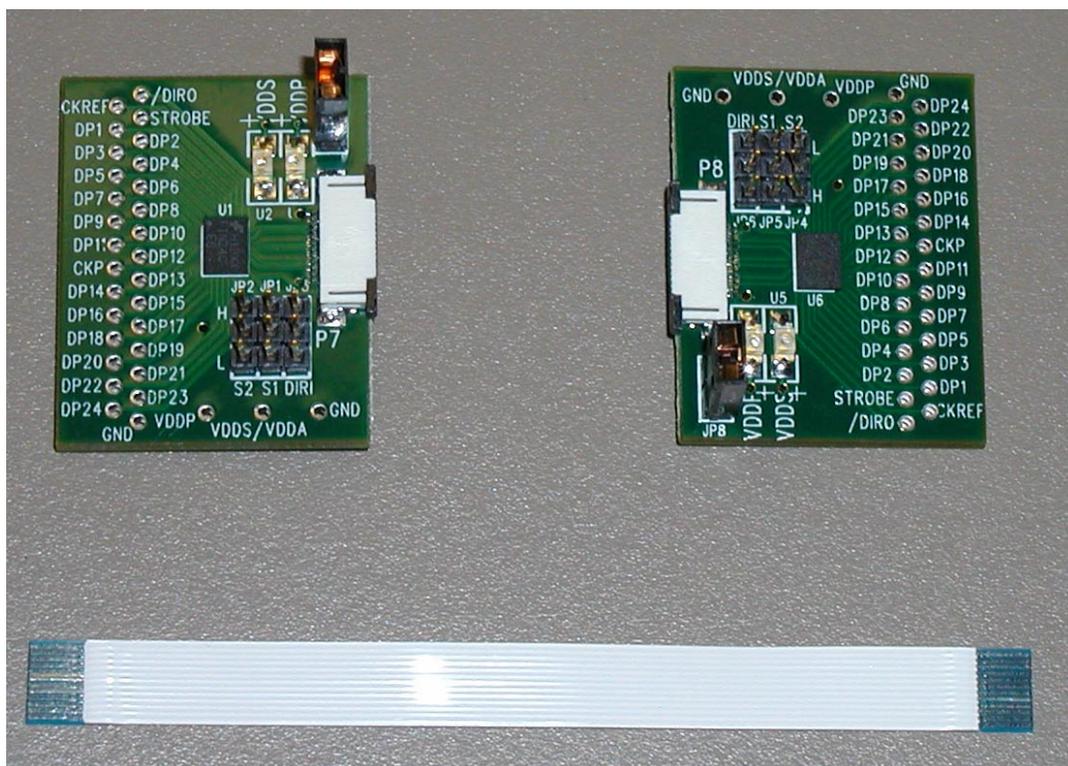
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The following user's guide supports the Evaluation Board system for the FIN micro Serializer and Deserializer devices ( $\mu$ SerDes™). It should be used in conjunction with the FIN24AC datasheet, as well as Fairchild's application notes and  $\mu$ SerDes Technical support team. Interface questions@fairchildsemi.com.

## 1. Overview

The  $\mu$ SerDes micro evaluation system is comprised of two separate boards. The FIN24AC  $\mu$ SerDes evaluation board are each labeled FM050503B. Either board may be configured as a Serializer or Deserializer. The boards sections are identical except for the pin out of the serial connector, as well as the orientation of the printing. The two sections are connected through the included flex cable that carries the serial data, clock and power supplies. In addition to basic connectivity, the cable may be utilized for relative near field EMI testing. Each board is capable of being configured in multiple ways. The  $\mu$ SerDes demo can be conducted through use of lab equipment such as signal generators and logic analyzers. The demo boards provide via holes for connection to test systems. A description of the connections is included in this demo board guide.



**Figure 1: Micro Demo Boards**

## 2. End Applications

- Micro-Controller or Pixel Interfaces
- Image Sensors
- Small Displays  
LCD, cellphone, digital camera, portable gaming, printer, PDA, video camera, automotive, etc.

## 3. Contents of Evaluation Board

- Serializer Evaluation Board with Jumpers
- Deserializers Evaluation Board with Jumpers
- Flex cable

## 4. Evaluation Board Specification

### 4.1 Board Default Configuration

The evaluation board is shipped from the factory as follows:

- The boards are connected and oriented so that writing may be read, the left unit is a serializer, and the right board is a deserializer.
- VDDS/VDDA are connected between serializer and deserializer through the flex.
- VDDP is connected between serializer and deserializer through the flex.
- There is no connection between VDDP and VDDS/VDDA.
- Jumpers 7+8 (JP7 + JP8) are installed to activate power indicator LEDs.

Upon board receipt, the user should verify that the flex is well connected into each socket. Table 1 lists appropriate jumper settings. See device data sheets for description of device connections.

Board Label	Name	Description
JP7, JP8	LED Enable	This may be removed to exclude LED power from current measurements.
S1, S2 (FIN24A, FIN12)	REFCLOCK Frequency Range Selection (CKREF)	These signals must be connected to either a HIGH or LOW condition dependent upon the desired frequency range of operation. See respective datasheet.
S1, S2 (FIN24)	Unidirectional Setting for Bits 21:24	Sets DP[21:24] as fixed inputs, outputs or inputs and outputs. See respective datasheets.
DIR1	Serializer/Deserializer Control	Configuration the $\mu$ SerDes as a serialized or deserializer. Can be tied HIGH, LOW, or driven.

**Table 1: Jumper Settings**

## 4.2 Connecting Power to the Board

Each board has two power supply connections, plus ground. When the flex cable supplied is utilized, power from one board is fed to the other board through the flex. Consequently, only one board needs to be powered. All power supplies must be connected to an appropriate voltage range. Table 2 lists typical voltages utilized. An LED on each board confirms the operation of the power supply.

**Note 1:** An LED may illuminate rather dimly with a power supply set to a low setting. In addition, if power is connected to the board on only 1 side, a brief glance at the LEDs on the opposite will show that the flex is connected correctly and supplying power to the opposite side.

**Note 2:** The power supplies between sections of the board are connected together by default. (VDDP Board 1 to VDDP Board 2, and VDDS/VDDA Board 1 to VDDS/VDDA Board 2))

**Note 3:** For proper operation, make sure all power supplies are activated before input signal is provided to the serializer.

Name	Description
V <sub>D</sub> DA	Voltage Reference Supply Range: 2.5V to 2.9V
V <sub>D</sub> DS	Supply Voltage for the Core and Serial I/O. Must be at 2.5V to 2.9V
V <sub>D</sub> DP	Parallel and Translation Supply Range: 1.65V to 3.6V
Ground	Common to all supplies, and to $\mu$ SerDes ground slug beneath the part.

**Table 2: Voltage Ranges**

## 4.3 Flex Connection

The flex connectors have a limited insertion/removal life. Consequently, it is not advisable to insert and remove the cable repeatedly. In addition, the flex cable supplied by Fairchild should be the only one used with this board. Please contact your Fairchild  $\mu$ SerDes representative to obtain a cable of different specifications.

The flex cable may be inserted or removed, but must be done so with care. To do so, gently slide the flex cable connector snap away from the board and remove the flex cable. When inserting the flex cable, ensure that the connector snap is first in the unlatched position (toward the outside of the board). Gently insert the cable with the contacts facing **upward**.

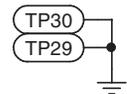
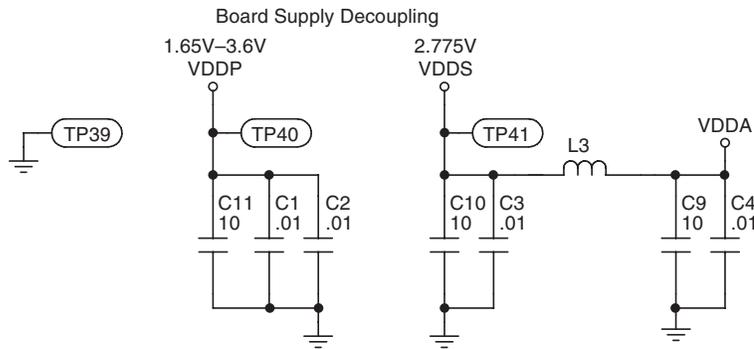
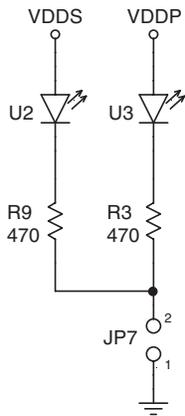
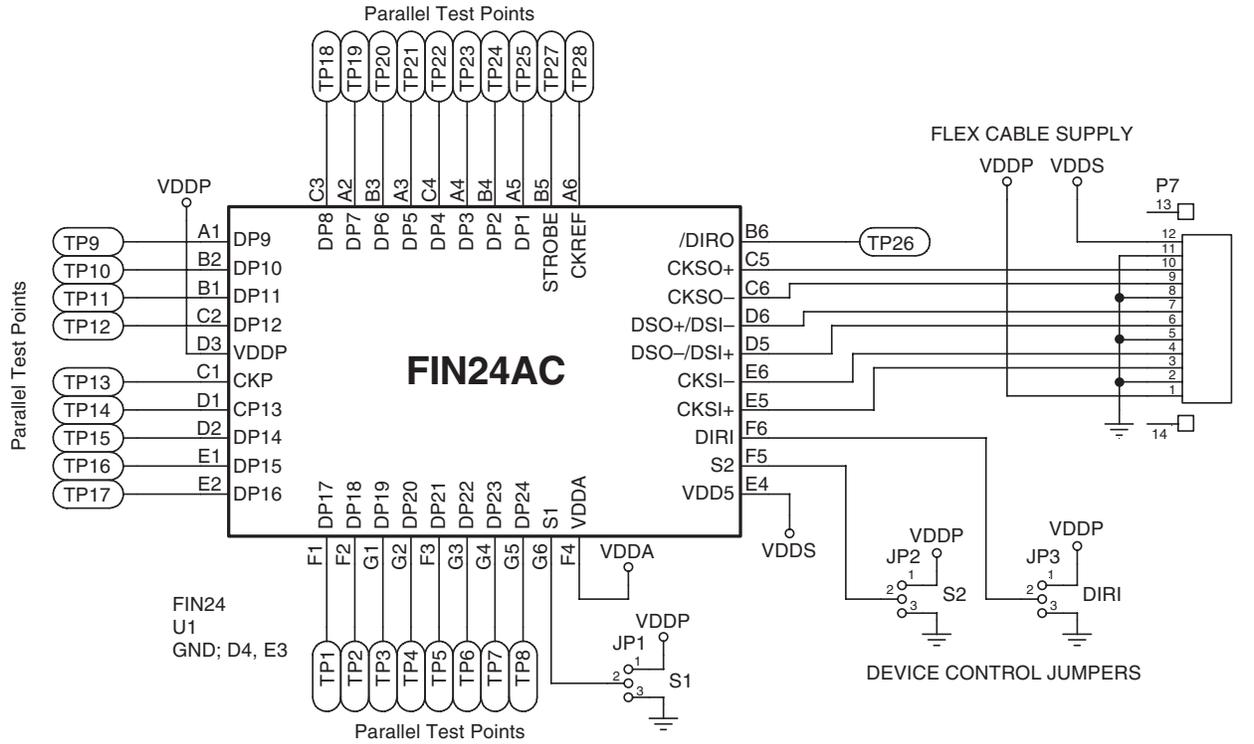
**Note:** An inadvertent short of power supplies on opposite sides of the board while connecting cables may result in extreme current passing through the board and flex cable, which may render the flex cable intermittent or inoperative. Be sure to turn off power before connecting the flex cable.

## 4.4 Troubleshooting

- The  $\mu$ SerDes Evaluation boards and the  $\mu$ SerDes ICs are both completely tested and should not cause problems.
- If deserializer output is not correct, ensure that the proper power-up sequence is being used. For correct operation, power up the devices first, then provide data and clock signals.
- To effectively troubleshoot, the data and clock paths may be probed on either side of the flex. Be aware when probing these locations, as the signals are LVDS by design, meaning the peak to peak voltage will be approximately 200mV, with slightly less than 1.0 Volt bias.
- True differential probes must be used to examine the LVDS signals. Using a terminated oscilloscope with a probe ground to one side of an LVDS signal, will force the 1.0 Volt bias to ground, resulting in a very incorrect signal. Alternatively, a board ground may be offset to accommodate the ground of an oscilloscope. Contact your Fairchild  $\mu$ SerDes representative for further assistance with this.
- Be aware with the FIN24A Serializer that input data Terminal 21 is output from Terminal 23 on the Deserializer, and Serializer input data Terminal 22 is output at the Deserializer on Terminal 24.
- Be aware that the FIN24 has a set frequency range, and that S1 and S2 control the direction of data bits[21:24].
- A careful examination of the serial clock will result in periodic discontinuities. This is normal and represents the imbedded word boundary.
- For additional information pertaining to  $\mu$ SerDes, please see Application Note *AN-5058  $\mu$ SerDes Family Frequently Asked Questions (FAQ)* and the corresponding device data sheets.

## 5. Board Schematics

### 5.1 FIN24AC Serializer Evaluation Board





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Replace components on the Evaluation Board only with those parts shown on the parts list in the User's Guide. Contact an authorized Fairchild representative with any questions.

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