FEB145-001 User's Guide
Non-Isolated 4.5W SEPIC PSU

Featured Fairchild Product: FSDL0165RNB

Table of Contents

1.0 General Board Description

The FEB145-001 Evaluation Board is a non-isolated off-line AC/DC converter (power supply) in SEPIC technology.
It has an universal input voltage range of $85V_{RMS}$ to $265V_{RMS}$ at a line frequency of 50Hz to 60Hz. The nominal output voltage is 15V DC at a maximum load current of 0.3A. However the output voltage can easily be changed by adding a zener diode.

The controller used on the FEB145-001 Evaluation Board is Fairchild Semiconductor's Power Switch (FPS) FSDL0165RNB. This device is an integrated Pulse Width Modulator (PWM) and Sense FET specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combine an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include : a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry.

1.1 Contents of the FEB145-001 Evaluation Kit

- FEB145-001 Evaluation Board
- FEB145-001 Evaluation Kit User's Guide
- CD-ROM containing the following:
  - FEB145-001 Evaluation Kit User's Guide
  - FSDL0165 Datasheet
  - 1N4007 Datasheet
  - 1N4148 Datasheet
  - UF4004 Datasheet
  - BZX55C15 Datasheet
  - BC337 Datasheet
  - Application Notes: AN-4134, AN-4137, AN-4141
  - Off-Line SMPS Design Tool

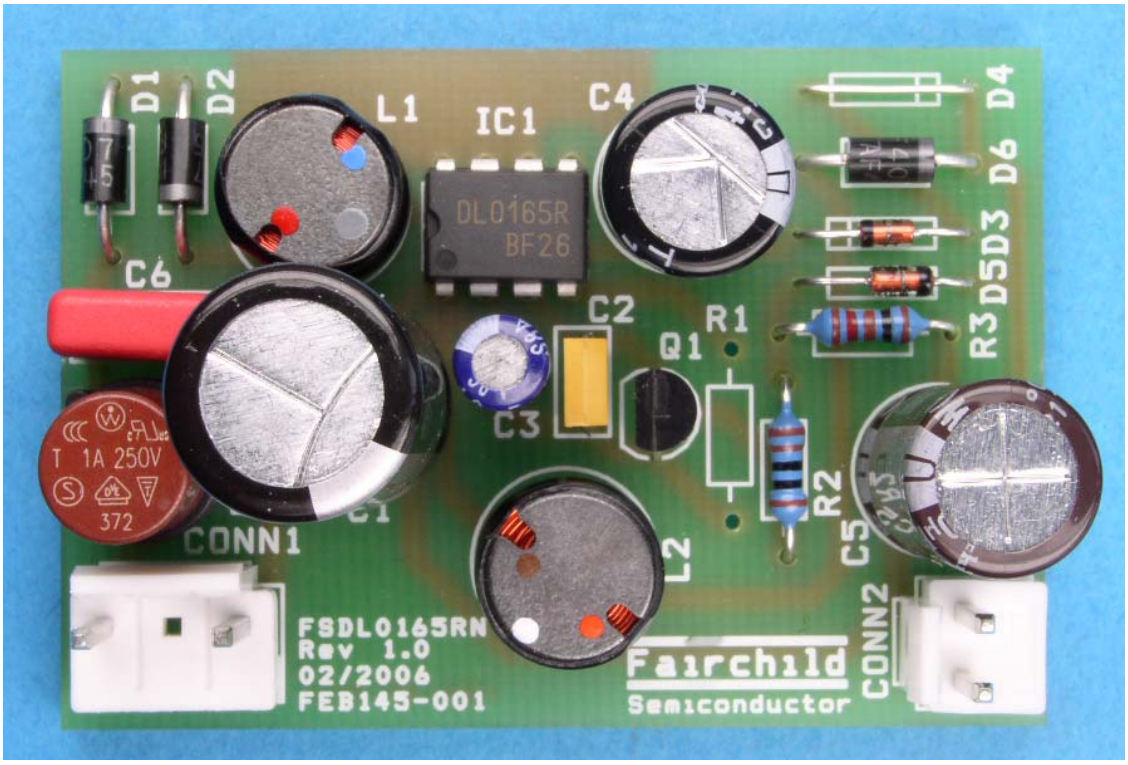
1.2 Power Supply Specification Table

Minimum Line Voltage	$85V_{RMS}$
Maximum Line Voltage	$265V_{RMS}$
Line Frequency	50Hz to 60Hz
Output	15VDC/0.3A

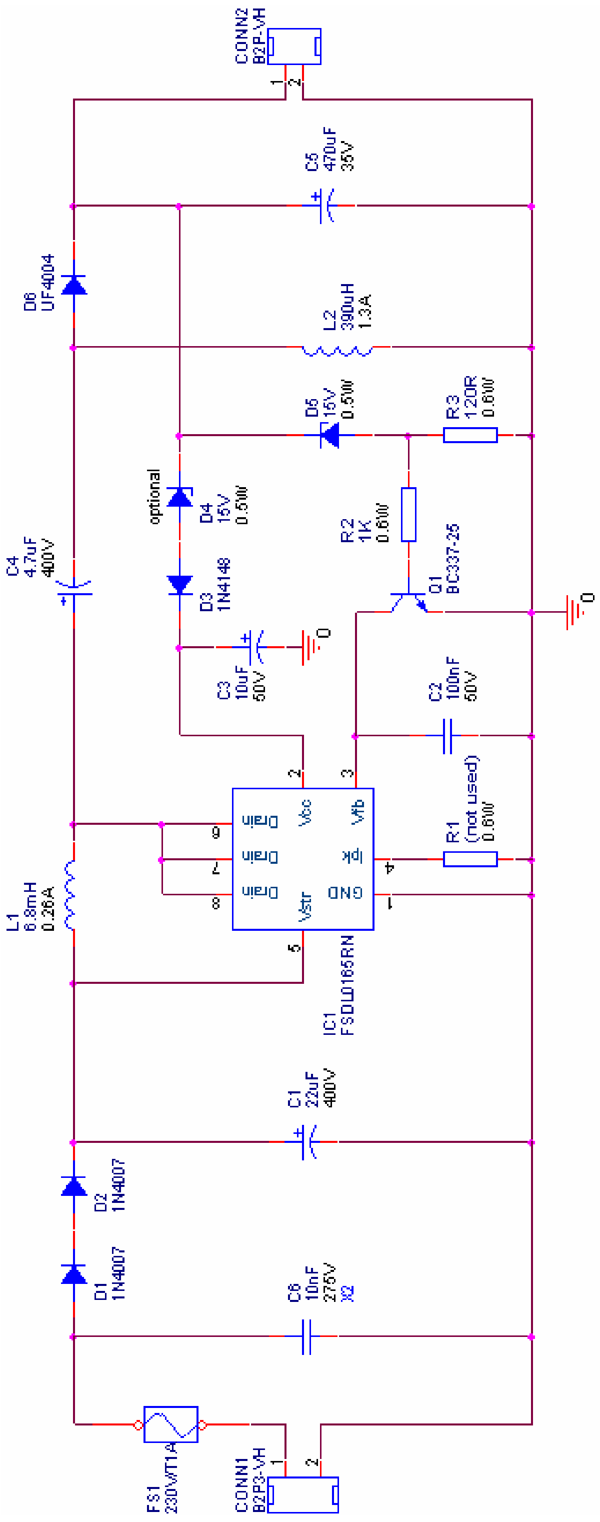
2.0 Circuit Description

The diodes D1, D2 and the DC link capacitor C1 rectify the line input voltage, C6 acts as EMI-filter.
The SEPIC topology works with two inductors L1, L2, a diode D6 and a SEPIC capacitor C4 which are switched by the FPS FSDL0165RNB. The supply voltage for the FPS is taken from the output over ZENER diode D4 (optional), rectifier diode D3 and DC link capacitor C3. For smoothing the ripple of the output voltage there is an electrolytic capacitor C5. Stabilisation of the output voltage is made by a network of a ZENER diode D5, the resistors R2, R3, the transistor Q1 and capacitor C2 which is directly fed into the feedback pin 3 of the FPS.

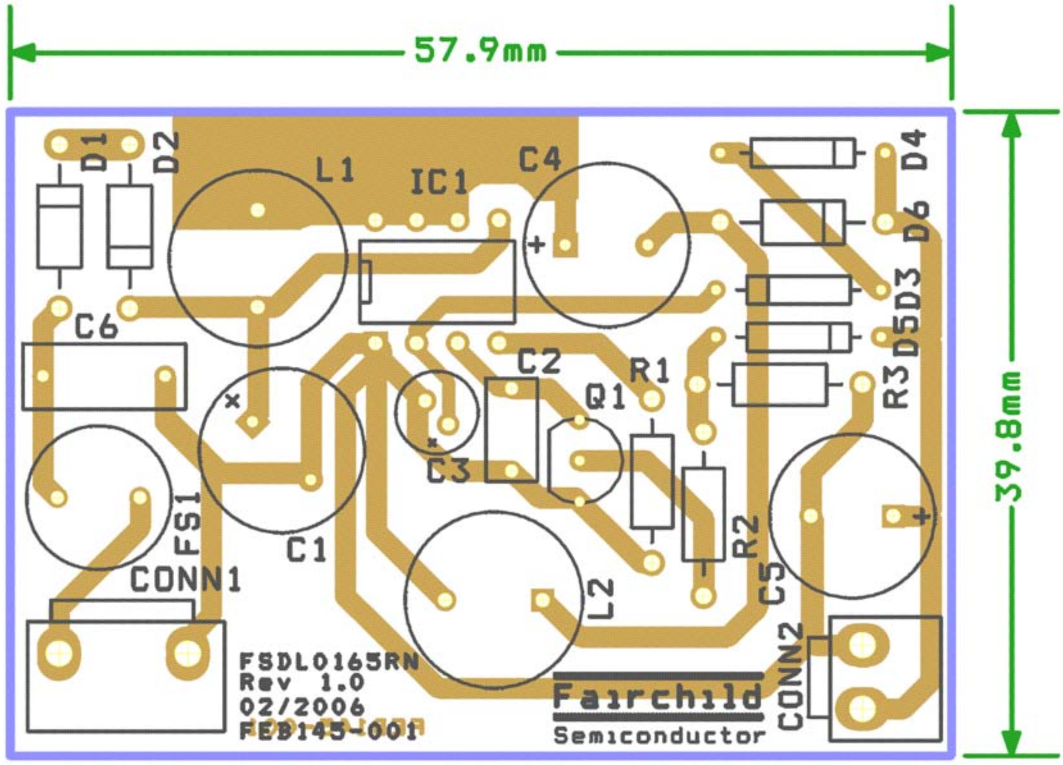
2.1 Board Photograph – Top Side View



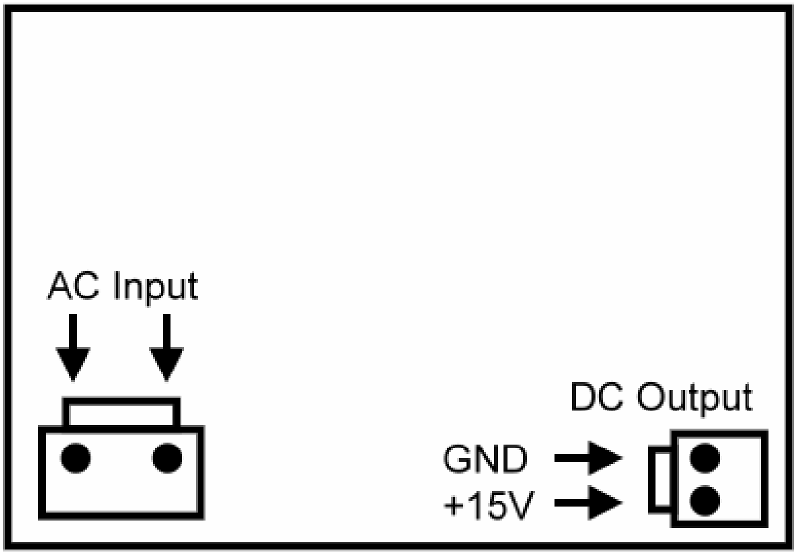
2.2 Schematic



2.3 PCB Layout –Top Side View



2.4 Evaluation Board Connection



3.0 Test Equipment

Oscilloscope:	TEKTRONIX TDS784C (1GHz / 4GS/s)
EMI:	Conducted Emissions Precompliance Test according to ‘Handbook of EC EMC Compliance’, Compliance Design Inc., 1993
Analyzer:	TEKTRONIX 2712
Multimeter:	RMS MULTIMETER FLUKE 85 II
Electronic Load:	Prodigit 3000C Base unit using 3311C, 3314C and 2x 3332A modules
Power Analyzer:	LEM NORMA 5000
AC Source:	Chroma Programmable AC Source Model 61502
Temperature Probe:	Greisinger dual channel digital thermometer GMH3230 using one GTF300 NiCr-Ni thermocouple

4.0 Test Results

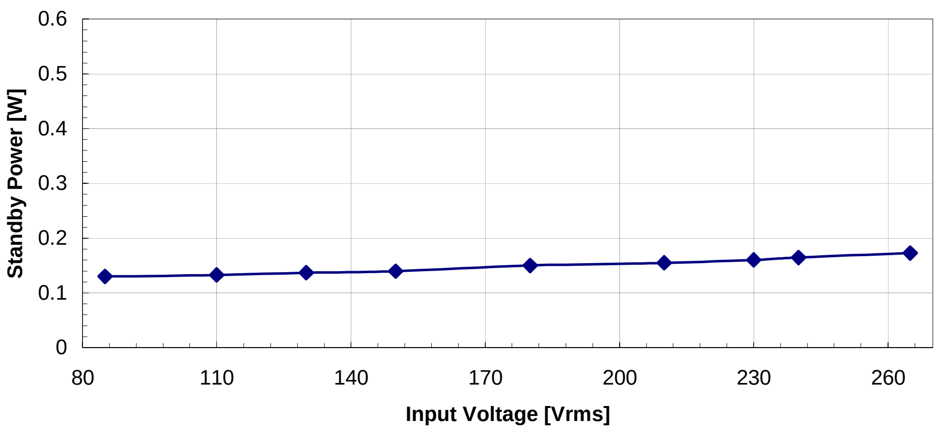
4.1 Standby Power vs Input Voltage

4.1.1 Test Condition and Method

The input power for various input voltages was measured with no load and with 10% of rated load. The standby power was calculated as $P_{STDBY} = P_{IN} - P_{OUT}$.

4.1.2 No Load Standby Power

V_{IN} [V_{RMS}]	85	110	130	150	180	210	230	240	265
P_{IN} [W]	0.13	0.133	0.137	0.14	0.15	0.155	0.16	0.165	0.173
P_{OUT} [W]	0	0	0	0	0	0	0	0	0
P_{STDBY} [W]	0.13	0.133	0.137	0.14	0.15	0.155	0.16	0.165	0.173



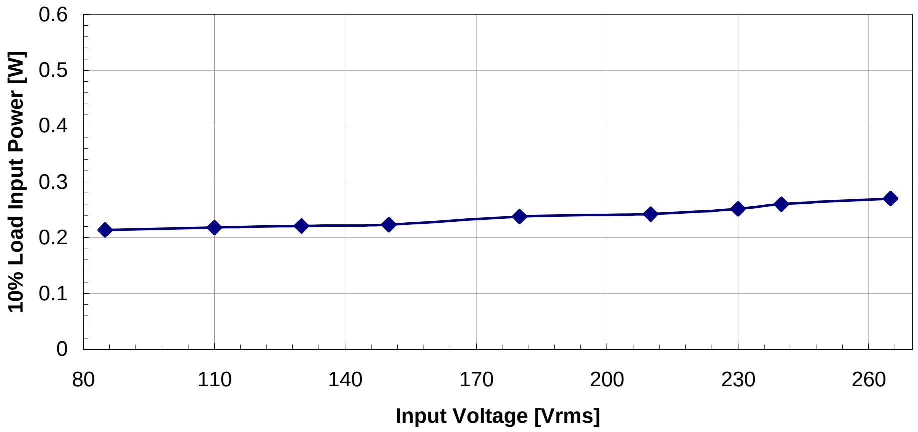
4.1.3 Accuracy of Output with No Load

The minimum and maximum values in the table below are calculated as deviations from the output voltage as specified in section 1.2

V_{IN} [V_{RMS}]	85	110	130	150	180	210	230	240	265		Min [%]	Max [%]
V_1 [V]	15.30	15.29	15.29	15.29	15.29	15.29	15.29	15.29	15.29		1.9	2.0

4.1.4 Power Consumption with 10% of Rated Load

V_{IN} [V_{RMS}]	85	110	130	150	180	210	230	240	265	85
P_{IN} [W]	0.671	0.675	0.678	0.68	0.695	0.7	0.71	0.72	0.73	0.671
P_{OUT} [W]	0.457	0.457	0.457	0.457	0.457	0.458	0.458	0.46	0.46	0.457
P_{STDBY} [W]	0.214	0.218	0.221	0.223	0.238	0.242	0.252	0.26	0.27	0.214



4.1.5 Accuracy of Output Voltage with 10% of Rated Load

The minimum and maximum values in the table below are calculated as deviations from the output voltage as specified in section 1.2.

V_{IN} [V_{RMS}]	85	110	130	150	180	210	230	240	265		**Min [%]**	**Max [%]**
V_1 [V]	15.24	15.24	15.23	15.24	15.25	15.26	15.27	15.27	15.27		1.6	1.8

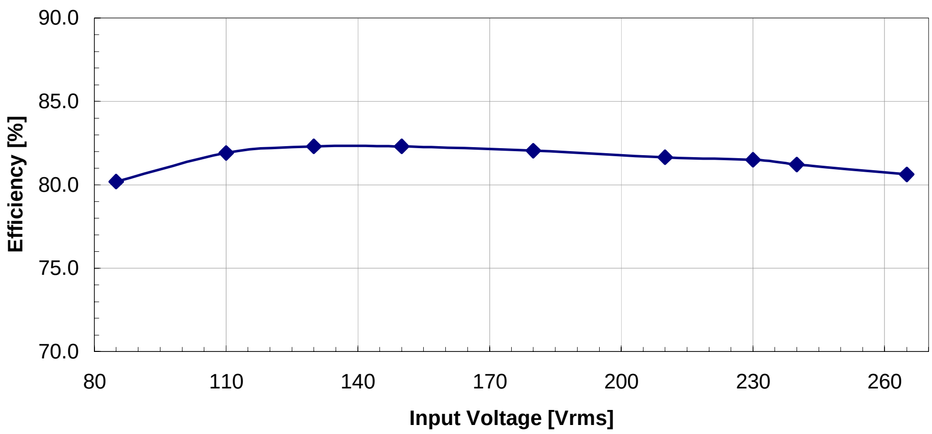
4.2 Full Load Efficiency vs Input Voltage

4.2.1 Test Condition and Method

The power supply was set up with its output loaded at rated load.The input voltage was swept across the specified range. The output load was kept constant. The input power was measured and efficiency calculated.

4.2.2 Result

V_{IN} [V_{RMS}]	85	110	130	150	180	210	230	240	265
P_{OUT} [W]	4.56	4.53	4.51	4.49	4.46	4.43	4.41	4.40	4.38
P_{IN} [W]	5.68	5.53	5.48	5.45	5.43	5.42	5.41	5.42	5.43
Efficiency [%]	80.2	81.9	82.3	82.3	82.1	81.6	81.5	81.2	80.6



4.3 Line Regulation

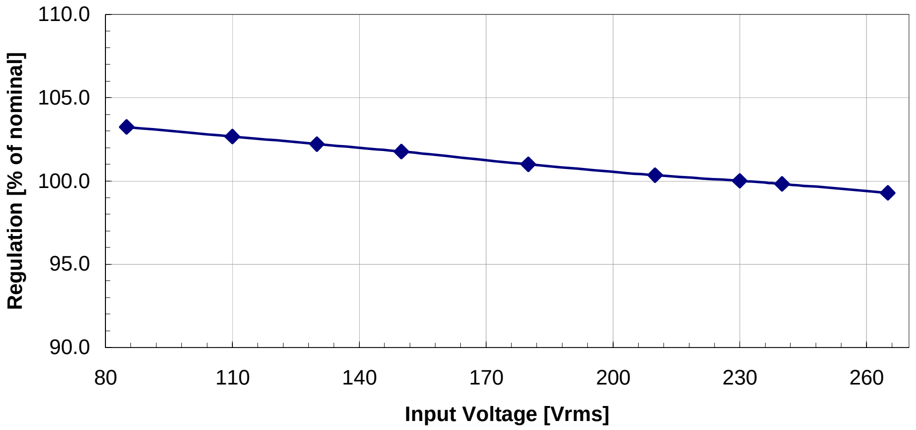
4.3.1 Test Condition and Method

The power supply was set up with the output loaded at rated load. The input voltage was swept across its specified range. Output voltage was measured for each input voltage and was displayed relative to the nominal output voltage. The nominal voltage in this case is the voltage measured at $V_{IN} = 230V_{RMS}$.

4.3.2 Result

The minimum and maximum values in the table below are calculated as deviations from the output voltage as specified in section 1.2.

V_{IN} [V_{RMS}]	85	110	130	150	180	210	230	240	265		**Min [%]**	**Max [%]**
V_1 [V]	15.18	15.09	15.03	14.96	14.85	14.75	14.70	14.67	14.59		-2.2	1.2



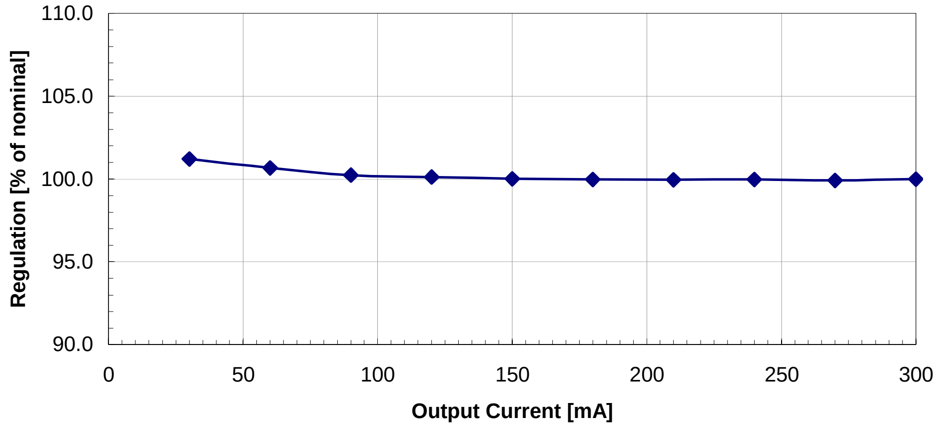
4.4 Load Regulation

4.4.1 Test Condition and Method

The load current of the output is swept from 10% to 100% of rated current. These measurements are done with 110V_{RMS} and 230V_{RMS} input voltage respectively. The results are displayed normalized to the voltages measured when the output is at 100% load.

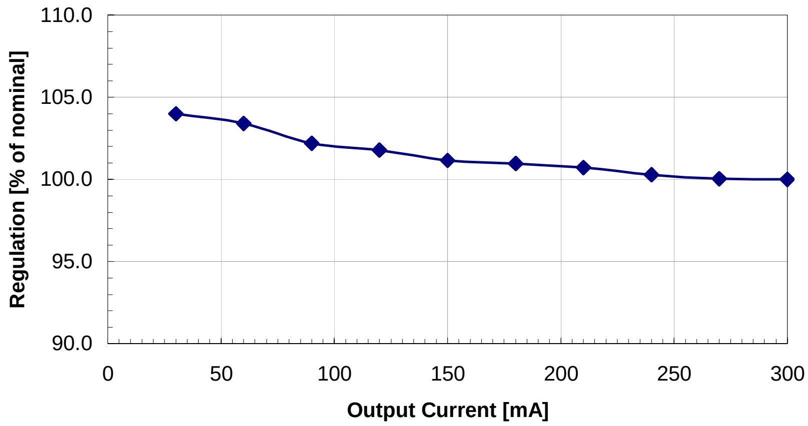
4.4.2 Result for V_{in} = 110V_{RMS}

I_1 [mA]	30	60	90	120	150	180	210	240	270	300
V_1 [V]	15.27	15.19	15.12	15.10	15.09	15.08	15.08	15.08	15.07	15.09



4.4.3 Result for V_{in} = 230V_{RMS}

I_1 [mA]	30	60	90	120	150	180	210	240	270	300
V_1 [V]	15.28	15.20	15.02	14.96	14.87	14.84	14.80	14.74	14.70	14.70



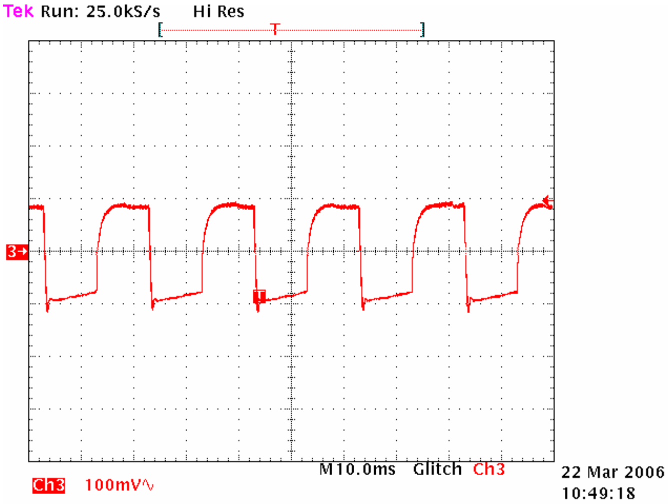
4.5 Dynamic Response of Output

4.5.1 Test condition and Method

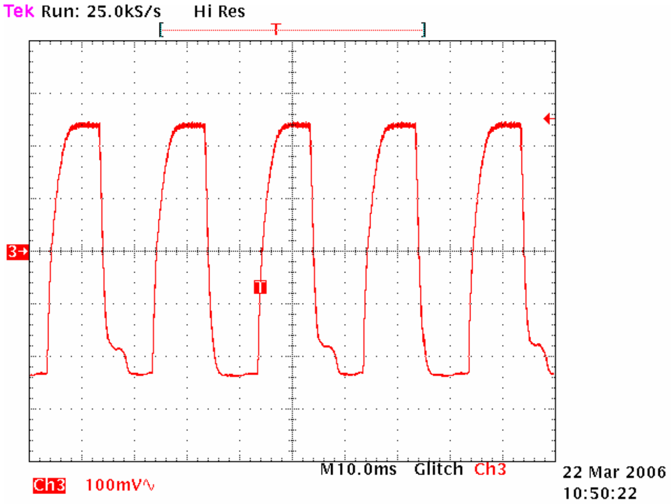
A periodically changing load stepped from 10% to 90% of rated current was connected to the output in test. A repetition frequency of 50Hz and a duty-cycle of 50% were used. The test was performed with an input voltage of $110V_{RMS}$ and $230V_{RMS}$ respectively.

4.5.2 Result

Result for V_{IN}=$110V_{RMS}$



Result for V_{IN}=$230V_{RMS}$



Ch3: V_1 (15V) @ 100mV/div, Timebase @ 10ms/div

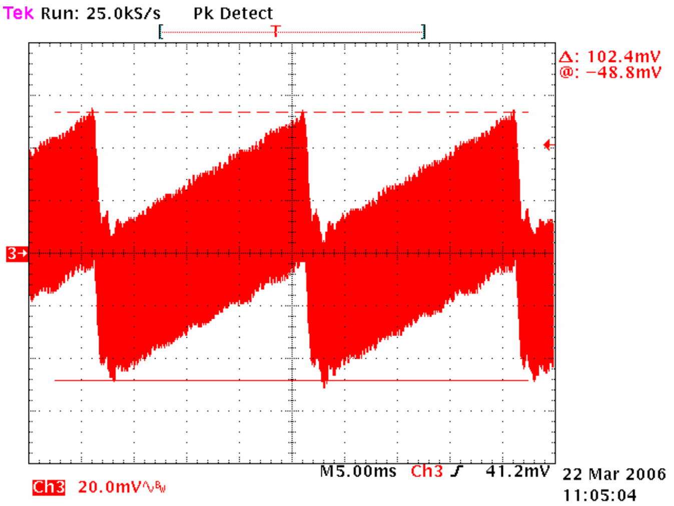
4.6 Output Ripple & Noise

4.6.1 Test Condition and Method

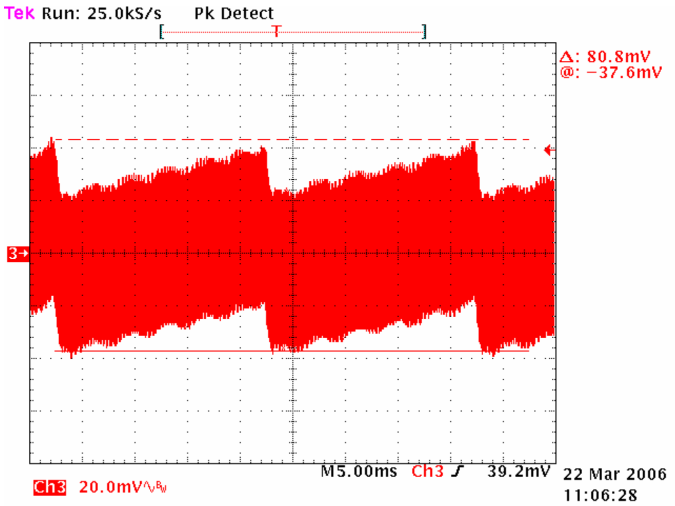
The output was loaded at the rated load. The so-called PARD (periodic and random disturbance) method was used to measure ripple and noise voltages. See for example Celestica application note AN-1259-1-R2. **IMPORTANT NOTE**: Output voltage ripple measurements cannot be made using a normal oscilloscope probe set-up. Magnetic field coupling into the ground connection for the oscilloscope probe could cause noise voltages far greater than the true ripple voltage. The test was performed with an input voltage of 110V_{RMS} and 230V_{RMS} respectively.

4.6.2 Result

Result for V_{IN}=110V_{RMS}



Result for V_{IN}=230V_{RMS}



Ch3: V_1 (15V) @ 20mV/div, Timebase @ 5ms/div

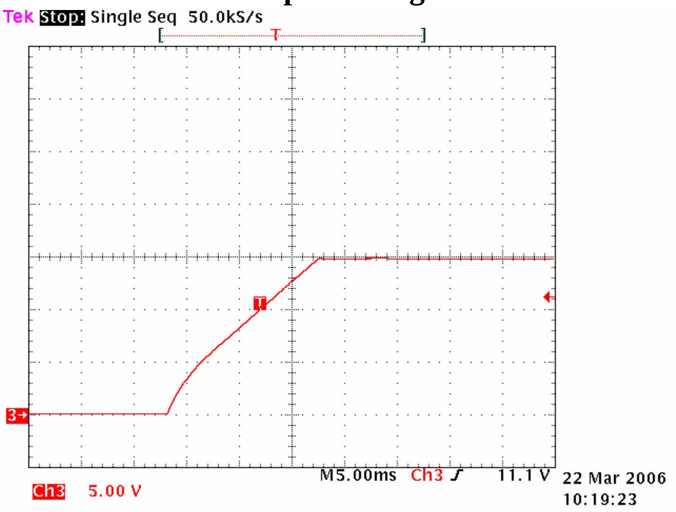
4.7 FPS Soft Start Test

4.7.1 Test Condition and Method

The output was loaded at the rated load. The voltage on the output as well as the drain voltage and current of the FPS were measured during a power up sequence. The test was performed with an input voltage of $110V_{RMS}$ and $230V_{RMS}$ respectively.

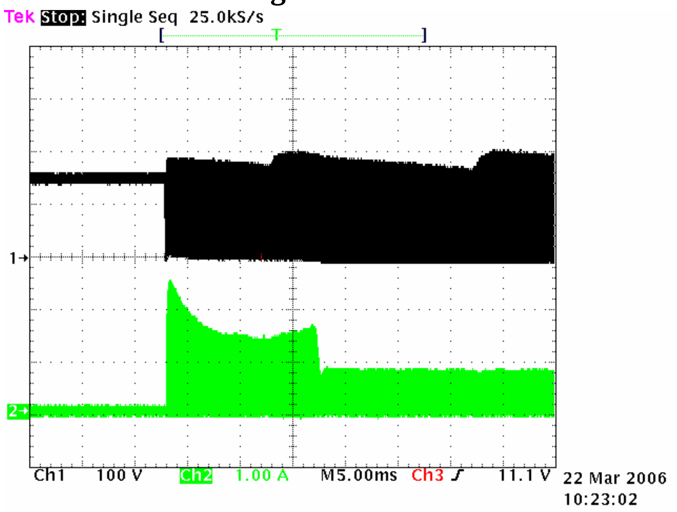
4.7.2 Result for $V_{in} = 110V_{RMS}$

Output Voltage



Ch3: V_1 (15V) @ 5V/div, Timebase @ 5ms/div

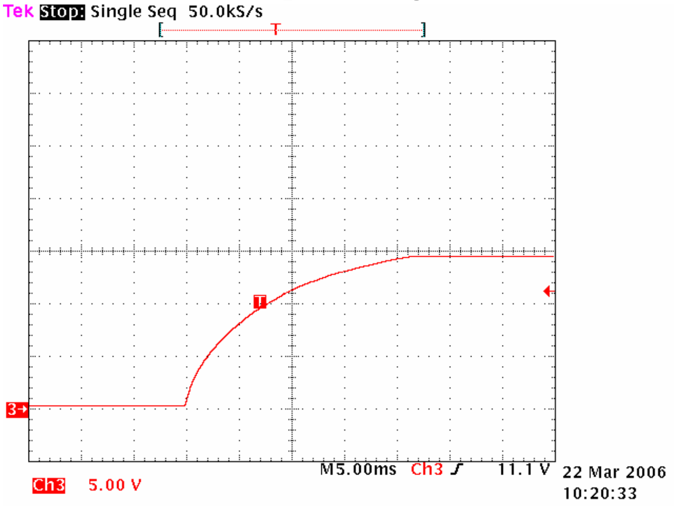
Drain Voltage and Drain Current



Ch1: Drain voltage @ 100V/div,
Ch2: Drain current @ 1A/div,
Timebase @ 5ms/div

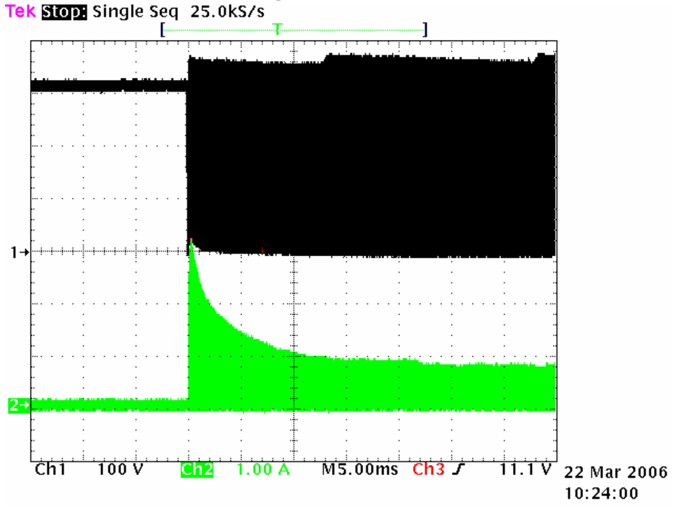
4.7.3 Result for V_{in} = 230V_{RMS}

Output Voltage



Ch3: V_1 (15V) @ 5V/div, Timebase @ 5ms/div

Drain Voltage and Drain Current



Ch1: Drain voltage @ 100V/div,
Ch2: Drain current @ 1A/div,
Timebase @ 5ms/div

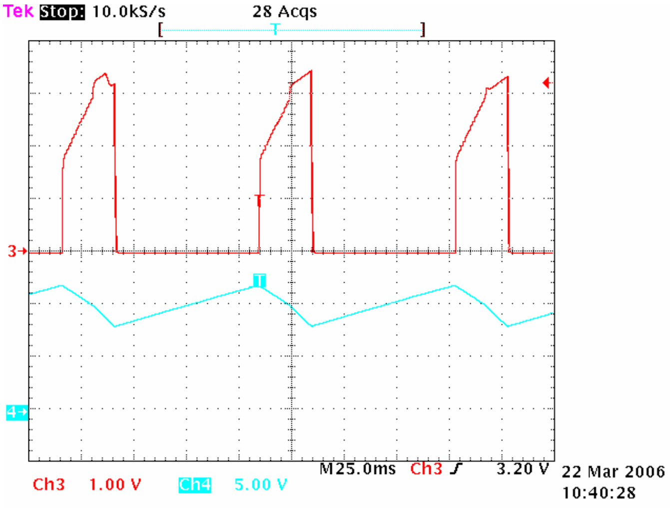
4.8 Output Short Circuit Protection Test

4.8.1 Test Condition and Method

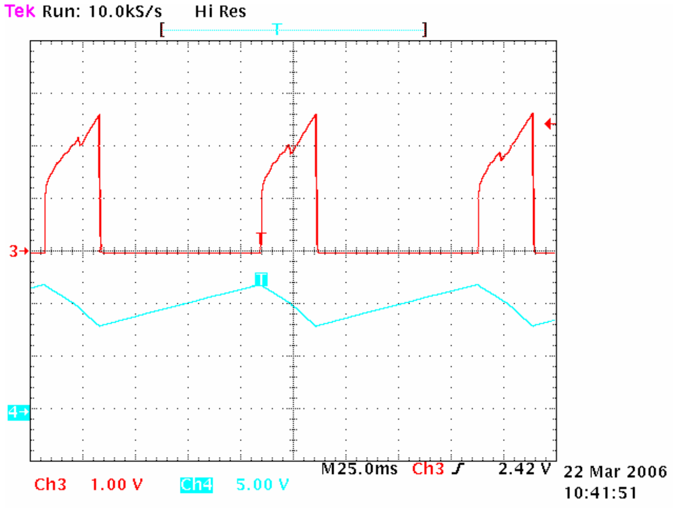
The output was externally short circuited during normal operating mode. The voltages at V_{FB} and V_{CC} were measured. The test was performed with an input voltage of $110V_{RMS}$ and $230V_{RMS}$ respectively.

4.8.2 Result

Result for V_{IN}=$110V_{RMS}$



Result for V_{IN}=$230V_{RMS}$



Ch3: V_{FB} @ 1V/div, Ch4: V_{CC} @ 1V/div, Timebase @ 25ms/div

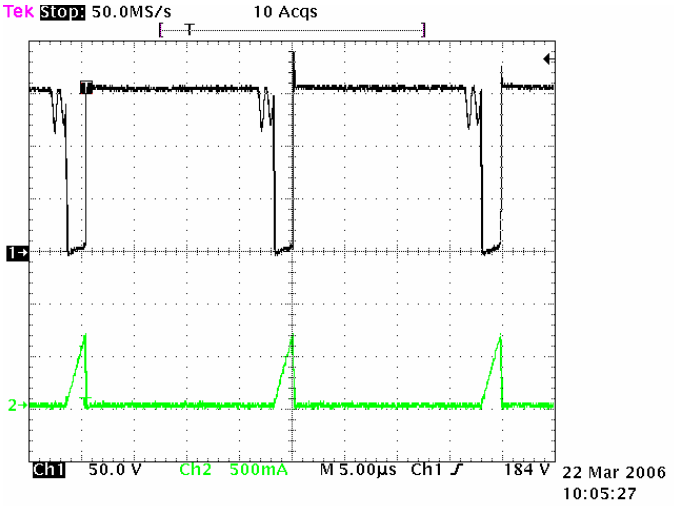
4.9 Typical FPS Drain Waveforms

4.9.1 Test Condition and Method

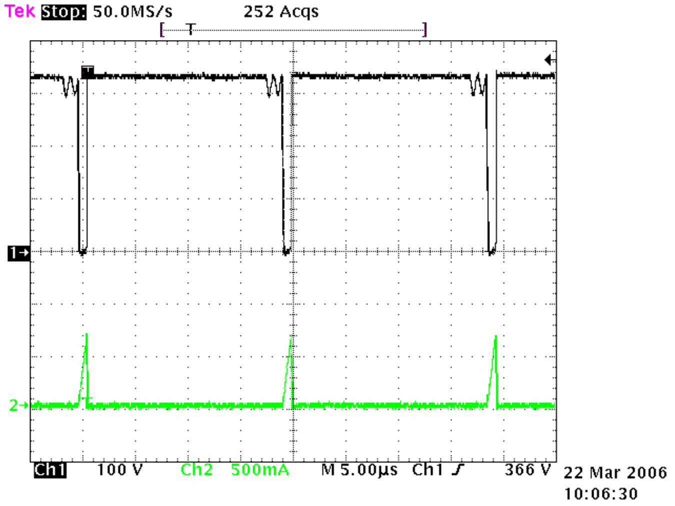
The output was loaded at the rated load. The Drain-Voltage and Drain-Current were measured. The test was performed with an input voltage of $110V_{RMS}$ and $230V_{RMS}$ respectively.

4.9.2 Result

Result for V_{IN}=110V_{RMS}



Result for V_{IN}=230V_{RMS}



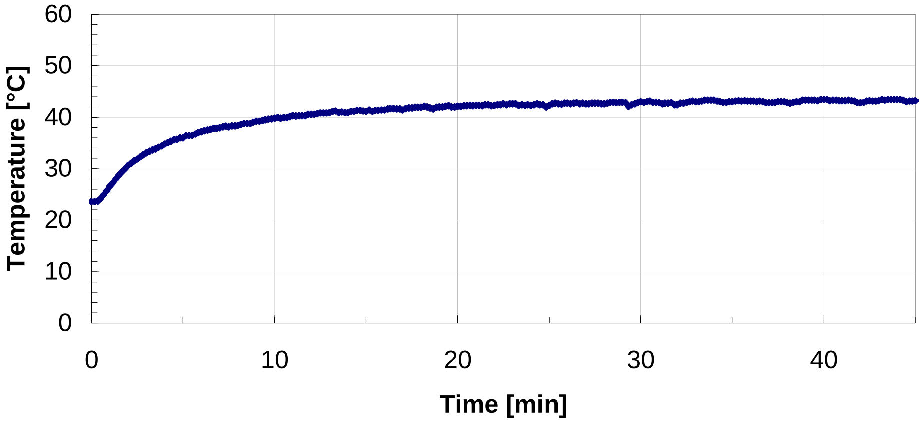
Ch1: Drain Voltage @ 50V/div, Ch2: Drain Current @ 500mA/div, Timebase @ 5µs/div

4.10 Thermal Performance

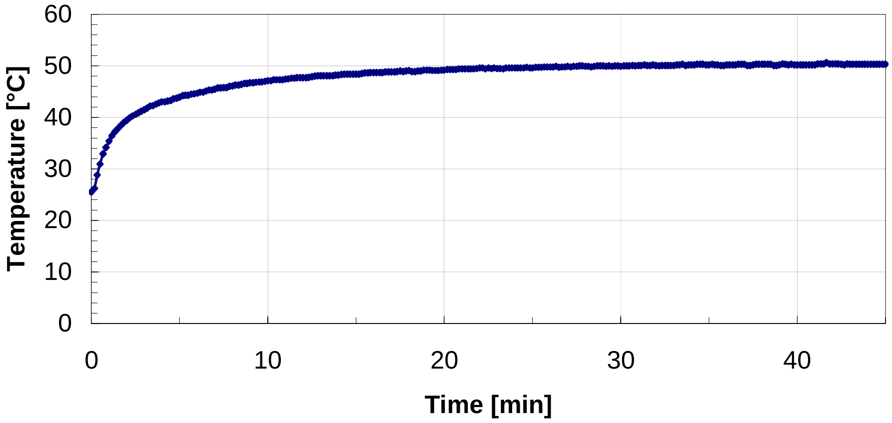
4.10.1 Test Condition and Method

The temperature of the FPS was measured with a thermocouple. The measured temperature was monitored from start up of the PSU until a steady state was recognized. The test was performed with an input voltage of $110V_{RMS}$ and $230V_{RMS}$ respectively under full load conditions. The ambient temperature was 25°C.

4.10.2 Result for V_{IN}=$110V_{RMS}$



4.10.3 Result for V_{IN}=$230V_{RMS}$

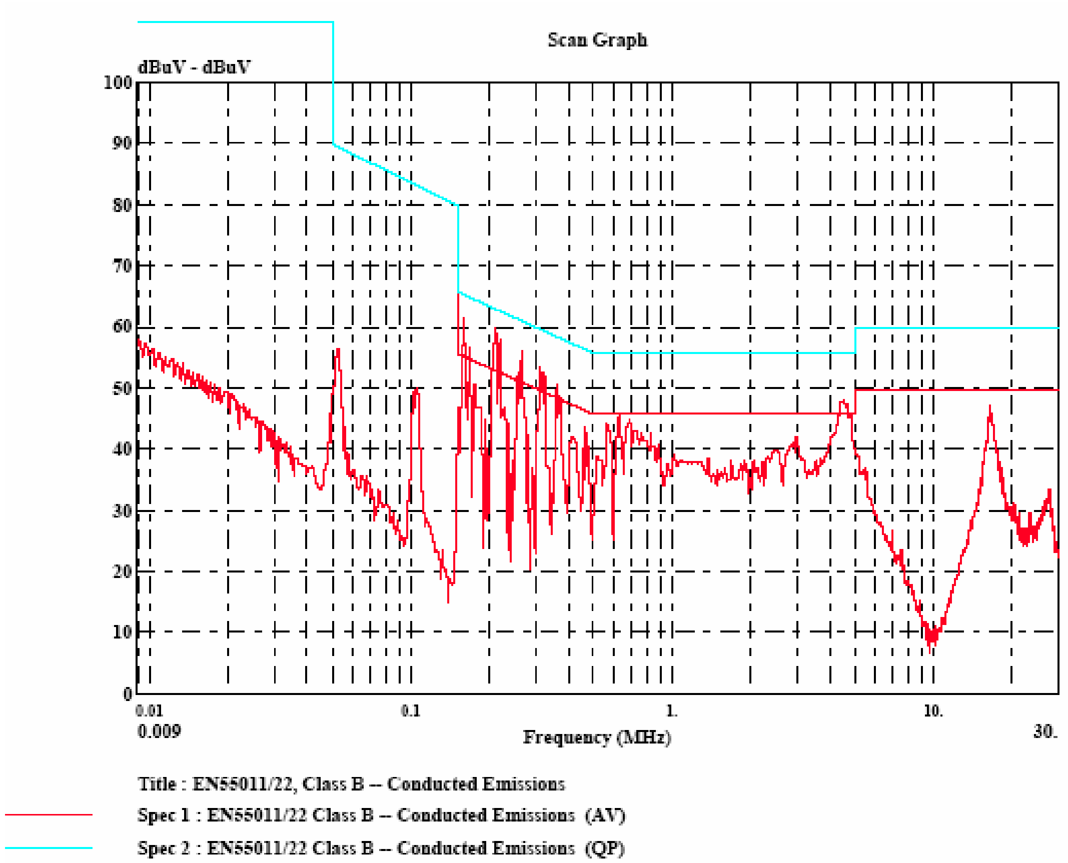


4.11 EMI Tests

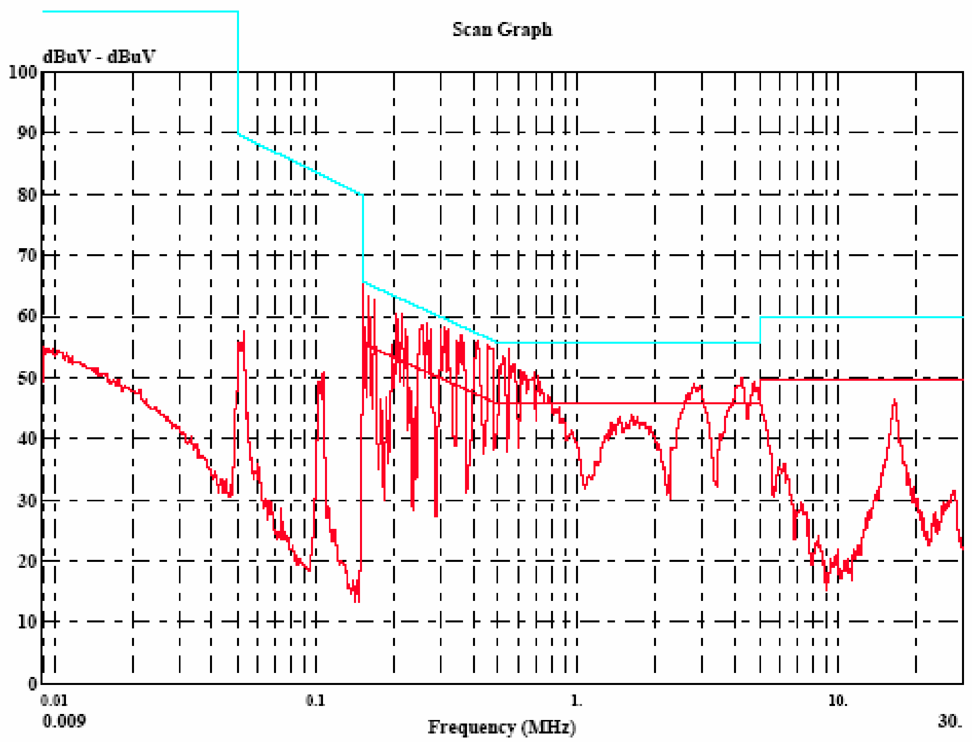
4.11.1 Test Condition

The power supply was set up with the output loaded at rated load. The peak level of the conducted EMI has been measured with the setup given in section 3.0 and is compared to the Quasi-Peak and Average limits given by CISPR 22 (EN55022). Input voltage of $110V_{RMS}$ and $230V_{RMS}$ has been used respectively.

4.11.2 Result for V_{IN}=$110V_{RMS}$



4.11.3 Result for V_{IN}=230V_{RMS}



Title : EN55011/22, Class B -- Conducted Emissions

Spec 1 : EN55011/22 Class B -- Conducted Emissions (AV)

Spec 2 : EN55011/22 Class B -- Conducted Emissions (QP)

5.0 Bill of Materials

Item	Quantity	Reference	Specification	Manufacturer / Type
1	1	CONN1	B2P3-VH	JST
2	1	CONN2	B2P-VH	JST
3	1	C1	22uF/400V	Panasonic ED Series
4	1	C2	100nF/50V	KEMET CK05
5	1	C3	10uF/50V	SAMWHA SD/SG Series
6	1	C4	4.7uF/400V	Rubycon BXC Series
7	1	C5	470uF/35V	Nichicon PW Series
8	1	C6	10nF	Wima MKP-X2
9	2	D1,D2	1N4007	Fairchild Semiconductor
10	1	D3	1N4148	Fairchild Semiconductor
11	2	D4,D5	15V / 0.5W	Fairchild Semiconductor
12	1	D6	UF4004	Fairchild Semiconductor
13	1	FS1	230V / T1A	Wickmann TR5
14	1	IC1	FSDL0165RNB	Fairchild Semiconductor
15	1	L1	6.8mH / 0.26A	Coilcraft RFB1010
16	1	L2	390uH / 1.3A	Coilcraft RFB1010
17	1	Q1	BC337-25	Fairchild Semiconductor
18	1	R1	(not used)	any
19	1	R2	1K / 0.6W	any
20	1	R3	120R / 0.6W	any

6.0 Printed Circuit Board Special Instructions

Operation of the board:

1. Connect a 0.3ADC load across the output terminal CONN2 (see section 2.4). The load must be capable of dissipating 5W at 15V.
2. Connect a DC voltmeter across the output terminal.
3. Connect an isolated variable AC source (such as a variac) to input terminal CONN1 (see section 2.4).
4. Slowly increase the AC input voltage to at least 85VAC (Do not exceed 265VAC).
5. Confirm that the output voltage increases as the input voltage is increased.
6. As the input voltage approaches very close to 85VAC the Board output should read 15VDC.
7. Remove the AC input and verify that the output voltage has dropped to zero.

Modification of the Board for other output voltages:

Other output voltages higher than 15V can be achieved by replacing D5 with an appropriate ZENER diode. The value of D5 determines the output voltage. However the maximum available output voltage is 0.7 x $V_{in(min)}$ due to the internal duty cycle limit. The maximum output current remains at 0.3A. It is important to keep the supply voltage of IC1 at 15V. Therefore you must use an additional ZENER diode D4 if V_{out} exceeds 15V. The value of D4 is calculated by V_{out} – 15V. For example for a 24V output: 24V – 15V = 9V. In this case use a BZX55C9V1 for D4 and a BZX55C24 for D5.

7.0 Featured Products

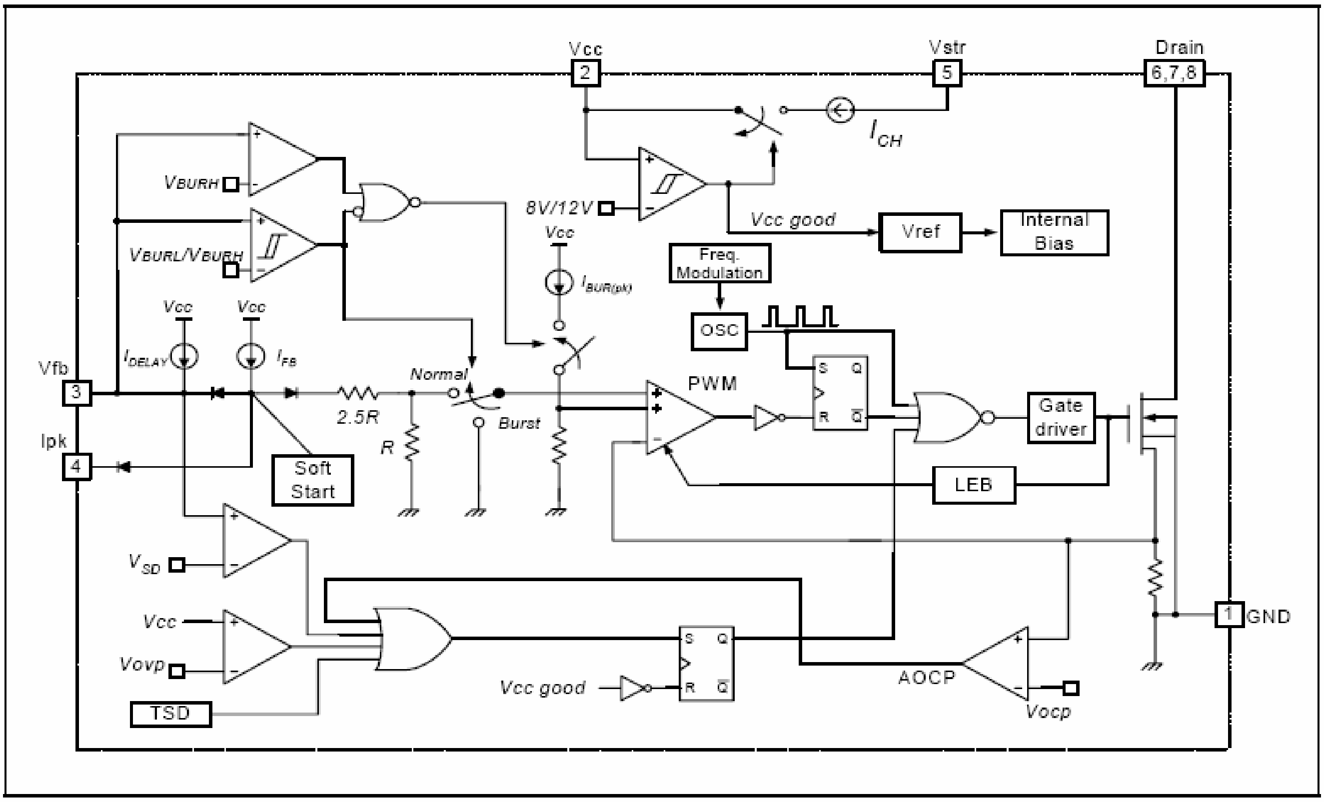
7.1 FSDL0165 Description

The FSDL0165RN consists of an integrated Pulse Width Modulator (PWM) and Sense FET, and is specifically designed for high performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high voltage power switching regulator which combines an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDL0165RN device reduces total component count, design size, weight while increasing efficiency, productivity and system reliability. This device provides a basic platform that is well suited for the design of cost-effective flyback converters.

7.1.1 FSDL0165 Features

- Internal Avalanche Rugged Sense FET
- Consumes only 0.65W at 240VAC & 0.3W load with Advanced Burst-Mode Operation
- Frequency Modulation for EMI Reduction
- Precision Fixed Operating Frequency
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Abnormal Over Current Protection (AOCP)
- Over Voltage Protection (OVP)
- Over Load Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit
- Built-in Soft Start

7.1.2 FSDL0165 Block Diagram



8.0 References and Resources

8.1 Application Notes

Application Note AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS^{TM})
Application Note AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS^{TM})
Application Note AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS^{TM}) Flyback Applications

8.2 Off-Line SMPS Design Tool

Fairchild Semiconductor provides you with easy-to-use design tools that build upon the online Power Supply Design Toolkit interactive tutorials and selector tools. This downloadable, PC Windows (all versions) based program provides you with step-by-step design tools to design a fixed frequency flyback offline power supply and a quasi-resonant converter that helps minimize switching noise. Fairchild Power Switches (FPS^{TM}) are key components in these designs.
It includes the following assistens and tools:

- FPS Flyback Design Assistant
- FPS QRC Design Assistant
- Easy Print-out of Annotated Schematics
- Advanced Database
- Interactive Tutorials

Download at: http://www.fairchildsemi.com/designcenter/acdc/SMPSDT16_Install.zip
NB: This file can be found on the CD-ROM

9.0 Warning and Disclaimer

WARNING AND DISCLAIMER

This Evaluation Board may employ high voltages so appropriate safety precautions should be used when operating this board. Replace components on the Evaluation Board only with those parts shown on the parts list in the User's Guide. Contact an authorized Fairchild representative with any questions. The Evaluation board is for demonstration purposes only and neither the Board nor this User's Guide constitute a sales contract or create any kind of warranty, whether express of implied, as to the applications or products involved. Fairchild warranties that its products will meet Fairchild's published specifications but does not guarantee that its products will work in any specific application. Fairchild reserves the right to makes changes without notice to any products described herein to improve reliability, function, or design. Either the applicable sales contract signed by Fairchild and Buyer, or if no contract exists Fairchild's Stand Terms and Conditions on

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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