DS04-21361-1E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F07SL

■ DESCRIPTION

The Fujitsu MB15F07SL is a serial input Phase Locked Loop (PLL) frequency synthesizer with two 1100 MHz prescalers. The two 1100 MHz prescalers have a dual modulus division ratio of 128/129 or 64/65 enabling pulse swallowing operation.

The supply voltage range is between 2.4 V and 3.6 V. The MB15F07SL uses the latest BiCMOS process. As a result, the supply current is typically 5 mA at 2.7 V. A refined charge pump supplies a well-balanced output current of 1.5 mA or 6 mA. The charge pump current is selectable by serial data.

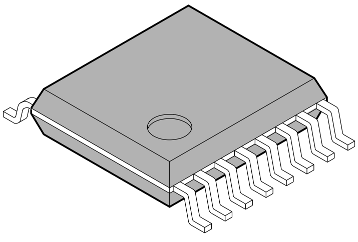
MB15F07SL is ideally suited for wireless mobile communications, such as GSM and PDC.

■ FEATURES

- High frequency operation: PLL 1, 2: 1100 MHz max
- Low power supply voltage: V_{CC} = 2.4 to 3.6 V
- Ultra Low power supply current: I_{CC} = 5.0 mA typ. (V_{CC} = 2.7 V, Ta = +25°C, in PLL1, 2 locking state)
  I_{CC} = 5.5 mA typ. (V_{CC} = 3.0 V, Ta = +25°C, in PLL1, 2 locking state)
- Direct power saving function: Power supply current in power saving mode
  Typ. 0.1 µA (V_{CC} = Vp = 3.0 V, Ta = +25°C), Max. 10 µA (V_{CC} = Vp = 3.0 V)
- Dual modulus prescaler: 1100 MHz prescaler (64/65, 128/129)
- Serial input 14-bit programmable reference divider: R = 3 to 16,383
- Serial input programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 3 to 2,047
- Software selectable charge pump current
- On-chip phase control for phase comparator
- Operating temperature: Ta = –40 to +85°C

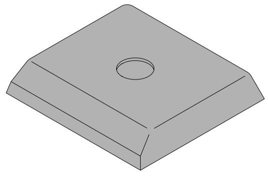
■ PACKAGES

16-pin, Plastic SSOP



(FPT-16P-M05)

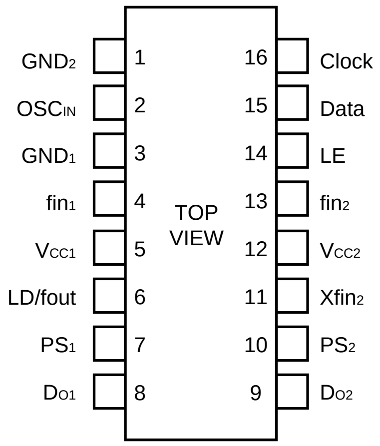
16-pad, Plastic BCC



(LCC-16P-M03)

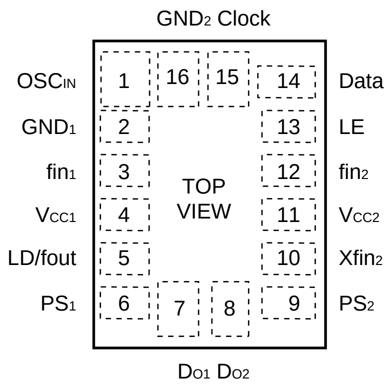
■ PIN ASSIGNMENTS

16-pin SSOP



(FPT-16P-M05)

16-pad BCC

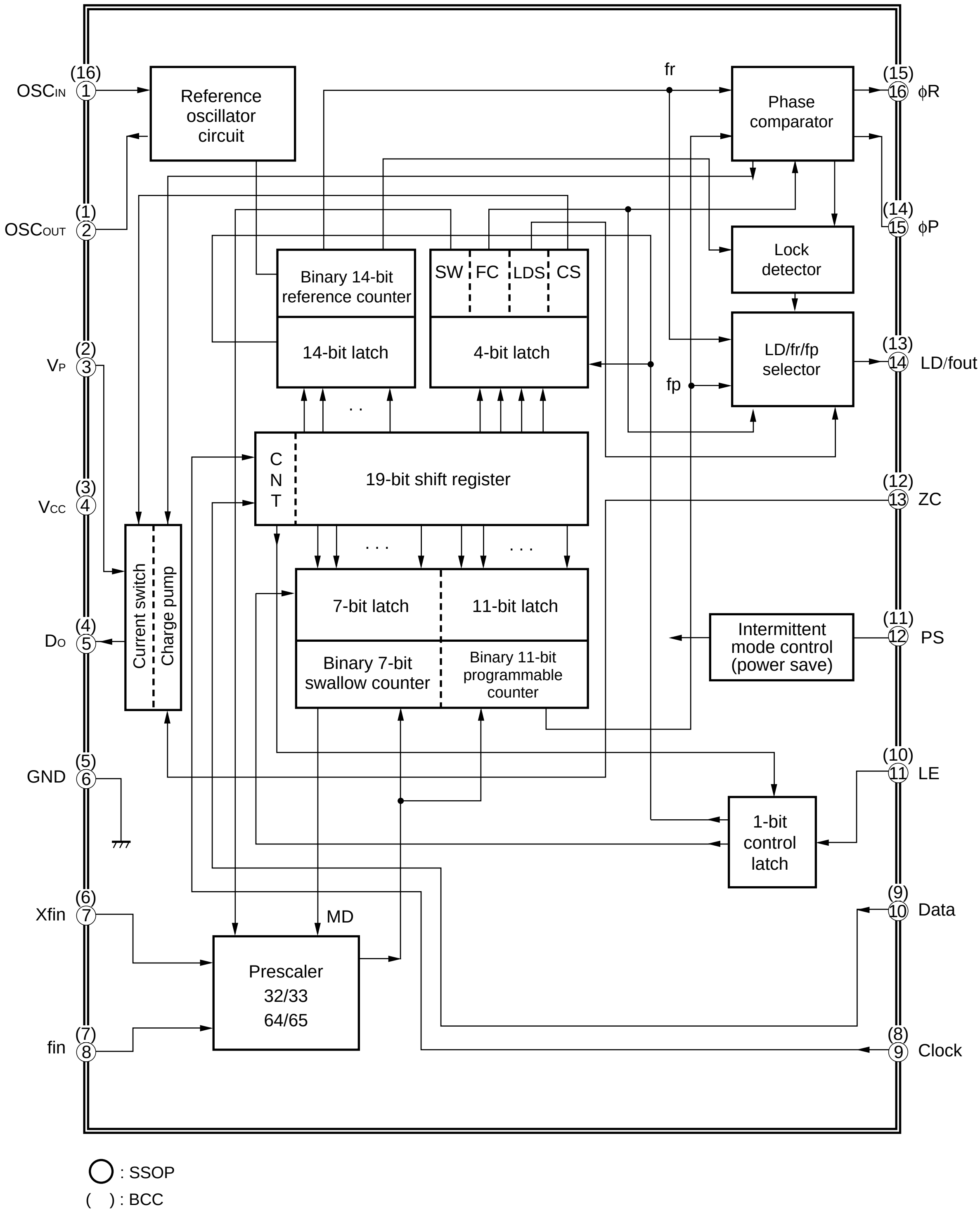


(LCC-16P-M03)

■ PIN DESCRIPTIONS

Pin no.		Pin name	I/O	Descriptions
SSOP	BCC			
1	16	GND_2	–	Ground for PLL 2 section.
2	1	OSC_{IN}	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.
3	2	GND_1	–	Ground for the PLL 1 section.
4	3	fin_1	I	Prescaler input pin for the PLL 1. Connection to an external VCO should be via AC coupling.
5	4	V_{CC1}	–	Power supply voltage input pin for the PLL 1 section.
6	5	LD/fout	O	Lock detect signal output (LD)/phase comparator monitoring output (fout). The output signal is selected by LDS bit in a serial data. LDS bit = “H” ; outputs fout signal LDS bit = “L” ; outputs LD signal
7	6	PS_1	I	Power saving mode control for the PLL 1 section. This pin must be set at “L” during Power-ON. (Open is prohibited.) PS_1 = “H” ; Normal mode PS_1 = “L” ; Power saving mode
8	7	Do_1	O	Charge pump output for the PLL 1 section. Phase characteristics of the phase detector can be selected via programming of the FC-bit.
9	8	Do_2	O	Charge pump output for the PLL 2 section. Phase characteristics of the phase detector can be selected via programming of the FC-bit.
10	9	PS_2	I	Power saving mode control for the PLL 2 section. This pin must be set at “L” during Power-ON. (Open is prohibited.) PS_2 = “H” ; Normal mode PS_2 = “L” ; Power saving mode
11	10	$Xfin_2$	I	Prescaler complementary input for the PLL 2 section. This pin should be grounded via a capacitor.
12	11	V_{CC2}	–	Power supply voltage input pin for the PLL 2 section, the shift register and the oscillator input buffer. When power is OFF, latched data of PLL 2 is lost.
13	12	fin_2	I	Prescaler input pin for the PLL 2. Connection to an external VCO should be via AC coupling.
14	13	LE	I	Load enable signal inpunt (with a schmitt trigger input buffer.) When the LE bit is set “H”, data in the shift register is transferred to the corresponding latch according to the control bit in the serial data.
15	14	Data	I	Serial data input (with a schmitt trigger input buffer.) Data is transferred to the corresponding latch (PLL 1-ref counter, PLL 1-prog. counter, PLL 2-ref. counter, PLL 2-prog. counter) according to the control bit in the serial data.
16	15	Clock	I	Clock input for the 23-bit shift register (with a schmitt trigger input buffer.) One bit of data is shifted into the shift register on a rising edge of the clock.

■ BLOCK DIAGRAM



O -- SSOP
( ) -- BCC

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remark
		Min.	Max.		
Power supply voltage	V_{CC}	–0.5	+4.0	V	
Input voltage	V_I	–0.5	V_{CC} +0.5	V	
Output voltage	V_O	GND	V_{CC}	V	
Storage temperature	Tstg	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.4	3.0	3.6	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.4 V to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CC}*1	PLL 1, PLL 2 total, $fin_1 = fin_2$ = 1100 MHz, $V_{CC1} = V_{CC2}$ = 2.7 V ($V_{CC1} = V_{CC2}$ = 3.0 V)	–	5.0 (5.5)	–	mA
Power saving current		I_{PS}	$PS_1 = PS_2$ = “L”	–	0.1*2	10	µA
Operating frequency	fin_1*3	fin_1	PLL 1	100	–	1100	MHz
	fin_2*3	fin_2	PLL 2	100	–	1100	MHz
	OSC_{IN}	fosc	–	3	–	40	MHz
Input sensitivity	fin_1	$Vfin_1$	PLL 1, 50 Ω system	–15*8	–	+2	dBm
	fin_2	$Vfin_2$	PLL 2, 50 Ω system	–15*8	–	+2	dBm
	OSC_{IN}	V_{OSC}	–	0.5		V_{CC}	Vp-p
“H” level input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	V_{CC} × 0.7 + 0.4	–	–	V
“L” level input voltage		V_{IL}	Schmitt trigger input	–	–	V_{CC} × 0.3 – 0.4	
“H” level input voltage	PS	V_{IH}	–	V_{CC} × 0.7	–	–	V
“L” level input voltage		V_{IL}	–	–	–	V_{CC} × 0.3	
“H” level input current	Data, Clock, LE, PS	I_{IH}*4	–	–1.0	–	+1.0	µA
“L” level input current		I_{IL}*4	–	–1.0	–	+1.0	
“H” level input current	OSC_{IN}	I_{IH}	–	0	–	+100	µA
“L” level input current		I_{IL}*4	–	–100	–	0	
“H” level output voltage	LD/fout	V_{OH}	V_{CC} = 3.0 V, I_{OH} = –1 mA	V_{CC} – 0.4	–	–	V
“L” level output voltage		V_{OL}	V_{CC} = 3.0 V, I_{OL} = 1 mA	–	–	0.4	
“H” level output voltage	Do_1 Do_2	V_{DOH}	V_{CC} = 3.0 V, I_{DOH} = –0.5 mA	V_{CC} – 0.4	–	–	V
“L” level output voltage		V_{DOL}	V_{CC} = 3.0 V, I_{DOL} = 0.5 mA	–	–	0.4	
High impedance cutoff current	Do_1 Do_2	I_{OFF}	V_{CC} = 3.0 V, V_{OFF} = 0.5 V to V_{CC} – 0.5 V	–	–	2.5	nA
“H” level output current	LD/fout	I_{OH}*4	V_{CC} = 3.0 V	–1.0	–	–	mA
“L” level output current		I_{OL}*4	V_{CC} = 3.0 V	–	–	1.0	

(Continued)

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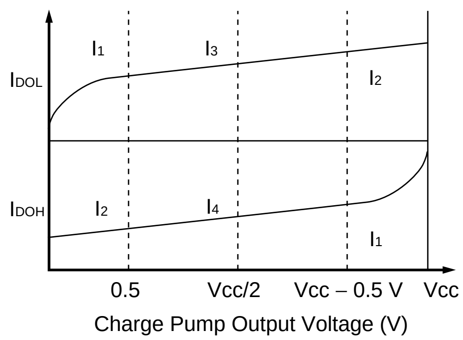
(V_{CC} = 2.4 to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H" level output current	Do_1 Do_2	I_{DOH} *4	V_{CC} = 3.0 V, V_{DOH} = V_{CC}/2, Ta = +25°C	CS bit = "H"	–	–6.0	–	mA
				CS bit = "L"	–	–1.5	–	mA
"L" level output current		I_{DOL}	V_{CC} = 3.0 V, V_{DOL}= V_{CC}/2, Ta = +25°C	CS bit = "H"	–	6.0	–	mA
				CS bit = "L"	–	1.5	–	mA
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT} *5	V_{DO} = V_{CC}/2		–	3	–	%
	vs V_{DO}	I_{DOVD} *6	0.5 V ≤ V_{DO} ≤ V_{CC} – 0.5 V		–	10	–	%
	vs Ta	I_{DOTA} *7	–40°C ≤ Ta ≤ +85°C, V_{DO} = V_{CC}/2		–	10	–	%

*1: Conditions; fosc = 12 MHz, Ta = +25°C, in locking state.
*2: V_{CC1} = V_{CC2} = 3.0 V, fosc = 12.8 MHz, Ta = +25°C, in power saving mode.
*3: AC coupling. 1000pF capacitor is connected under the condition of min. operating frequency.
*4: The symbol "–" (minus) means direction of current flow.
*5: V_{CC} = 3.0 V, Ta = +25°C $(|I_3| - |I_4|)/[(|I_3| + |I_4|)/2] \times 100(\%)$
*6: V_{CC} = 3.0 V, Ta = +25°C $[(|I_2| - |I_1|)/2]/[(|I_1| + |I_2|)/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
*7: V_{CC} = 3.0 V, $[|I_{DO(85°C)} - I_{DO(-40°C)}|/2]/[|I_{DO(85°C)} + I_{DO(-40°C)}|/2] \times 100(\%)$ (Applied to each I_{DOL}, I_{DOH})
*8:

	Prescaler divided ratio	Charge pump current	$Vfin_1$(min)
fin_1	64/65	1.5 mA mode	–10 dBm
		6.0 mA mode	–10 dBm
	128/129	1.5 mA mode	–15 dBm
		6.0 mA mode	–15 dBm

	Prescaler divided ratio	Charge pump current	$Vfin_2$(min)
fin_2	64/65	1.5 mA mode	–15 dBm
		6.0 mA mode	–10 dBm
	128/129	1.5 mA mode	–15 dBm
		6.0 mA mode	–15 dBm



■ FUNCTIONAL DESCRIPTION

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(M \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
M : Preset divide ratio of dual modulus prescaler (64 or 128 for PLL 1/PLL 2)
N : Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC} : Reference oscillation frequency
R : Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of PLL 1/PLL 2 sections, programmable reference dividers of PLL 1/PLL 2 sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of Clock, one bit of serial data is transferred into the shift register. When the LE signal is taken high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table 1. Control Bit

Control bit		Destination of serial data
CN1	CN2	
L	L	The programmable reference counter for the PLL 1
H	L	The programmable reference counter for the PLL 2
L	H	The programmable counter and the swallow counter for the PLL 1
H	H	The programmable counter and the swallow counter for the PLL 2

Shift Register Configuration

Programmable Reference Counter

LSB → Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	CS	X	X	X	X

CN1,2 : Control bit [Table 1]
R1 to R14 : Divide ratio setting bits for the programmable reference counter (3 to 16,383) [Table 2]
T1, 2 : Test purpose bit [Table 3]
CS : Charge pump currnet select bit [Table 9]
X : Dummy bits (Set “0” or “1”)

NOTE: Data input with MSB first.

Programmable Counter

LSB → Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW1/2	FC1/2	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CNT1, 2 : Control bit [Table 1]
N1 to N11: Divide ratio setting bits for the programmable counter (3 to 2,047) [Table 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table 5]
$SW_{1/2}$: Divide ratio setting bit for the prescaler (PLL 1 for the SW_1, PLL 2 for the SW_2) [Table 6]
$FC_{1/2}$: Phase control bit for the phase detector (PLL 1: FC_1, PLL 2: FC_2) [Table 7]
LDS : LD/fout signal select bit [Table 8]
NOTE: Data input with MSB first.

Table 2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table 3. Test Purpose Bit Setting

T 1	T 2	LD/fout pin state
L	L	Outputs fr_1.
H	L	Outputs fr_2.
L	H	Outputs fp_1.
H	H	Outputs fp_2.

Table 4. Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
·	·	·	·	·	·	·	·	·	·	·	·
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table 5. Binary 7-bit Swallow Counter Data Setting

Divide ratio (N)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
·	·	·	·	·	·	·	·
127	1	1	1	1	1	1	1

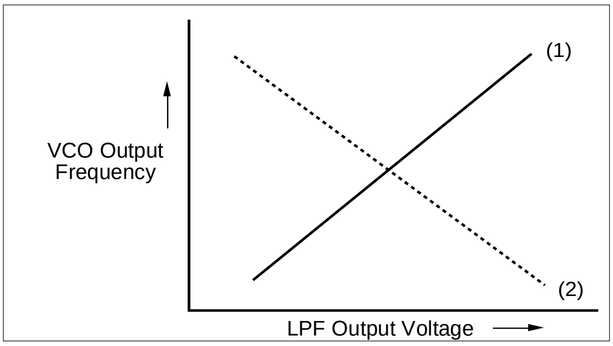
Note: • Divide ratio (A) range = 0 to 127

Table 6. Prescaler Data Setting

		SW = "H"	SW = "L"
Prescaler divide ratio	PLL 1	64/65	128/129
	PLL 2	64/65	128/129

Table 7. Phase Comparator Phase Switching Data Setting

	FC1, 2 = "H"	FC1, 2 = "L"
	Do1, 2	
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	(1)	(2)



Note: • Z = High-impedance
• Depending upon the VCO and LPF polarity, FC bit should be set.

Table 8. LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout ($fr_{1/2}$, $fp_{1/2}$) signals
L	LD signal

Table 9. Charge Pump Current Setting

CS	Current value
H	±6.0 mA
L	±1.5 mA

Power Saving Mode (Intermittent Mode Control Circuit)

Table 10. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

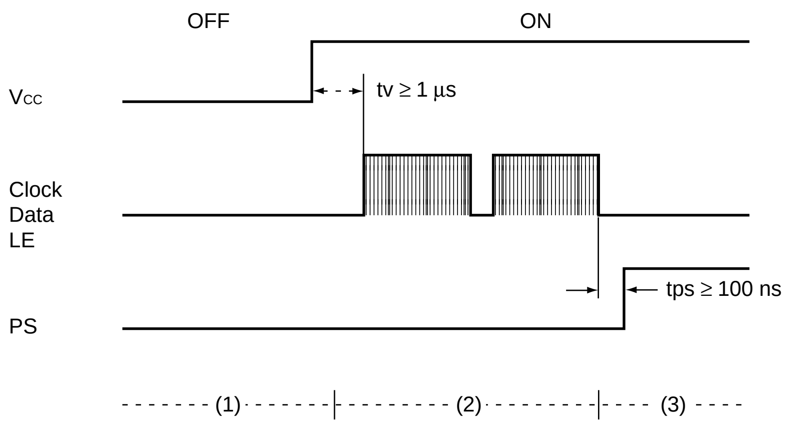
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

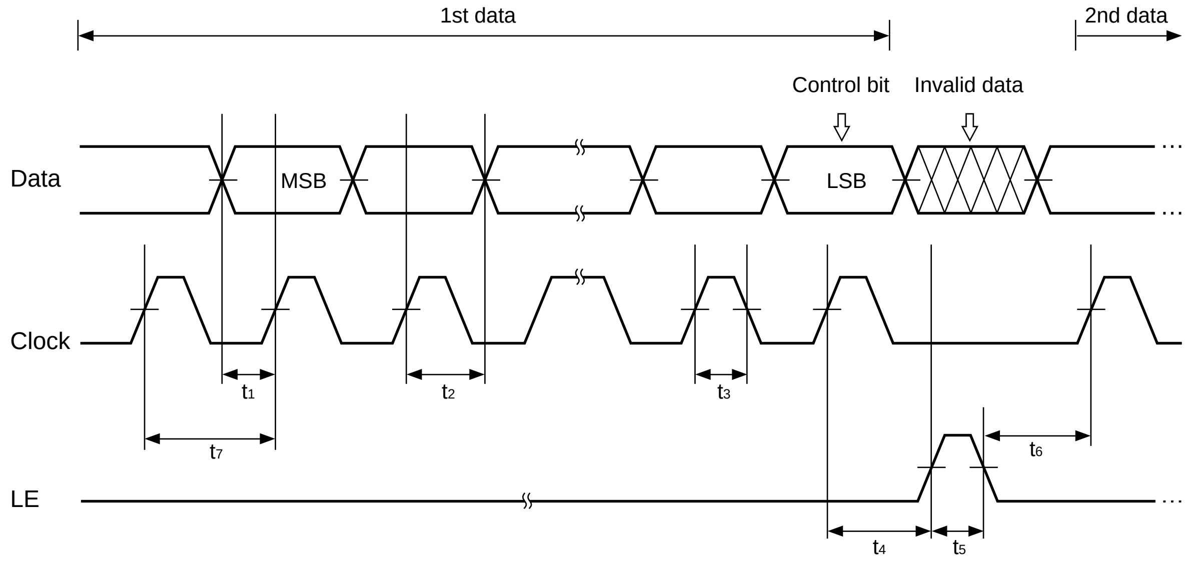
Note: • When power (V_{CC}) is first applied, the device must be in standby mode, PS = Low, for at least 1 µs.

Note: • PS pin must be set at “L” for Power-ON.



(1) PS = L (power saving mode) at Power-ON
(2) Set serial data 1 µs later after power supply remains stable ($V_{CC} \geq 2.2$ V).
(3) Release power saving mode (PS: L → H) 100 ns later after setting serial data.

■ SERIAL DATA INPUT TIMING



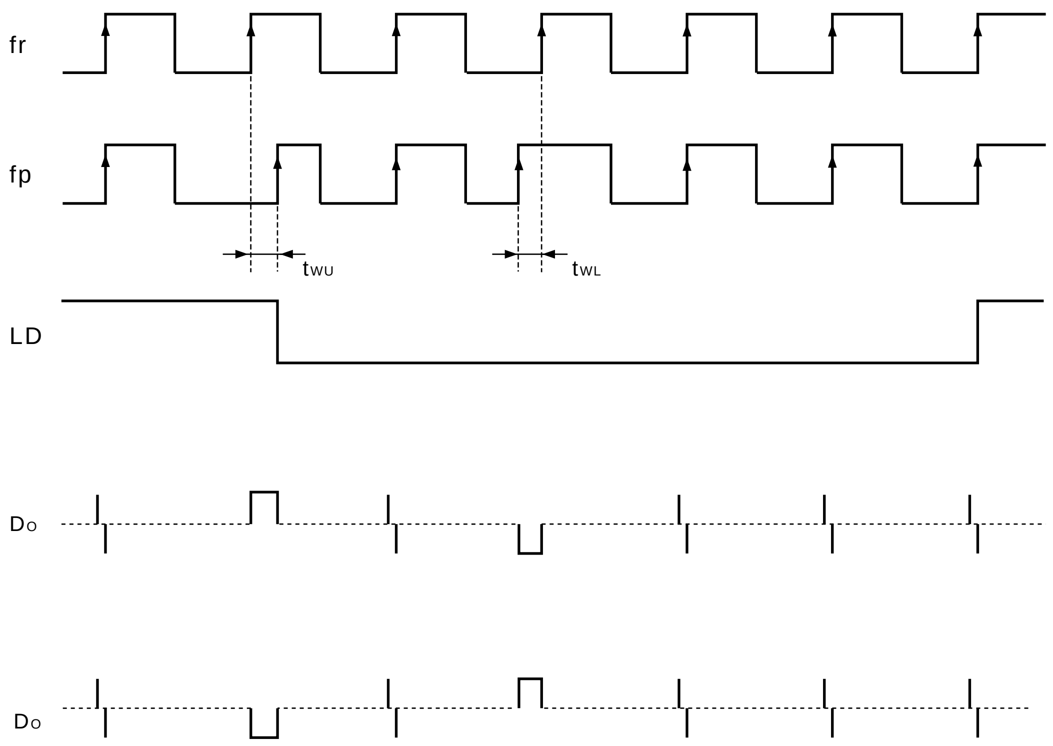
On rising edge of the clock, one bit of the data is transfered into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t_1	20	–	–	ns
t_2	20	–	–	ns
t_3	30	–	–	ns
t_4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t_5	100	–	–	ns
t_6	20	–	–	ns
t_7	100	–	–	ns

Note: LE should be “L” when the data is transferred into the shift register.

■ PHASE COMPARATOR OUTPUT WAVEFORM

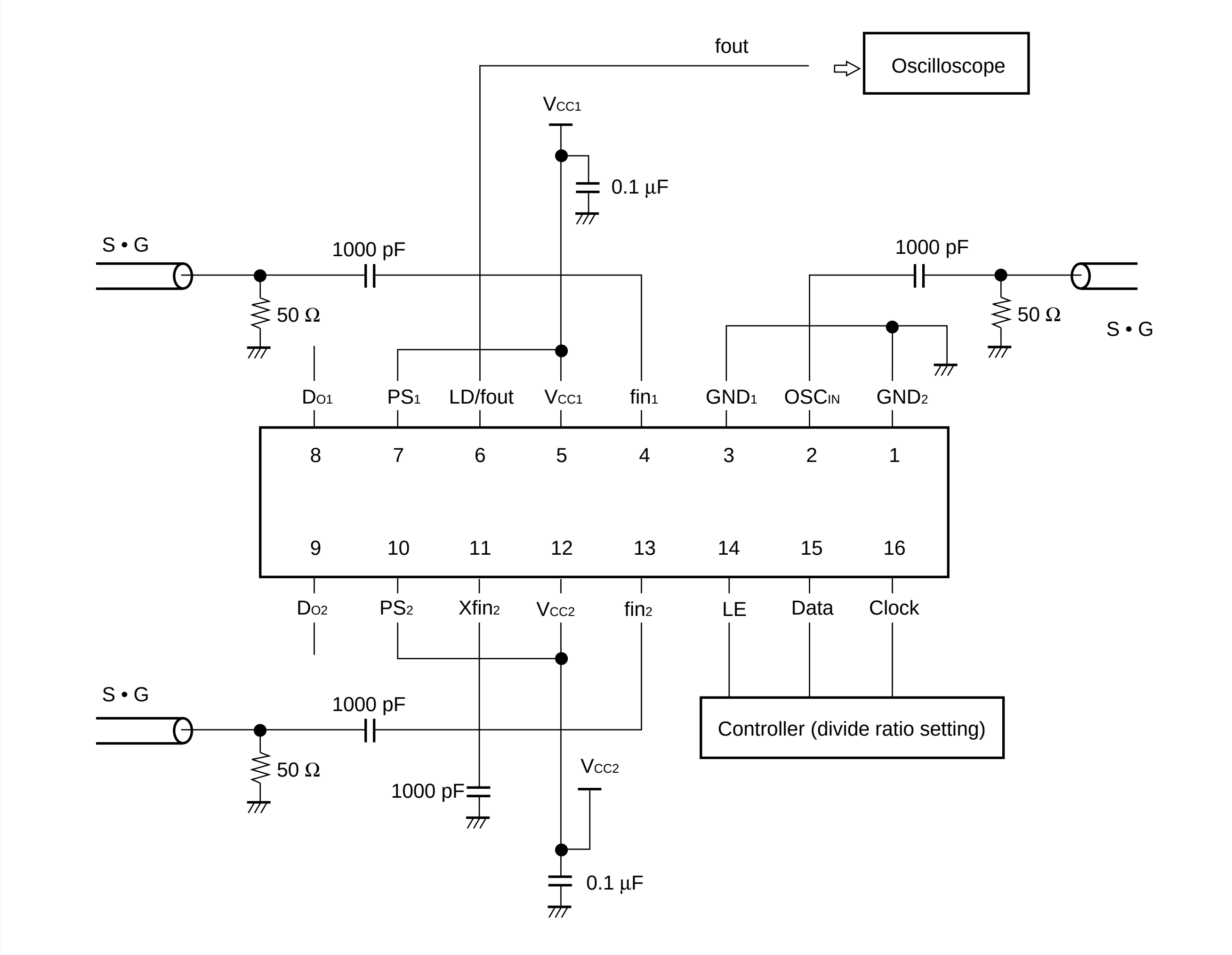


LD Output Logic Table

IF-PLL section	RF-PLL section	LD output
Locking state/Power saving state	Locking state/Power saving state	H
Locking state/Power saving state	Unlocking state	L
Unlocking state	Locking state/Power saving state	L
Unlocking state	Unlocking state	L

Notes:
- Phase error detection range = -2π to $+2\pi$
- Pulses on $Do_{1/2}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSC_{IN} input frequency as follows.
  $t_{WU} \geq$ 2/fosc: i. e. $t_{WU} \geq$ 156.3 ns when foscin = 12.8 MHz
  $t_{WU} \leq$ 4/fosc: i. e. $t_{WL} \leq$ 312.5 ns when foscin = 12.8 MHz

■ MEASURMENT CIRCUIT (for Measuring Input Sensitivity fin/OSCin)

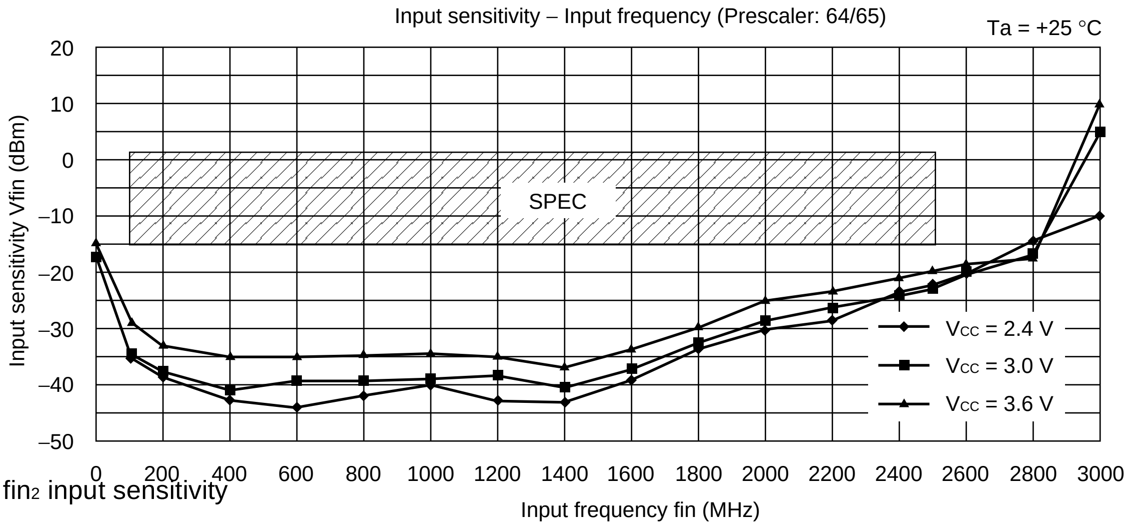


Note: SSOP-16

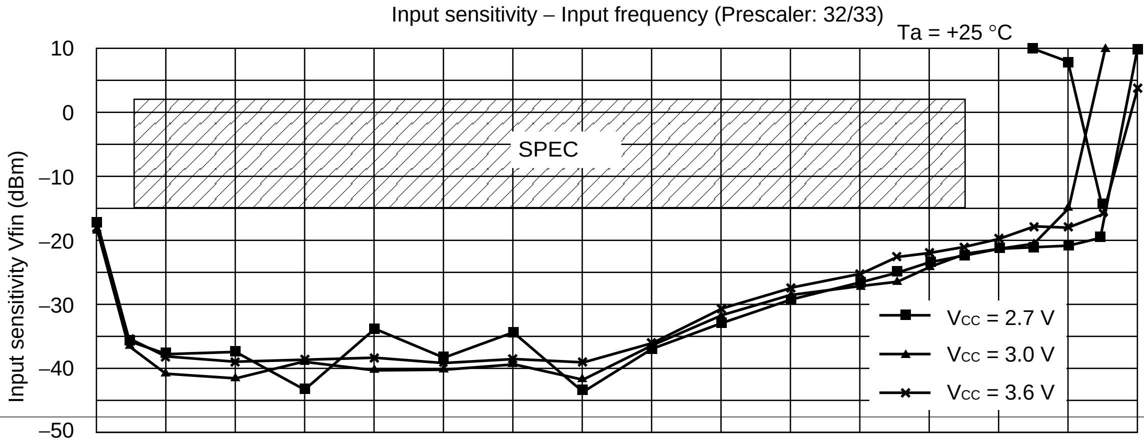
■ TYPICAL CHARACTERISTICS

1. fin input sensitivity

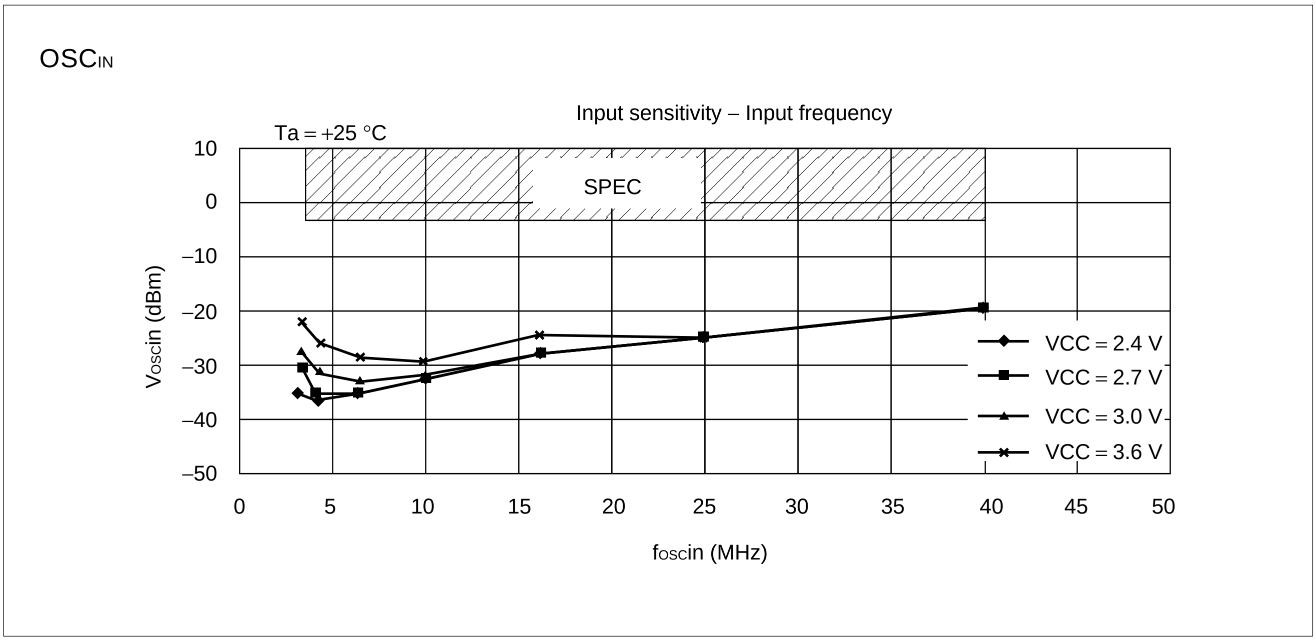
fin1 input sensitivity



fin2 input sensitivity

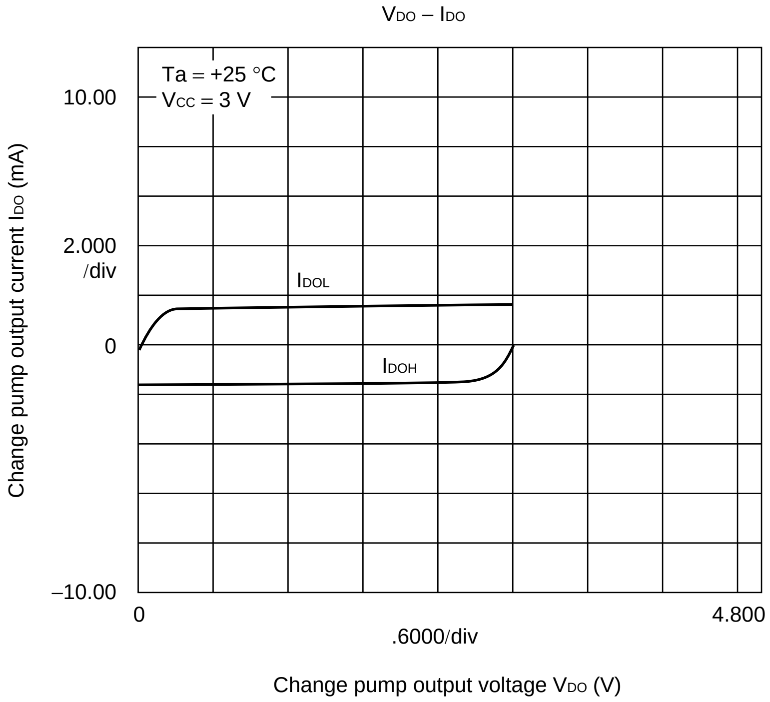


2. OSC_{IN} input sensitivity

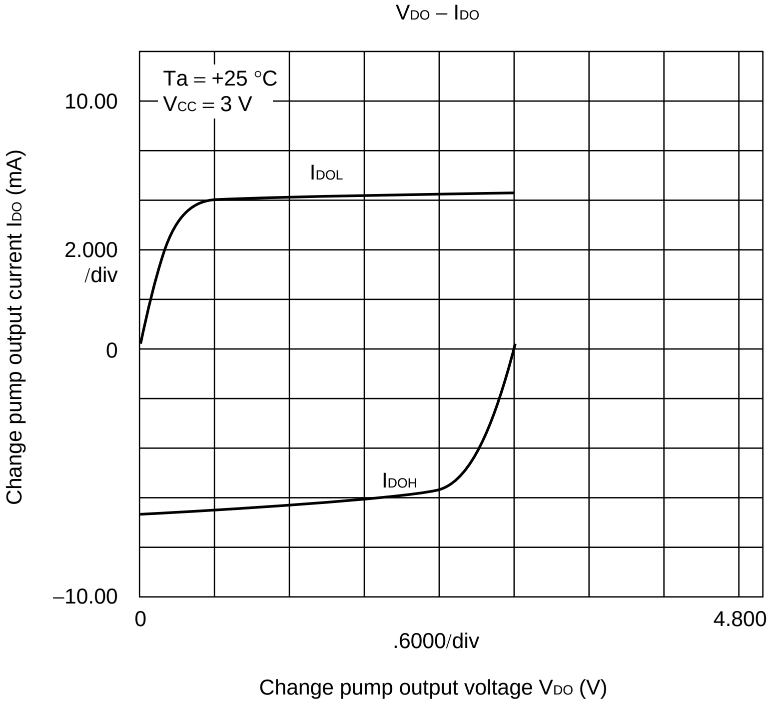


3. Do output current (PLL1)

1.5 mA mode

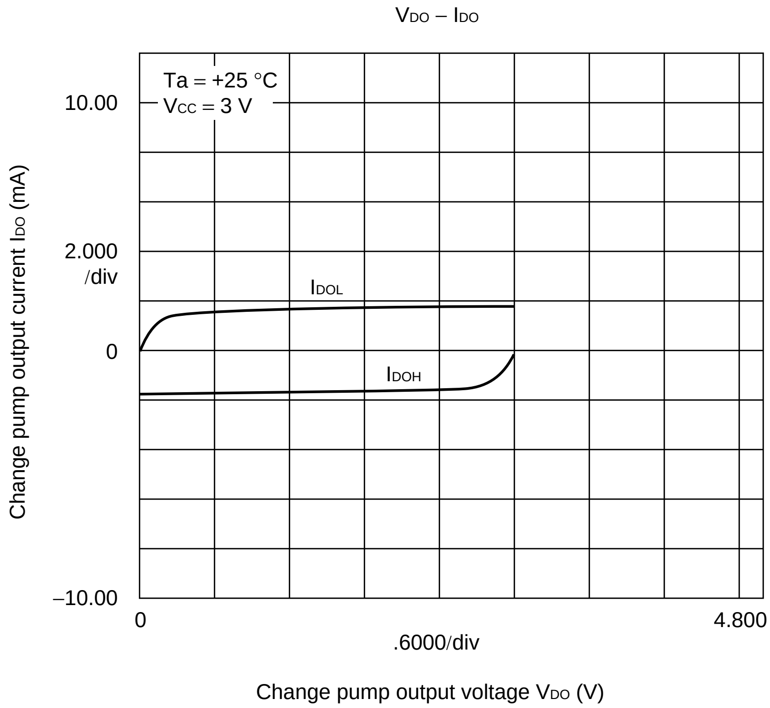


6.0 mA mode

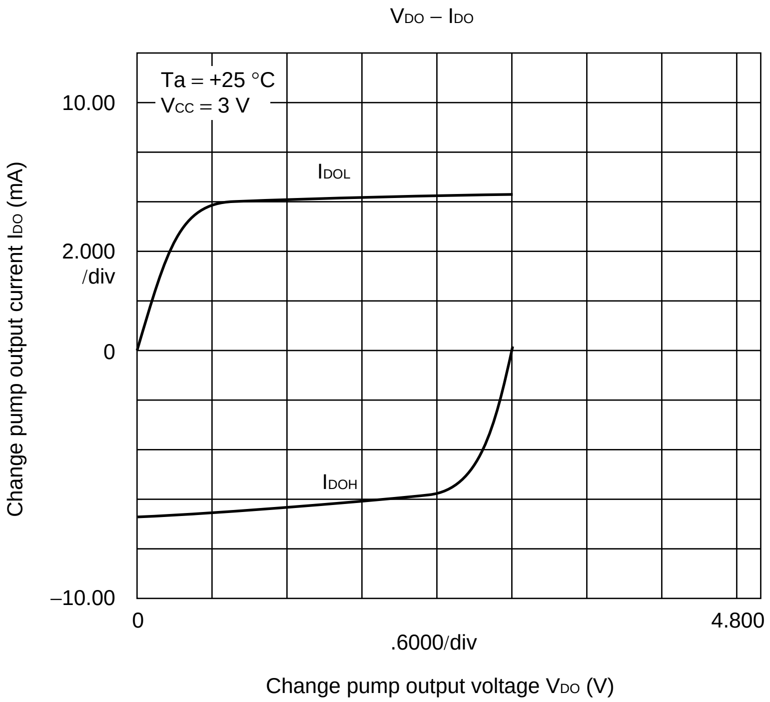


4. Do output current (PLL2)

1.5 mA mode

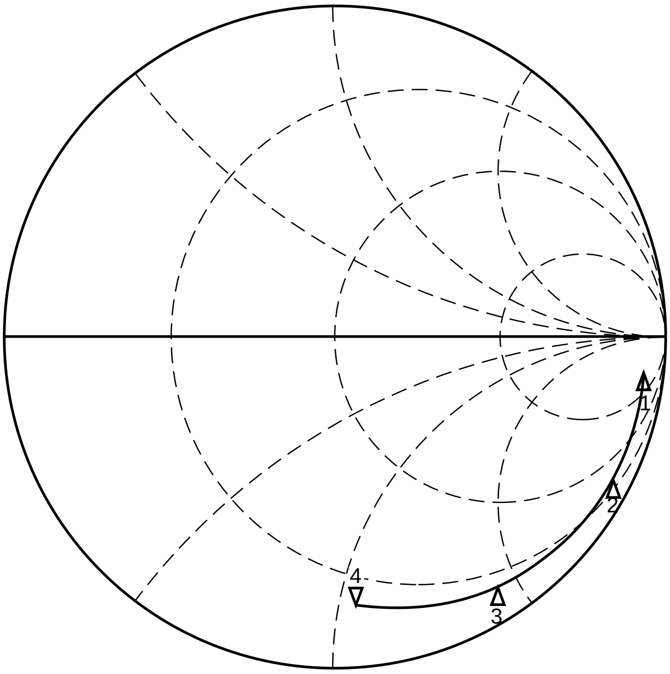


6.0 mA mode



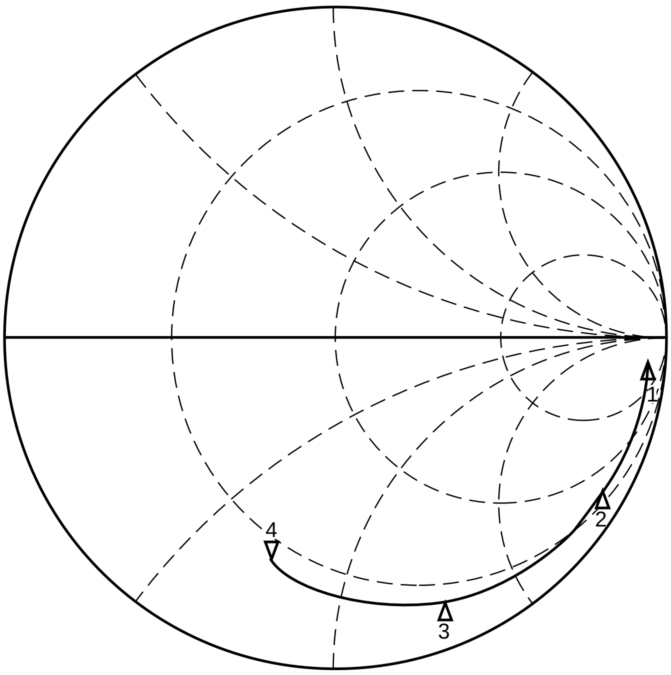
5. fin input impedance

fin1 input impedance



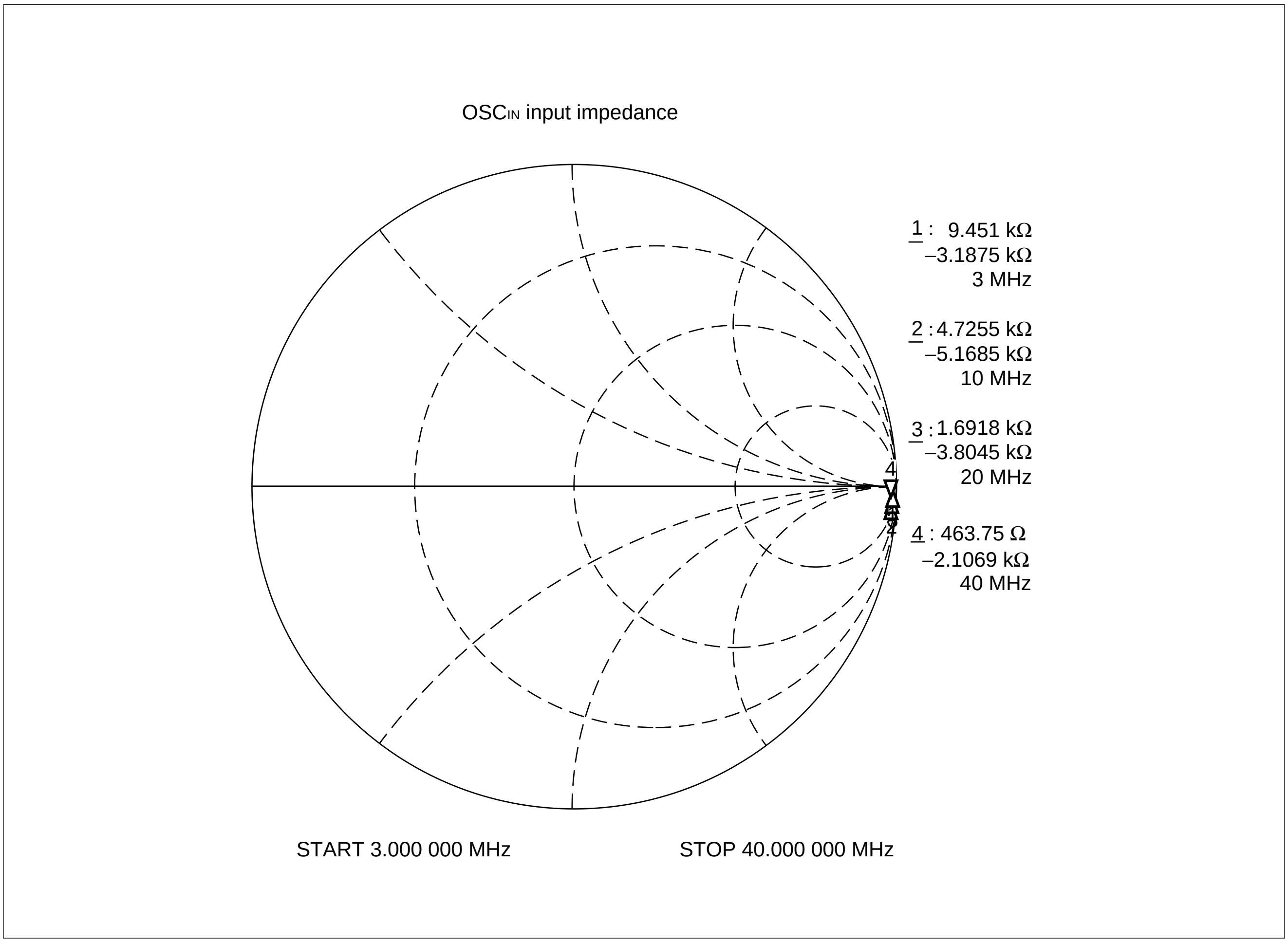
START 100.000 000 MHz STOP 1 100.000 000 MHz

fin2 input impedance

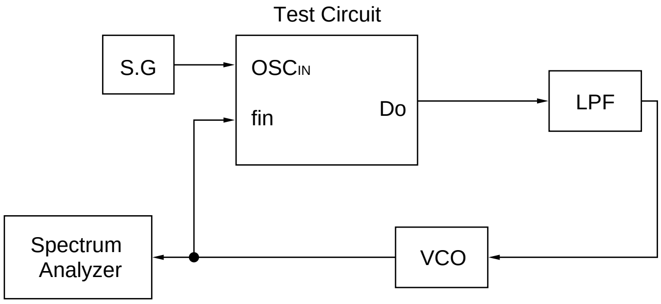


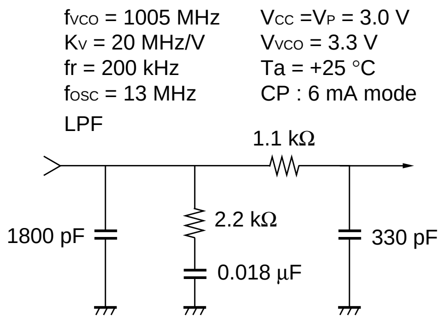
START 100.000 000 MHz STOP 1 100.000 000 MHz

6. OSC$_{IN}$ input impedance

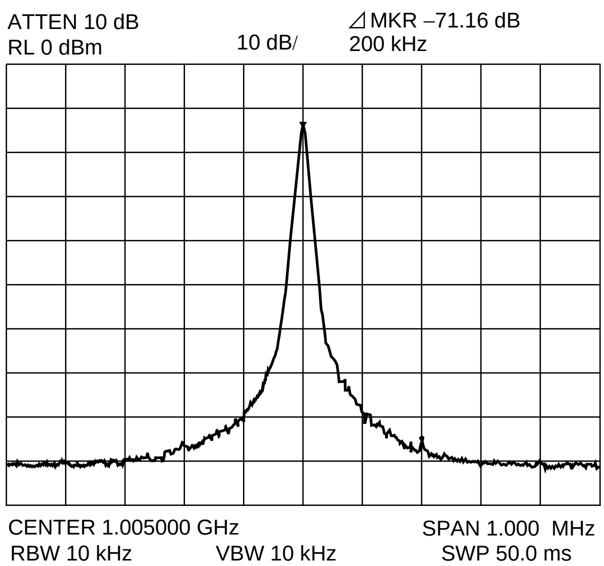


■ REFERENCE INFORMATION

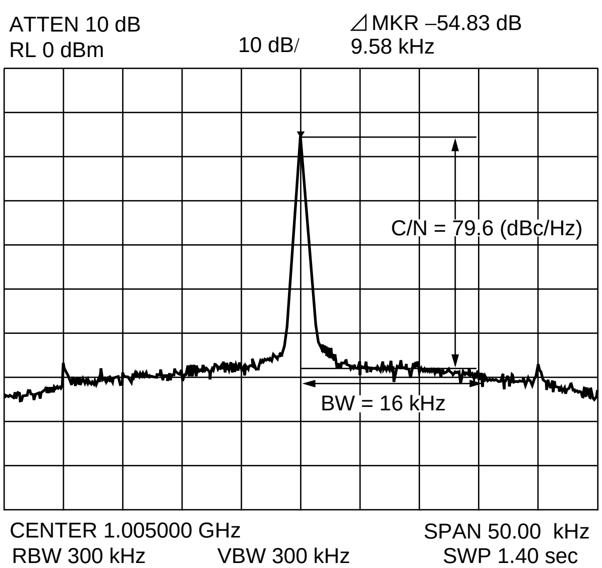




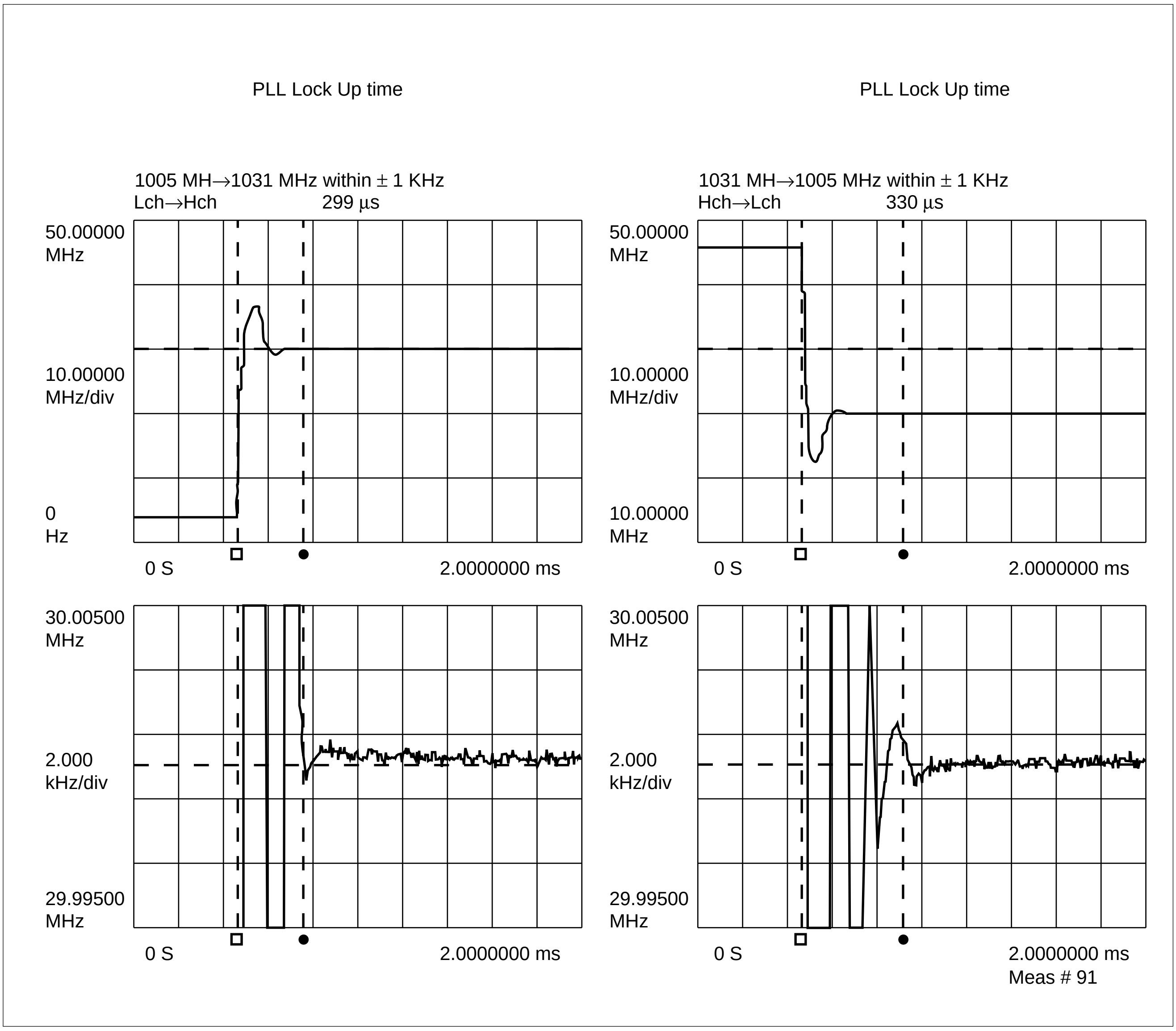
PLL Reference Leakage



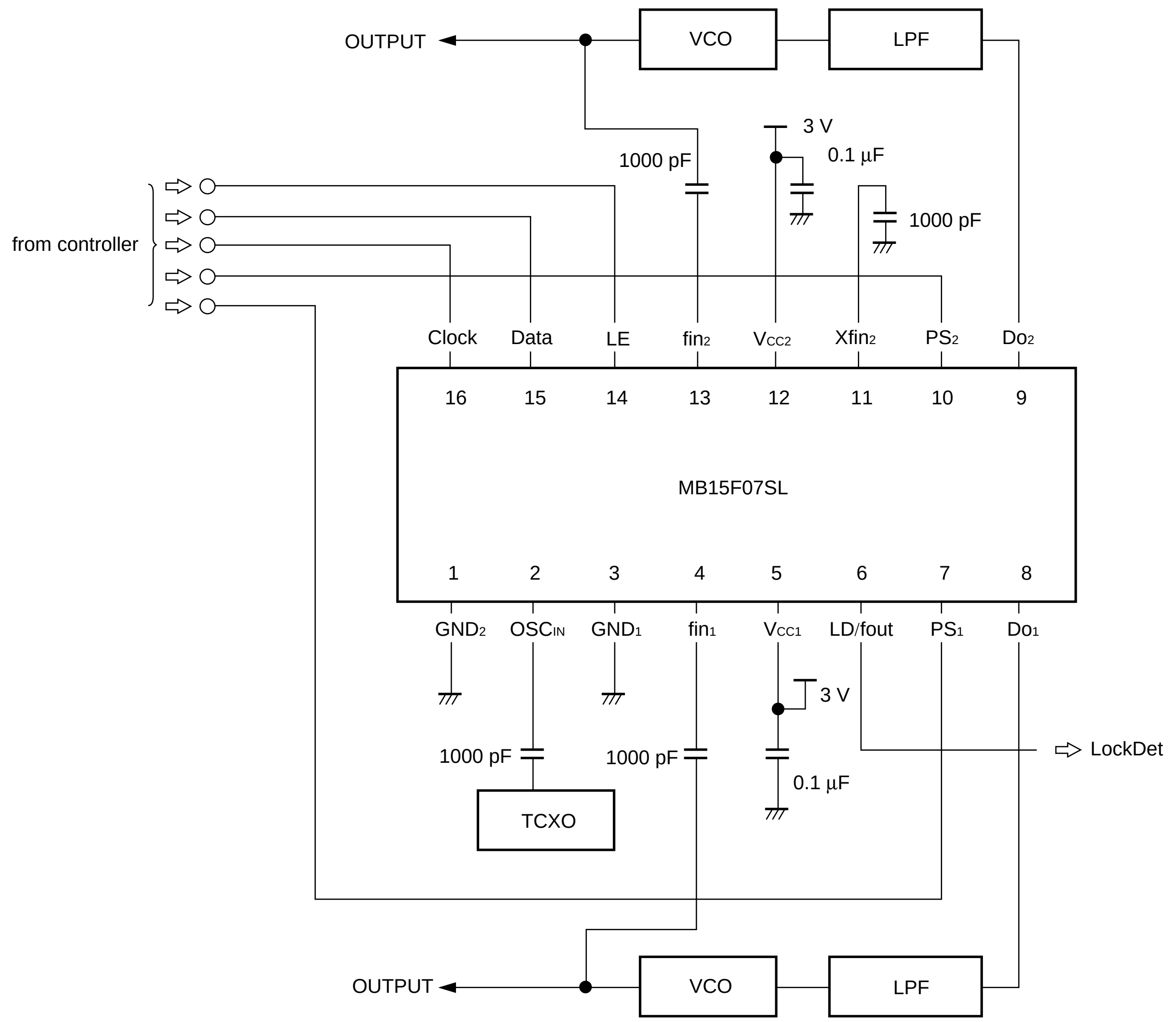
PLL Phase Noise



(Continued)


PLL Lock Up time
PLL Lock Up time
1005 MH→1031 MHz within ± 1 KHz
Lch→Hch
299 µs
1031 MH→1005 MHz within ± 1 KHz
Hch→Lch
330 µs
50.00000 MHz
10.00000 MHz/div
0 Hz
50.00000 MHz
10.00000 MHz/div
10.00000 MHz
0 S
2.0000000 ms
30.00500 MHz
2.000 kHz/div
29.99500 MHz
Meas # 91

■ APPLICATION EXAMPLE



Note: SSOP-16

■ USAGE PRECAUTIONS

(1) V_{CC2} must equal V_{CC1}.
Even if either PLL 2 or PLL 1 is not used, power must be supplied to both V_{CC2} and V_{CC1} to keep them equal.
It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

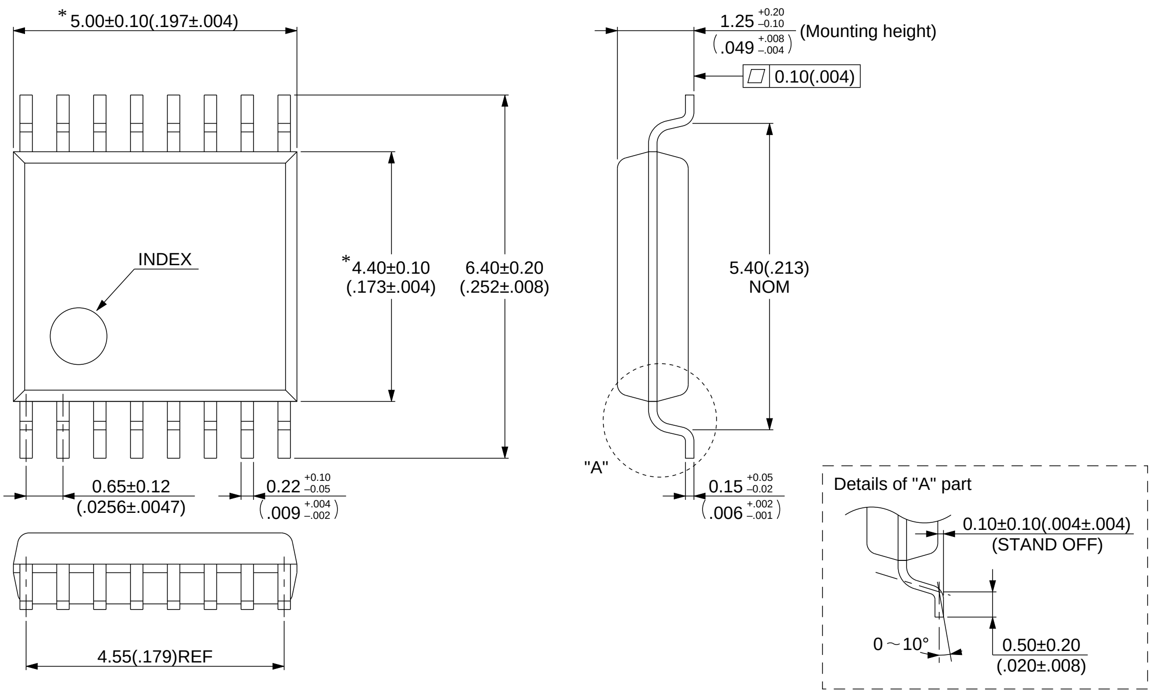
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F07SLPFV1	16-pin, plastic SSOP (FPT-16P-M05)	
MB15F07SLPV	16-pad, plastic BCC (LCC-16P-M03)	

■ PACKAGE DIMENSIONS

16-pin, Plastic SSOP
(FPT-16P-M05)

* : These dimensions do not include resin protrusion.



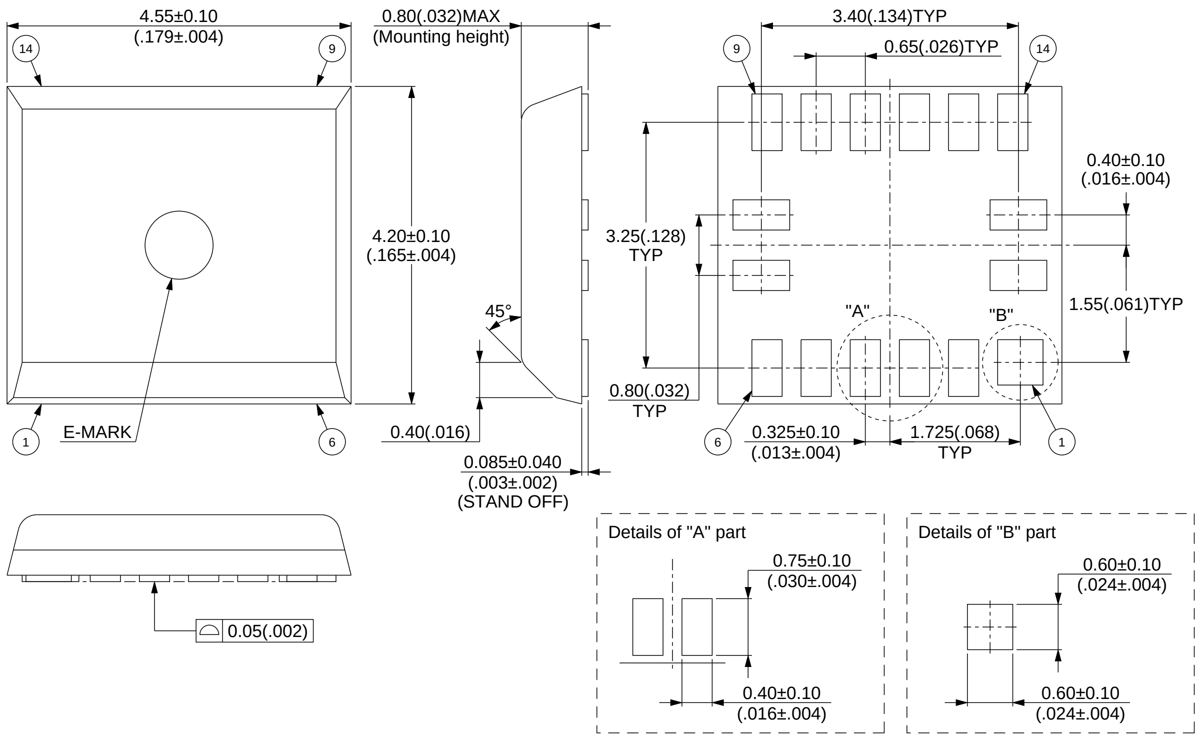
Dimensions in mm (inches)

(Continued)

(Continued)

16-pad, Plastic BCC
(LCC-16P-M03)

* : These dimensions do not include resin protrusion.



Dimensions in mm (inches)

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