

DATA SHEET

UMA1021M

Low-voltage frequency synthesizer
for radio telephones

Product specification
Supersedes data of 1996 May 06
File under Integrated Circuits, IC17

1996 August 28

Low-voltage frequency synthesizer for radio telephones

UMA1021M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable main divider
- 3-line serial interface bus
- Independent fully programmable reference divider, driven from external crystal oscillator
- Dual charge pump outputs
- Hard and soft power-down control.

APPLICATIONS

- 900 MHz and 2 GHz mobile telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1021M BICMOS device integrates a prescaler, programmable dividers, and a phase comparator to implement a phase-locked loop.

The device is designed to operate from 3 NiCd cells, in pocket phones, with low current and nominal 3 V supplies.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with a fully programmable reference divider. All divider ratios are supplied via a 3-wire serial programming bus.

Separate power and ground pins are provided to the analog (charge-pump) and digital circuits. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD1} and V_{DD2} must also be at the same potential (V_{DD}). V_{CC} must be equal to or greater than V_{DD} (e.g. $V_{DD} = 3\text{ V}$ and $V_{CC} = 5\text{ V}$ for wider VCO control voltage range).

The phase detector has two charge-pump outputs, CP and CPF, the latter of which is enabled directly at pin FAST. This permits the design of adaptive loops. The charge pump currents (phase detector gain) are fixed by an external resistance at pin ISET and via the serial interface. Only a passive loop filter is necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge-pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD} + I_{CC}$	supply current		–	10	–	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode		–	5	–	μA
f_{RF}	RF input frequency		300	–	2200	MHz
f_{xtal}	crystal reference input frequency		3	–	35	MHz
f_{PC}	phase comparator frequency		–	200	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	$^{\circ}\text{C}$

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1021M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

Low-voltage frequency synthesizer for radio telephones

UMA1021M

BLOCK DIAGRAM

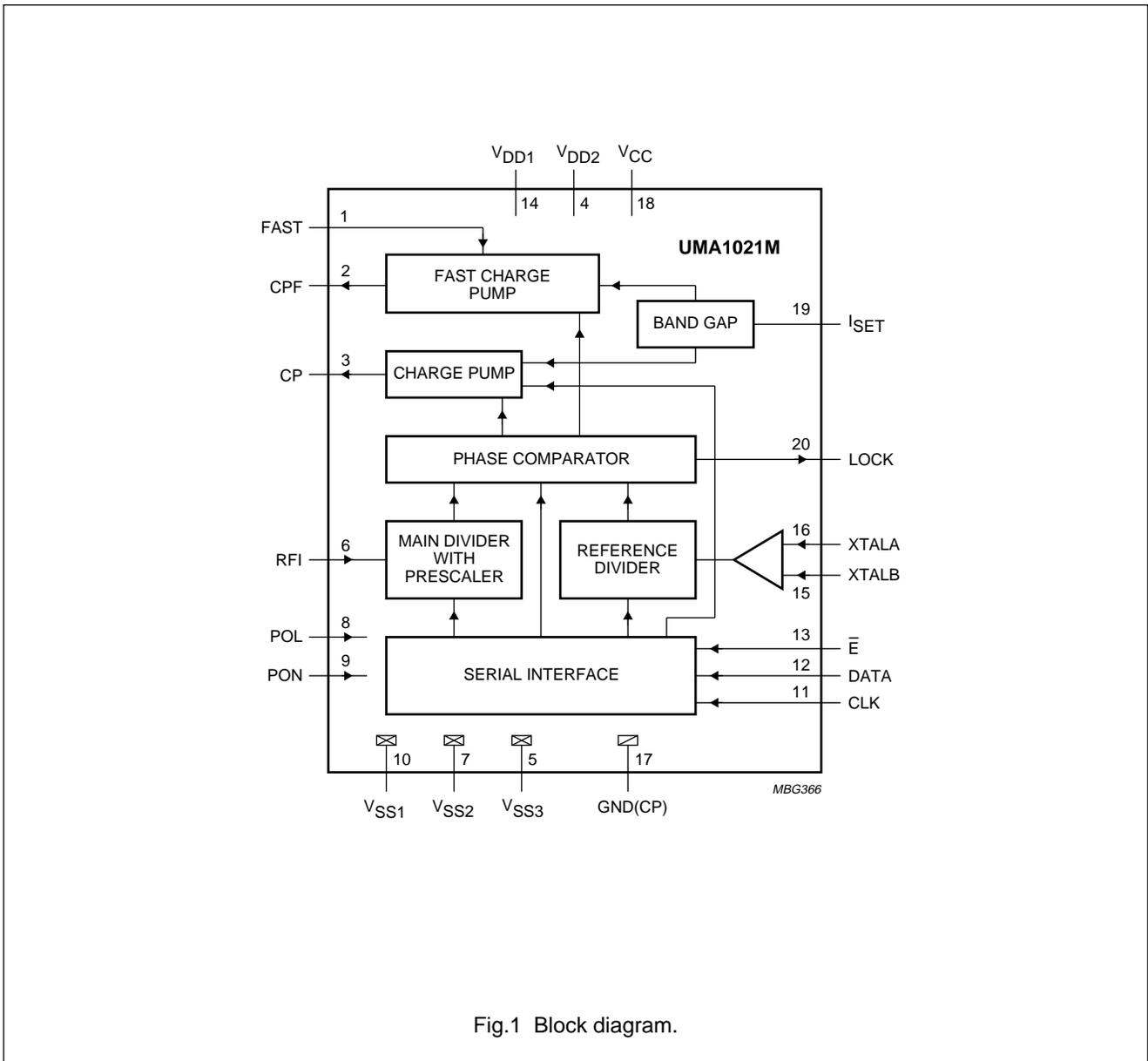


Fig.1 Block diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

PINNING

SYMBOL	PIN	DESCRIPTION
FAST	1	enable input for fast charge-pump output CPF
CPF	2	fast charge-pump output
CP	3	normal charge-pump output
V _{DD2}	4	power supply 2
V _{SS3}	5	ground 3
RFI	6	2 GHz main divider input
V _{SS2}	7	ground 2
POL	8	digital input to select polarity of power-on inputs (PON and sPON): POL = 0 for active LOW and POL = 1 for active HIGH
PON	9	power-on input
V _{SS1}	10	ground 1
CLK	11	programming bus clock input
DATA	12	programming bus data input
\bar{E}	13	programming bus enable input
V _{DD1}	14	power supply 1
XTALB	15	complementary crystal frequency input from TCXO; if not used should be decoupled to ground
XTALA	16	crystal frequency input from TCXO; if not used should be decoupled to ground
GND(CP)	17	ground for charge-pump
V _{CC}	18	supply for charge-pump
I _{SET}	19	external resistor from this pin to ground sets the charge-pump currents
LOCK	20	out-of-lock detector output

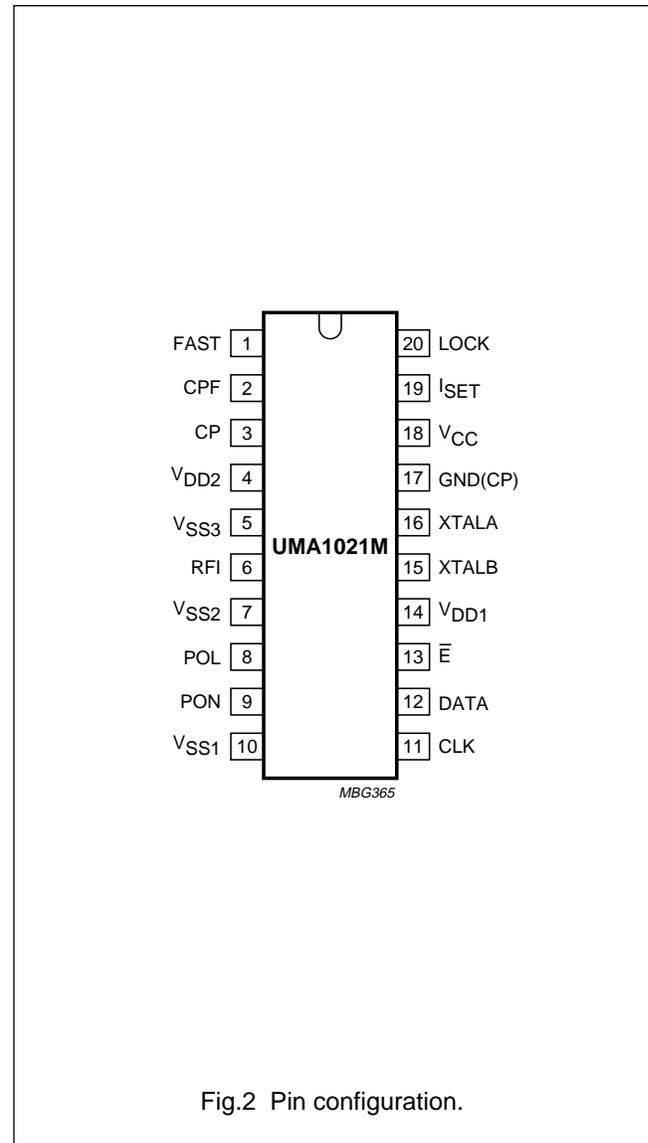


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main divider

The main divider is clocked at pin RFI by the RF signal which is AC-coupled from an external VCO. The divider operates with signal levels from 50 to 225 mV (RMS), and at frequencies from 300 MHz to 2.2 GHz. It consists of a fully programmable bipolar prescaler followed by a CMOS counter. Any divide ratios from 512 to 131071 inclusive can be programmed.

Reference divider

The reference divider is clocked by the differential signal between pins XTALA and XTALB. If only one of these inputs is used, the other should be decoupled to ground. The applied input signal(s) should be AC-coupled. The circuit operates with levels from 50 up to 500 mV (RMS) and at frequencies from 3 to 35 MHz. Any divide ratios from 8 to 2047 inclusive can be programmed.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

Phase detector

The phase detector is driven by the output edges of the main and reference dividers. It produces current pulses at pins CP and CPF whose amplitudes are programmed. The pulse duration is equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP and CPF sink current. If the reference divider edge arrives first, CP and CPF source current.

The currents at CP and CPF are programmed via the serial bus as multiples of a reference current set by an external resistor connected between pin I_{SET} and V_{SS} (see Table 3). CP remains active except in power-down. CPF is enabled via input pin FAST which is synchronized with respect to the phase detector to prevent output current pulses being interrupted. By appropriate connection to the loop filter, dual bandwidth loops can be designed; short time constant during frequency switching (FAST mode) to speed-up channel changes, and low bandwidth in the settled state to improve noise and breakthrough levels.

Additional circuitry is included to ensure that the gain of the phase detector remains linear even for small phase errors.

Out-of-lock detector

The out-of-lock detector is enabled (disabled) via the serial interface by setting bit OOL HIGH (LOW). An open drain transistor drives the output pin LOCK (pin 20). It is recommended that the pull-up resistor from this pin to V_{DD} is chosen to be of sufficient value to keep the sink current in the LOW state to below 400 μ A. When the out-of-lock detector is enabled, LOCK is HIGH if the error at the phase detector input is less than approximately 25 ns, otherwise LOCK is LOW. If the out-of-lock detector is disabled, LOCK remains HIGH.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable (\bar{E}). The data sent to the device is loaded in bursts framed by \bar{E} . Programming clock edges and their appropriate data bits are ignored until \bar{E} goes active LOW. The programmed information is loaded into the addressed latch when \bar{E} returns HIGH.

During normal operation, \bar{E} should be kept HIGH. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programmed data even during power-down.

When the synthesizer is powered-on, the presence of a TCXO signal at the reference divider input and a VCO signal at the main divider input is **required** for correct programming.

Data format

The leading bits (dt16 to dt0) make up the data field, while the trailing four bits (ad3 to ad0) are the address field. The UMA1021M uses 4 of the 16 available addresses. These are chosen for compatibility with other Philips Semiconductors radio telephone ICs. The data format is shown in Table 1. The first bit entered is dt16, the last bit is ad0. For the divider ratios, the first bits entered (PM16 and PR10) are the most significant (MSB).

The trailing address bits are decoded on the rising edge of \bar{E} . This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum \bar{E} pulse width after data transfer.

The test register (address 0000) does not normally need to be programmed. However if it is programmed, all bits in the data field should be set to logic 0.

Power-down mode

The synthesizer is on when both the input signals PON and the programmed bit sPON are active. The 'active' level for these two signals is chosen at pin POL (see Table 2). When turned on, the dividers and phase detector are synchronized to avoid random phase errors. When turned off, the phase detector is synchronized to avoid interrupting charge-pump pulses. For synchronisation functions to work correctly on power-up or power-down (using either hardware or software programming), the presence of TCXO and VCO signals is required to drive the appropriate divider inputs. The UMA1021M has a very low current consumption in the power-down mode.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

Table 1 Bit allocation; note 1

REGISTER BIT ALLOCATION													LAST IN												
DATA FIELD													ADDRESS												
dt16	dt15	dt14	dt13	dt12	dt11	dt10	dt9	dt8	dt7	dt6	dt5	dt4	dt3	dt2	dt1	dt0	ad3	ad2	ad1	ad0					
Test bits ⁽²⁾													0	0	0	0									
X	X	X	X	OOL ⁽³⁾	X	CR1	CR0	X	X	sPON ⁽³⁾	X	X	X	X	X	X	0	0	0	0					
main divider coefficient													PM0			0	1	0	0	1	0	0	0	0	
reference divider coefficient													PR0			0	1	1	0	0	0	1	0	0	1

Notes

1. X = don't care.
2. The test register (address 0000) should not be programmed with any other values except all zeros for normal operation.
3. Bit sPON = software power-up for synthesizer (see Table 2); OOL = Out-Of-Lock (1 = enabled).
4. PM16 is the MSB of the main divider coefficient; PR10 is the MSB of the reference divider coefficient.

Table 2 Power-on programming

POL	PON	sPON	SYNTHESIZER STATE	COMPATIBILITY
0	0	0	on	UMA1019M/UMA1019AM
0	1	X	off	UMA1019M/UMA1019AM
0	X	1	off	UMA1019M/UMA1019AM
1	0	X	off	UMA1017M
1	X	0	off	UMA1017M
1	1	1	on	UMA1017M

Table 3 Fast and normal charge pumps current ratio (note 1)

CR1	CR0	Icp	IcPF	IcPF : Icp
0	0	2 × I _{SET}	8 × I _{SET}	4 : 1
0	1	2 × I _{SET}	16 × I _{SET}	8 : 1
1	0	1 × I _{SET}	12 × I _{SET}	12 : 1
1	1	1 × I _{SET}	16 × I _{SET}	16 : 1

Note

1. $I_{SET} = \frac{V_{SET}}{R_{SET}}$; reference current for charge pumps.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	digital supply voltage	-0.3	+5.5	V
V_{CC}	charge-pump supply voltage	-0.3	+5.5	V
$V_{CC} - V_{DD}$	difference in voltage between V_{CC} and V_{DD}	-0.3	+5.5	V
V_n	voltage at pins 6, 8, 9 and 11 to 13	-0.3	$V_{DD} + 0.3$	V
	voltage at pins 1, 2, 3, 15, 16, 19 and 20	-0.3	$V_{CC} + 0.3$	V
ΔV_{GND}	difference in voltage between any of GND(CP), V_{SS1} , V_{SS2} , and V_{SS3} (these pins should be connected together)	-0.3	+0.3	V
P_{tot}	total power dissipation	-	150	mW
T_{stg}	storage temperature	-55	+125	°C
T_{amb}	operating ambient temperature	-30	+85	°C
$T_{j(max)}$	maximum junction temperature	-	150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices. This device meets class 2 ESD test requirements [Human Body Model (HBM)], in accordance with "MIL STD 883C - method 3015".

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	120	K/W

Low-voltage frequency synthesizer for radio telephones

UMA1021M

CHARACTERISTICS

All values refer to the typical measurement circuit of Fig.5; $V_{DD1} = V_{DD2} = 2.7$ to 5.5 V; $V_{CC} = 2.7$ to 5.5 V; $T_{amb} = 25$ °C; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; pins 4, 14 and 18						
V_{DD}	digital supply voltage	$V_{DD1} = V_{DD2}$; $V_{CC} \geq V_{DD}$	2.7	–	5.5	V
V_{CC}	charge pump supply voltage	$V_{CC} \geq V_{DD}$	2.7	–	5.5	V
$I_{DD1} + I_{DD2}$	synthesizer digital supply current	$V_{DD} = 5.5$ V	–	7	9.5	mA
I_{CC}	charge pump supply current	$V_{CC} = 5.5$ V; $R_{SET} = 5.6$ k Ω	–	3	3.8	mA
$I_{CC(pd)} + I_{DD(pd)}$	total supply current in power-down mode	logic levels 0 V or V_{DD}	–	5	50	μ A
RF main divider input; pin 6						
f_{RF}	RF input frequency		300	–	2200	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	$R_s = 50$ Ω	50	–	225	mV
R_m	main divider ratio		512	–	131071	
Z_i	input impedance (real part)	$f_{RF} = 1$ GHz	–	1	–	k Ω
		$f_{RF} = 2$ GHz	–	60	–	Ω
C_i	typical pin input capacitance	$f_{RF} = 1$ GHz	–	1	–	pF
		$f_{RF} = 2$ GHz	–	1	–	pF
Synthesizer reference divider input; pins 15 and 16						
f_{xtal}	crystal reference input frequency		3	–	35	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 15 and 16 (RMS value)		50	–	500	mV
R_{ref}	reference division ratio		8		2047	
Z_i	input impedance (real part)	$f_{xtal} = 13$ MHz	–	10	–	k Ω
C_i	typical pin input capacitance	$f_{xtal} = 13$ MHz	–	1.5	–	pF
Phase detector						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump current setting resistor input; pin 19						
R_{SET}	external resistor connected between pin 19 and ground		5.6	–	12	k Ω
V_{SET}	regulated voltage at pin 19	$R_{SET} = 5.6$ k Ω	–	1.2	–	V

Low-voltage frequency synthesizer for radio telephones

UMA1021M

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Charge pump outputs; pins 2 and 3; $R_{SET} = 5.6 \text{ k}\Omega$						
$I_{ocp(Err)}$	charge pump output current error		-25	-	+25	%
I_{match}	sink-to-source current matching		-	± 5	-	%
I_{Llcp}	charge pump off leakage current	$V_{CP/CPF} = \frac{1}{2}V_{CC}$	-5	± 1	+5	nA
$V_{CP/CPF}$	charge pump voltage compliance		0.4	-	$V_{CC} - 0.4$	V
Phase noise						
N_{900}	synthesizer's contribution to close-in phase noise of 900 MHz RF signal at 1 kHz offset (GSM)	$f_{xtal} = 13 \text{ MHz};$ $V_{xtal} = 0 \text{ dBm};$ $f_{PC} = 200 \text{ kHz}$	-	-88	-	dBc/Hz
N_{1800}	synthesizer's contribution to close-in phase noise of 1.8 GHz RF signal at 1 kHz offset (DCS1800)	$f_{xtal} = 13 \text{ MHz};$ $V_{xtal} = 0 \text{ dBm};$ $f_{PC} = 200 \text{ kHz}$	-	-82	-	dBc/Hz
Interface logic input signal levels; pins 1, 8, 9, 11, 12 and 13						
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	-	$V_{DD} + 0.3$	V
V_{IL}	LOW level input voltage		-0.3	-	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	-5	-	+5	μA
C_i	input capacitance		-	2	-	pF
Lock detect output signal; pin 20; open-drain output						
V_{OL}	LOW level output voltage	$I_{sink} < 0.4 \text{ mA}$	-	-	0.4	V
t_{OOL}	phase error threshold for out-of-lock detector		-	25	-	ns

Low-voltage frequency synthesizer for radio telephones

UMA1021M

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{CC} = 3\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; \bar{E}					
t_{START}	delay to rising clock edge	40	–	–	ns
t_{END}	delay from last falling clock edge	–20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	4000 ⁽¹⁾	–	–	ns
$t_{SU;\bar{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 4 μs provided all the following conditions are fulfilled:

- a) Main divider input frequency $f_{RF} > \frac{447}{t_{W(min)}}$.
- b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$.

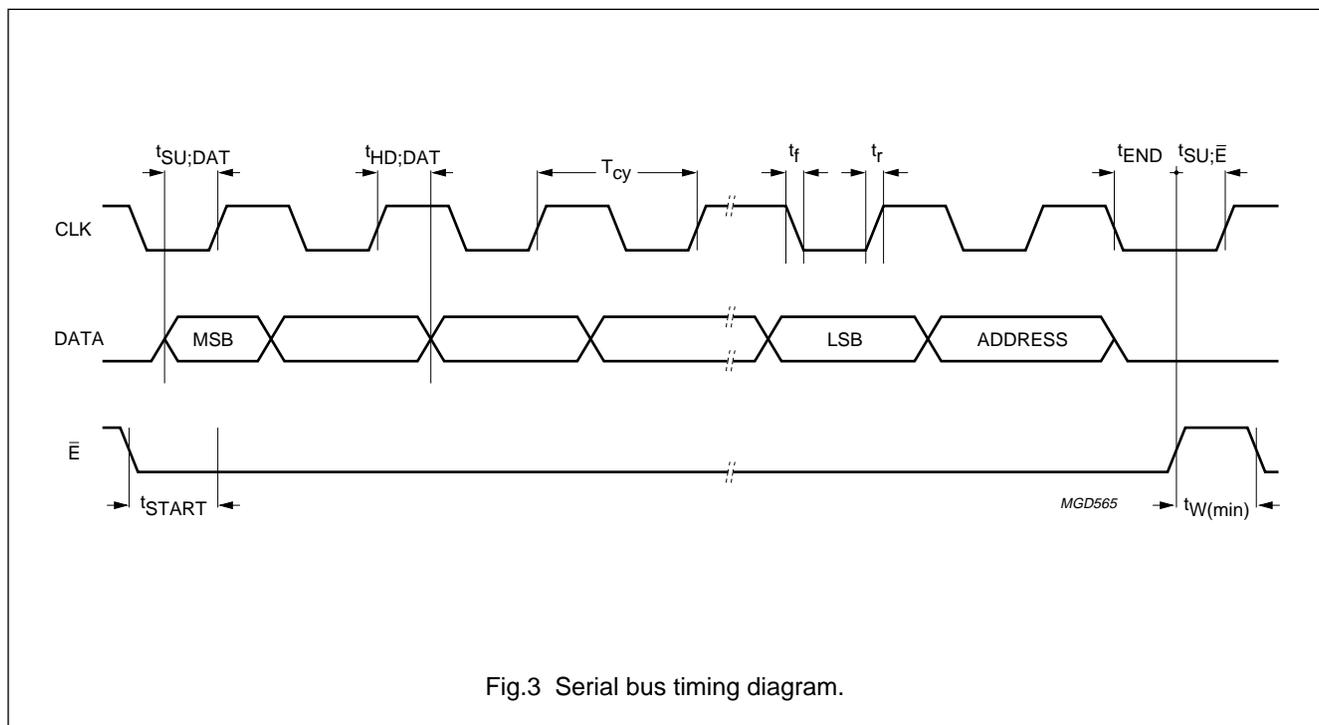


Fig.3 Serial bus timing diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

APPLICATION INFORMATION

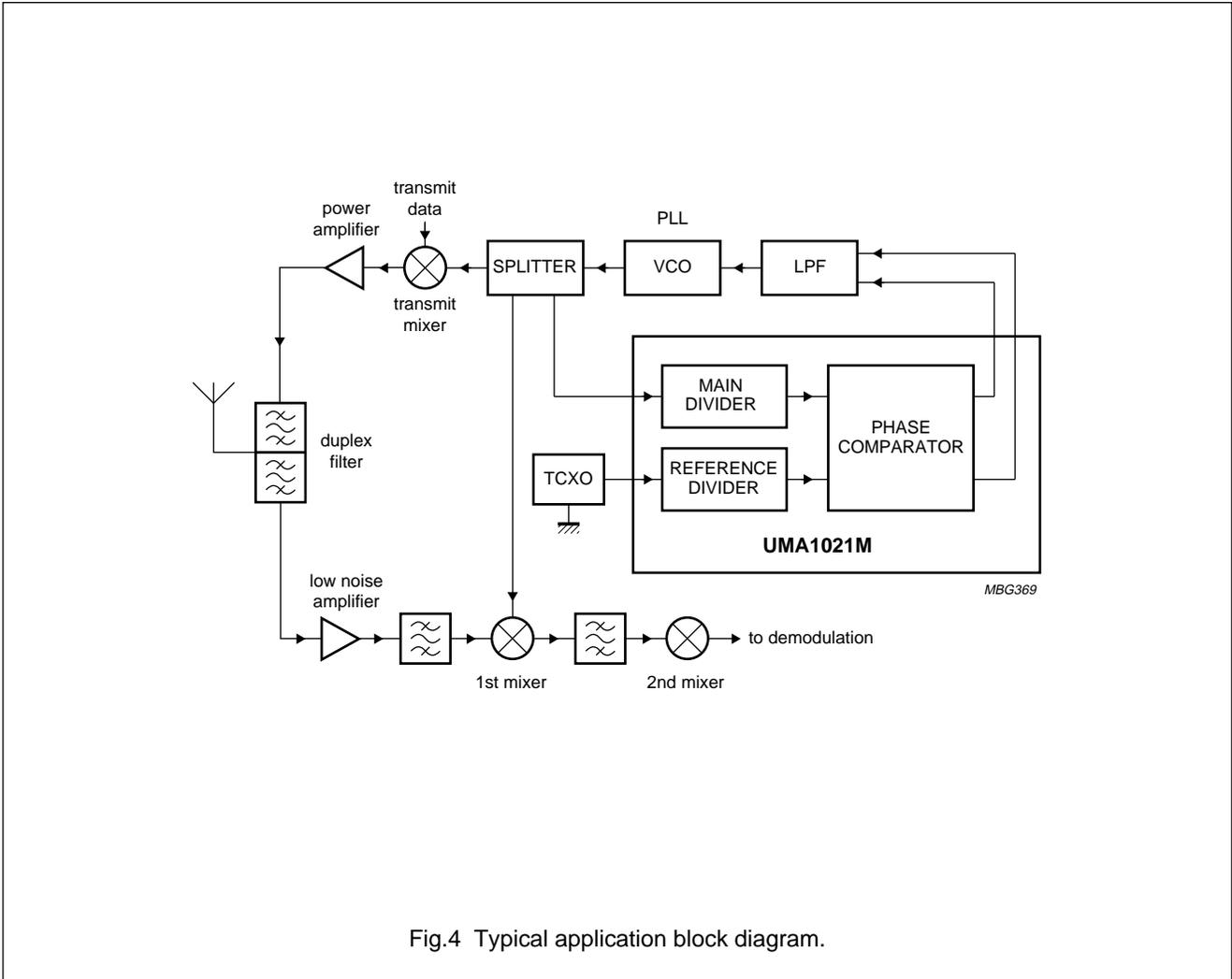
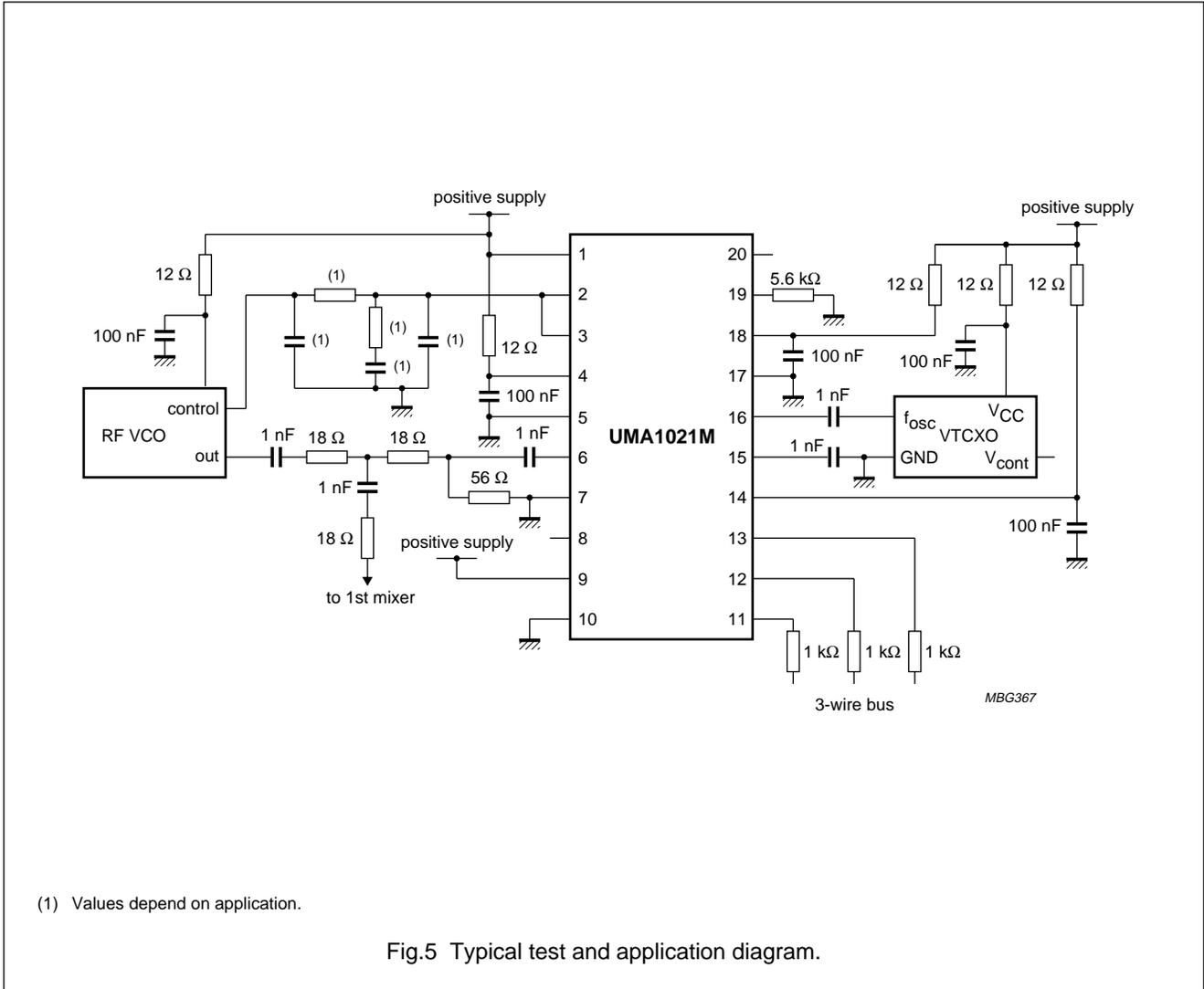


Fig.4 Typical application block diagram.

Low-voltage frequency synthesizer for radio telephones

UMA1021M



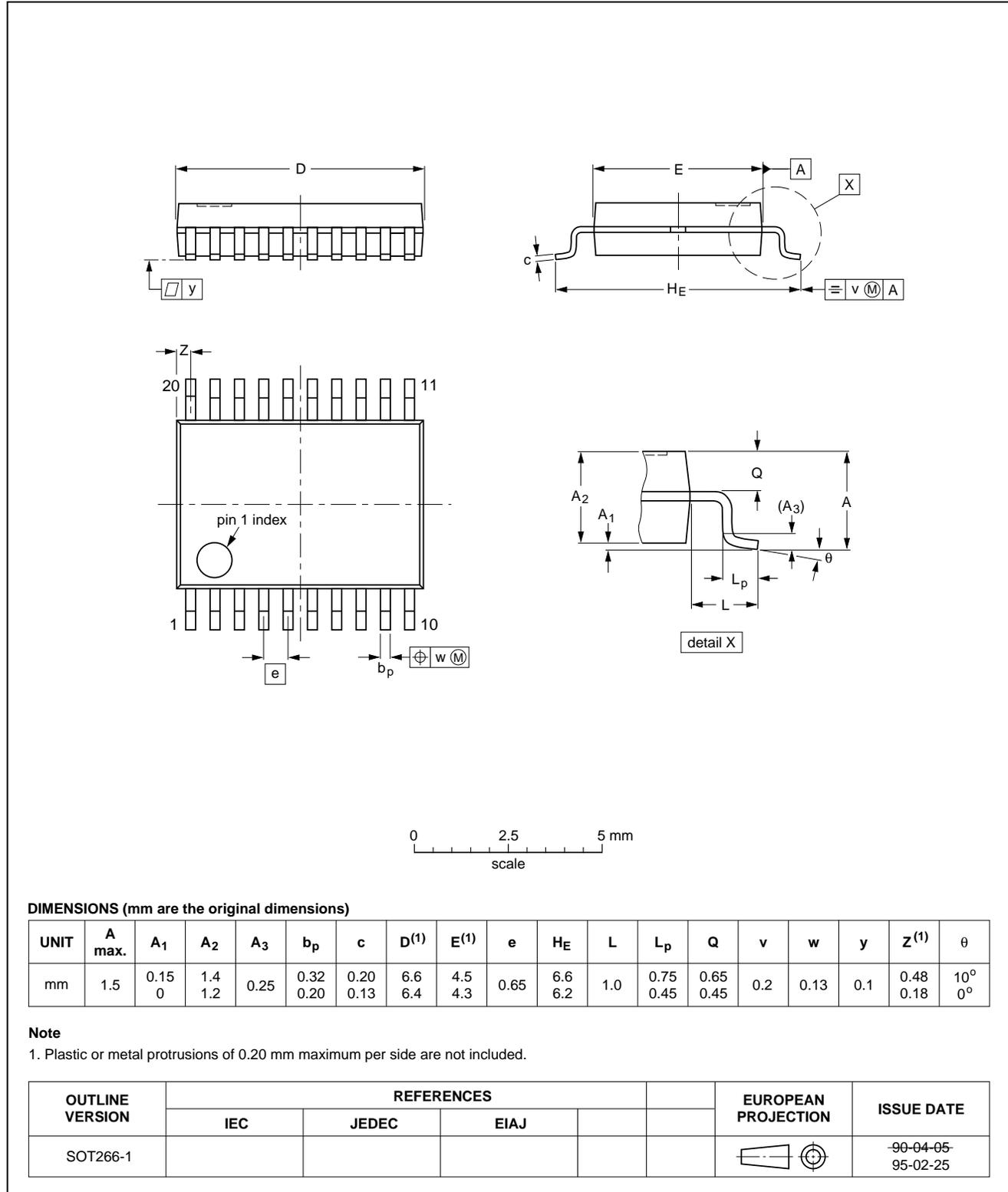
Low-voltage frequency synthesizer for radio telephones

UMA1021M

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm

SOT266-1



Low-voltage frequency synthesizer for radio telephones

UMA1021M

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for SSOP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

Even with these conditions, only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Low-voltage frequency synthesizer for radio telephones

UMA1021M

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 615 800, Fax. +358 615 80920

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS,
Tel. +30 1 4894 339/911, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 926 5361, Fax. +7 095 564 8323

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 825 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 1996

SCA51

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

647021/1200/03/pp16

Date of release: 1996 August 28

Document order number: 9397 750 01062

Let's make things better.

**Philips
Semiconductors**



PHILIPS