Logic Families/Objectives

- Digital Logic Voltage and Current Parameters
  - Fan-out, Noise Margin, Propagation Delay
- TTL Logic Family
- Supply current spikes and ground bounce
- TTL Logic Family Evolution
- ECL
- CMOS Logic Families and Evolution
- Logic Family Overview

Logic Families/Level of Integration

- SSI   <12 gates/chip
- MSI   12..99 gates/chip
- LSI   ..1000 gates/chip
- VLSI   …10k gates/chip
- ULSI   …100k gates/chip
- GSI   …1Meg gates/chip

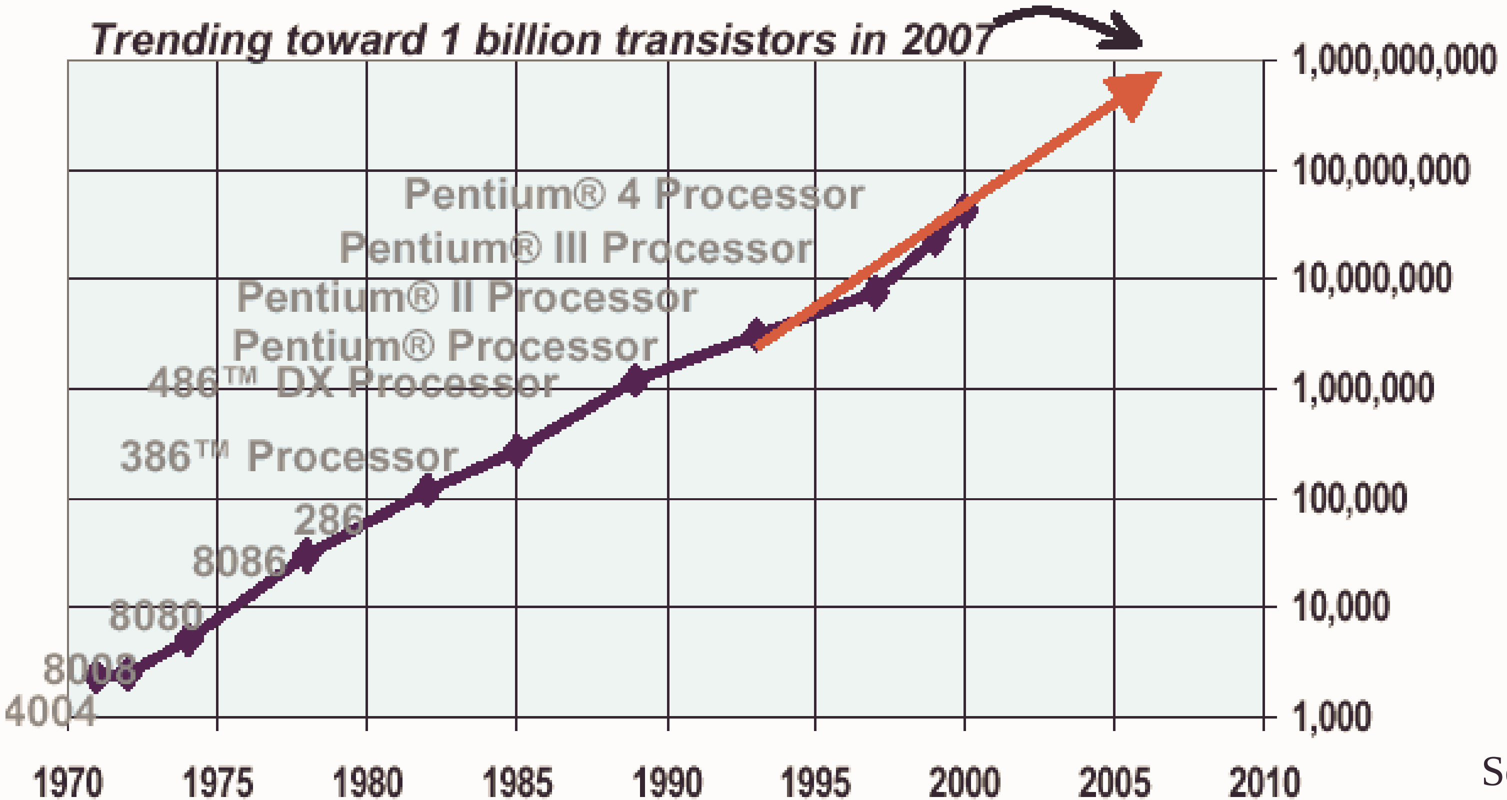
Note: Ratio gate count/transistor count is roughly 1/10

Level of integration ever increasing, because of
•cost
•speed
•size
•power
•reliability

Limits of integration:
•packaging
•power dissipation
•inductive and capacitive components
•flexibility
•critical quantity

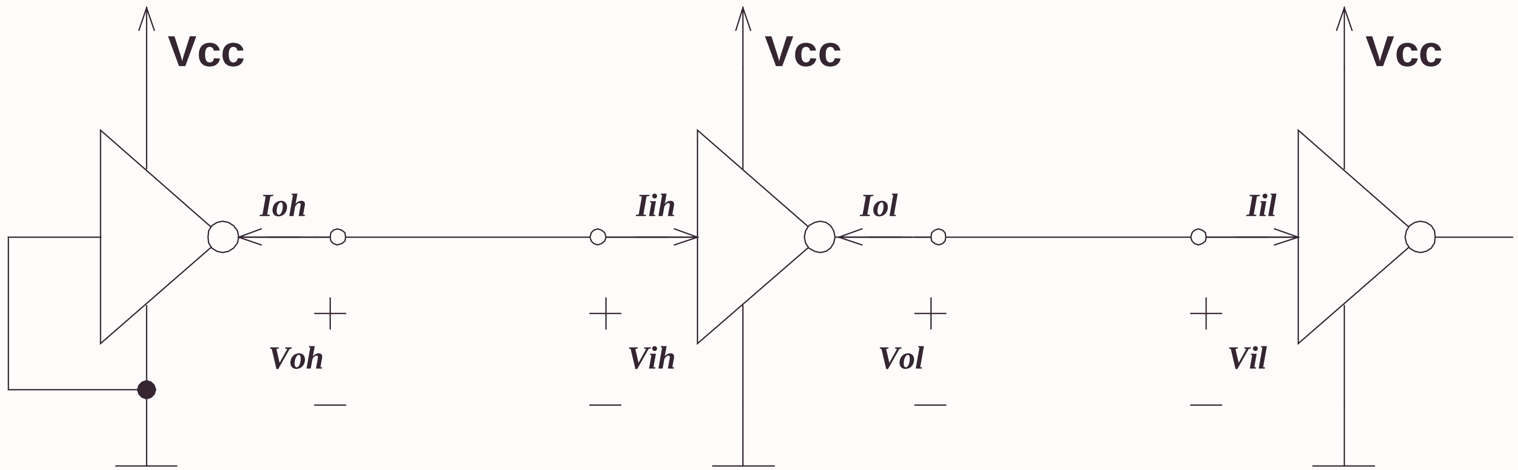
Logic Families/Level of Integration

– Remember: Gordon Moore, 1975. Predictions:
  - Mosfet device dimensions scale down by a factor of 2 every 3 years
  - #transistors/chip double every 1-2 years.



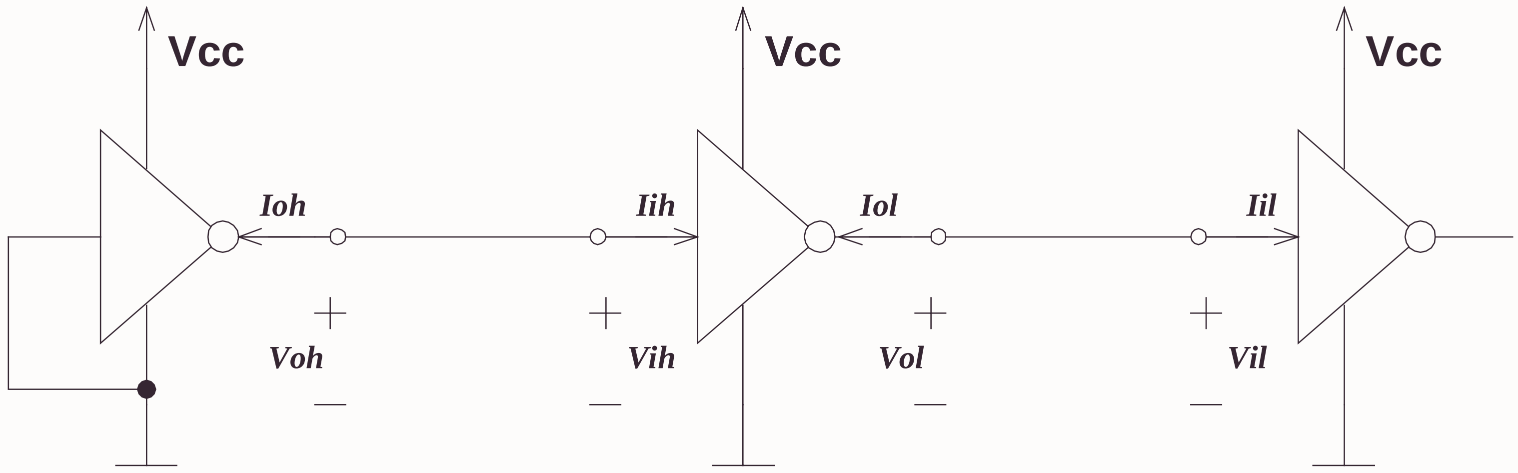
Source: G. Sery, Intel

Logic Families/Static VI Parameters



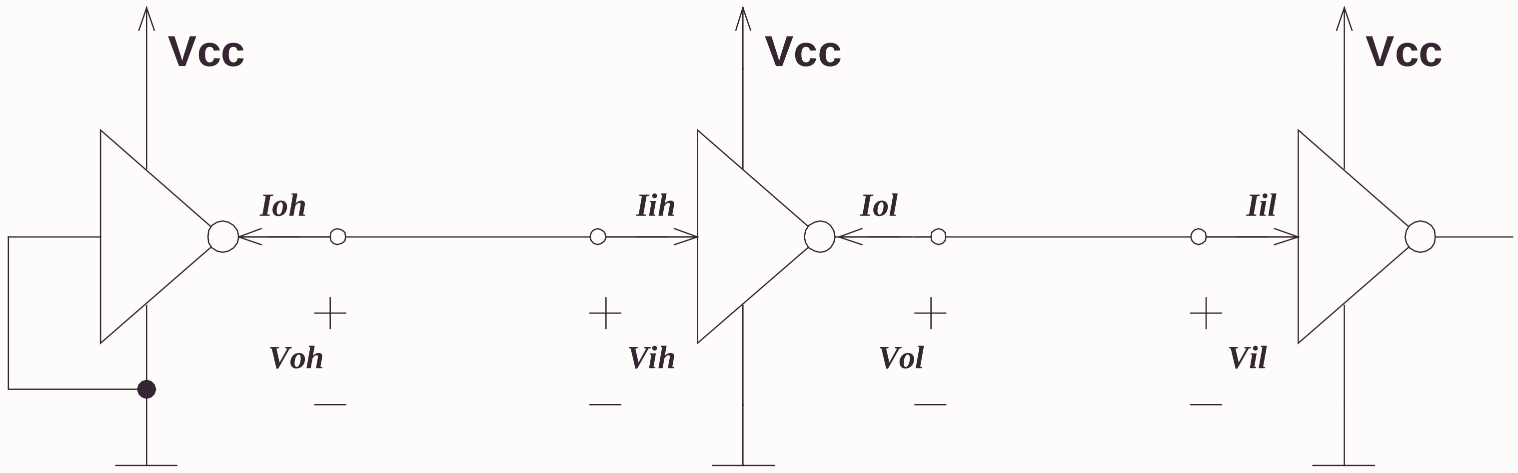
Parameter	Comment
Voh(min)	**High-Level Output Voltage**. The minimum voltage level at a logic circuit output in the logical 1 state under defined load conditions.
Vol(max)	**Low-Level Output Voltage**. The maximum voltage level at a logic circuit output in the logical 0 state under defined load conditions.

Logic Families/Static VI Parameters



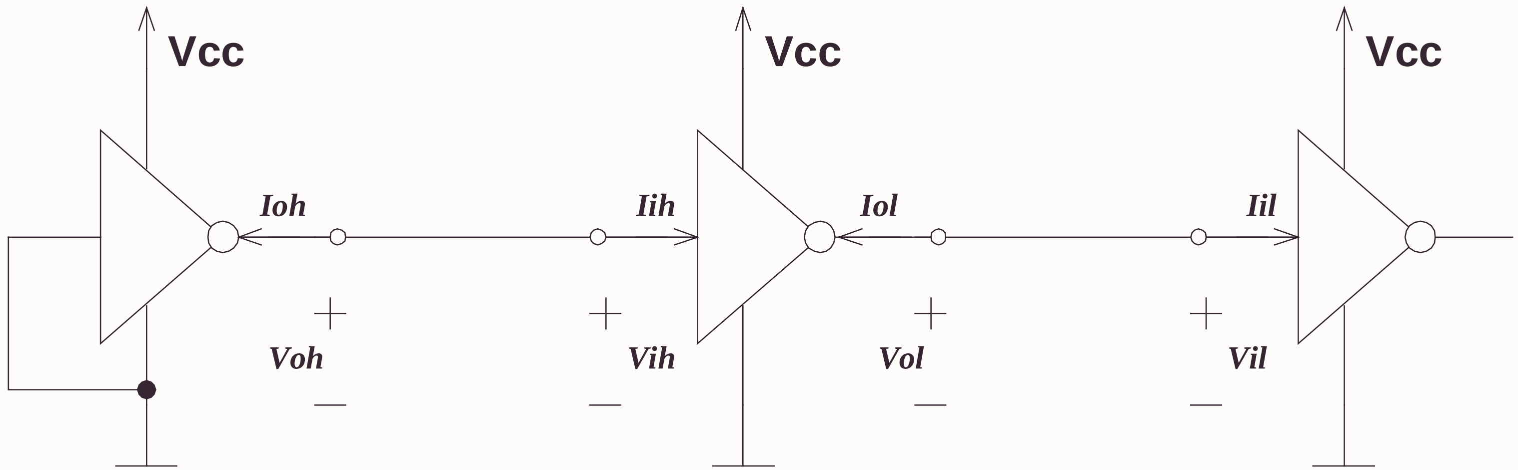
Parameter	Comment
Vih(min)	**High-Level Input Voltage**. The minimum voltage level required for a logical 1 at an input. Any voltage below this level may not be recognized as a logical 1 by the logic circuit.
Vil(max)	**Low-Level Input Voltage**. The maximum voltage level required for a logical 0 at an input. Any voltage above this level may not be recognized as a logical 0 by the logic circuit.

Logic Families/Static VI Parameters



Parameter	Comment
Ioh	**High-Level Output Current**. Current flowing into an output in the logical 1 state under specified load conditions.
Iol	**Low-Level Output Current**. Current flowing into an output in the logical 0 state under specified load conditions.

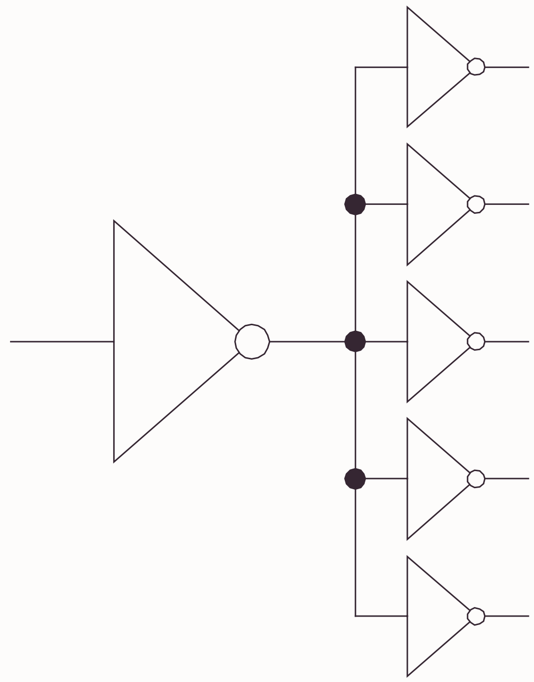
Logic Families/Static VI Parameters



Parameter	Comment
Iih	**High-Level Input Current**. Current flowing into an input when a specified high-level voltage is applied to that input.
Iil	**Low-Level Input Current**. Current flowing into an input when a specified low-level voltage is applied to that input.

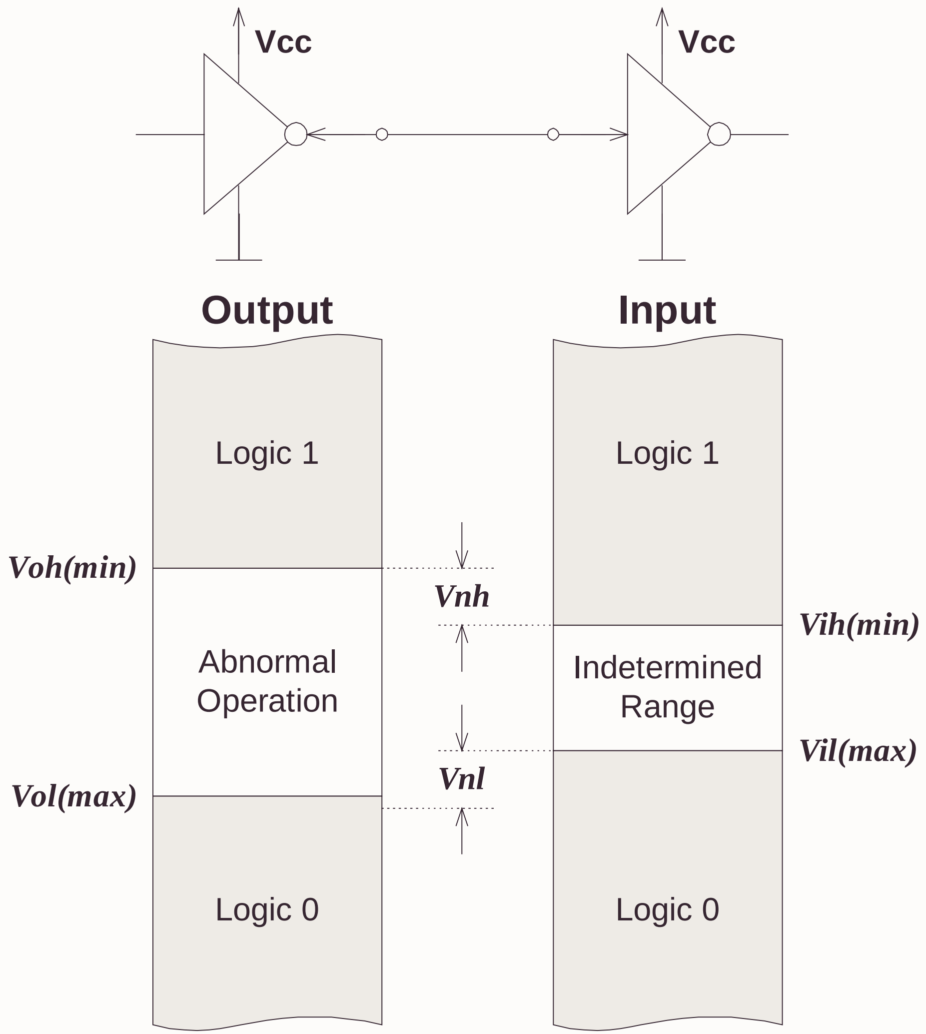
Logic Families/Fan-Out

– Fan-out: The maximum number of logic inputs that an output can drive reliably.



Beware:
Modern mixed-technology digital systems often employ logic from different logic families. In this case Fan-out is meaningless, unless the operating condition is specified exactly.
Unless otherwise specified, fan-out is always assumed to refer to ***load devices of the same family*** as the driving output.

Logic Families/Noise (Voltage) Margin



High state noise margin :

$$Vnh = Voh(min) - Vih(min)$$

Low state noise margin :

$$Vnl = Vil(max) - Vol(max)$$

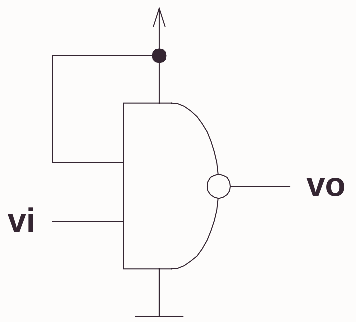
Noise margin :

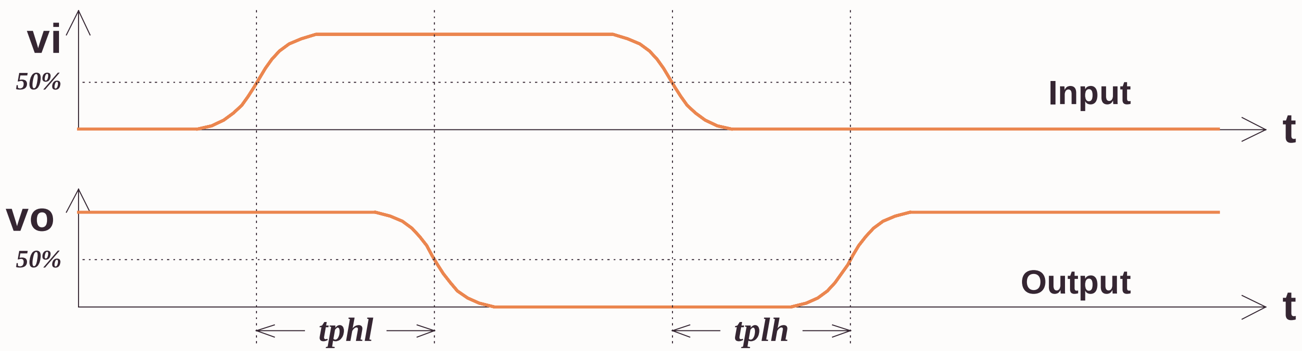
$$Vn = min(Vnh, Vnl)$$

Noise margin required for reliable operation of digital systems in the presence of noise, crosscoupling, and ground-bounce.

Sometimes quoted: Percentage noise margin… bears little practical value.

Logic Families/Propagation Delay





Parameter	Comment
tphl	**Input-to-output propagation delay time** for output going from high to low.
tplh	**Input-to-output propagation delay time** for output going from low to high.

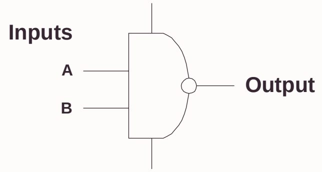
(Vague) comparison between logic families:

(e.g. for 74HC00: 25ns*100µW=2.5pJ)

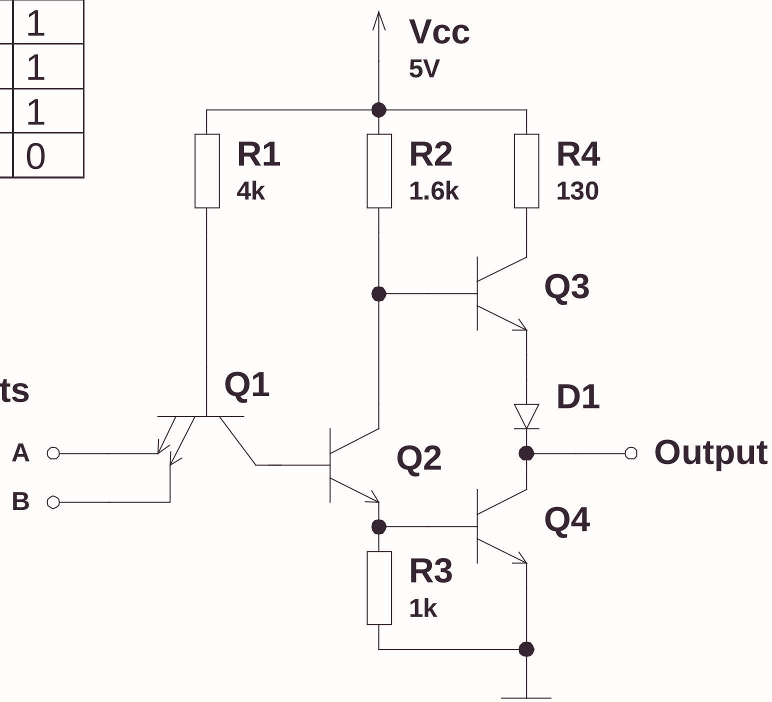
Gate Speed Power Product :

$$tp_{avg} \cdot Pdiss_{avg}$$

Logic Families/TTL Logic



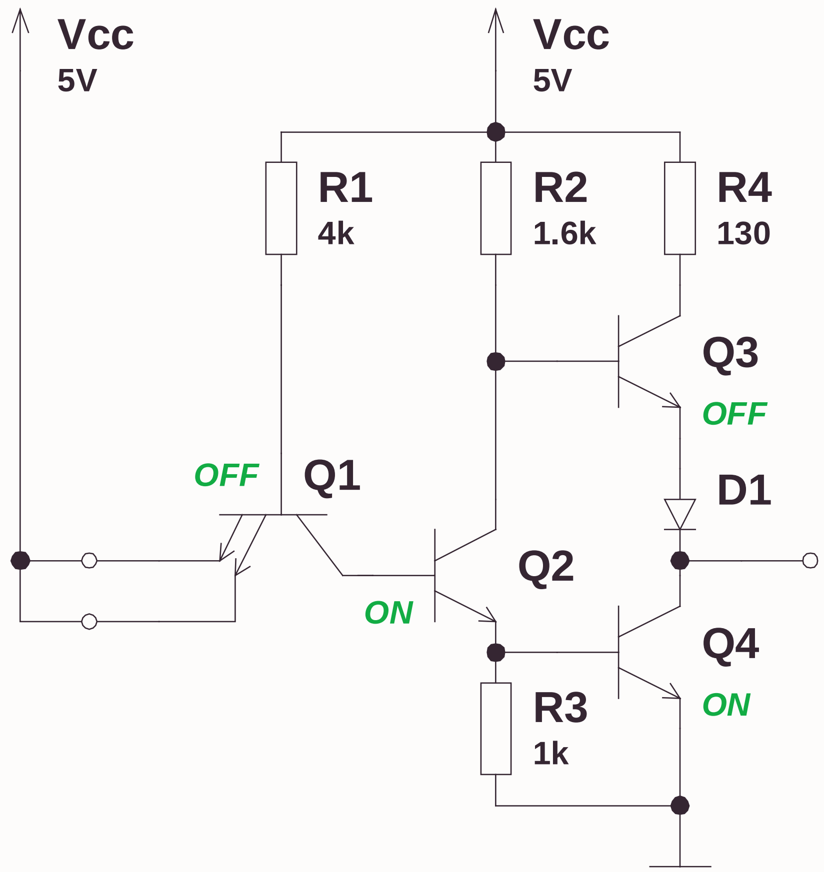
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Standard TTL Logic:

•Bipolar Transistor-Transistor Logic
•Introduced in 1964 (Texas Instruments)
•Tremendous influence on the characteristics of all logic devices today
•Standard TTL shaped digital technology
•Standard TTL Logic (e.g. 7400) practically obsolete (i.e. replaced by more advanced logic families, e.g. 74ALS00)
•A large variety of logic functions available
•Single- or multi-emitter input transistor Q1 (up to eight emitters)
•Totem-pole output arrangement (Q3, Q4)

Logic Families/TTL Logic/Static Analysis



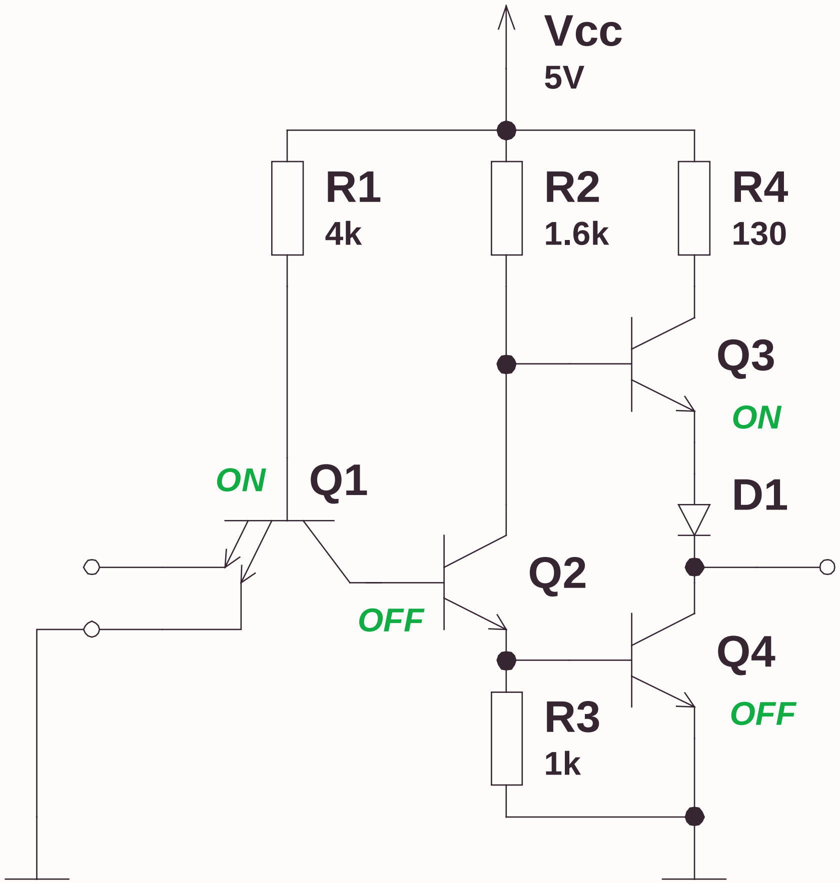
Low State Analysis:

- Inputs high (connected to Vcc)
- Q1: Inverse-active mode
- Input currents very low (base current of Q2)
- Q2 conducting (saturated)
- Q4 conducting
- Q3 and D1 off (approx 0.8V at B of Q3)
- Power dissipation in R1, Q1, R2, Q2, R3, Q4
- On-state resistance of Q4 is roughly 1..25Ω
- Non-ideal pull-down: Vcesat (Q4)
- Load will supply output low state current

Q4 is referred to as current-sinking transistor or pull-down transistor

Inputs interpreted as "high" when unconnected (floating).
DON'T LEAVE INPUTS UNCONNECTED !
Floating inputs are susceptible to noise…

Logic Families/TTL Logic/Static Analysis

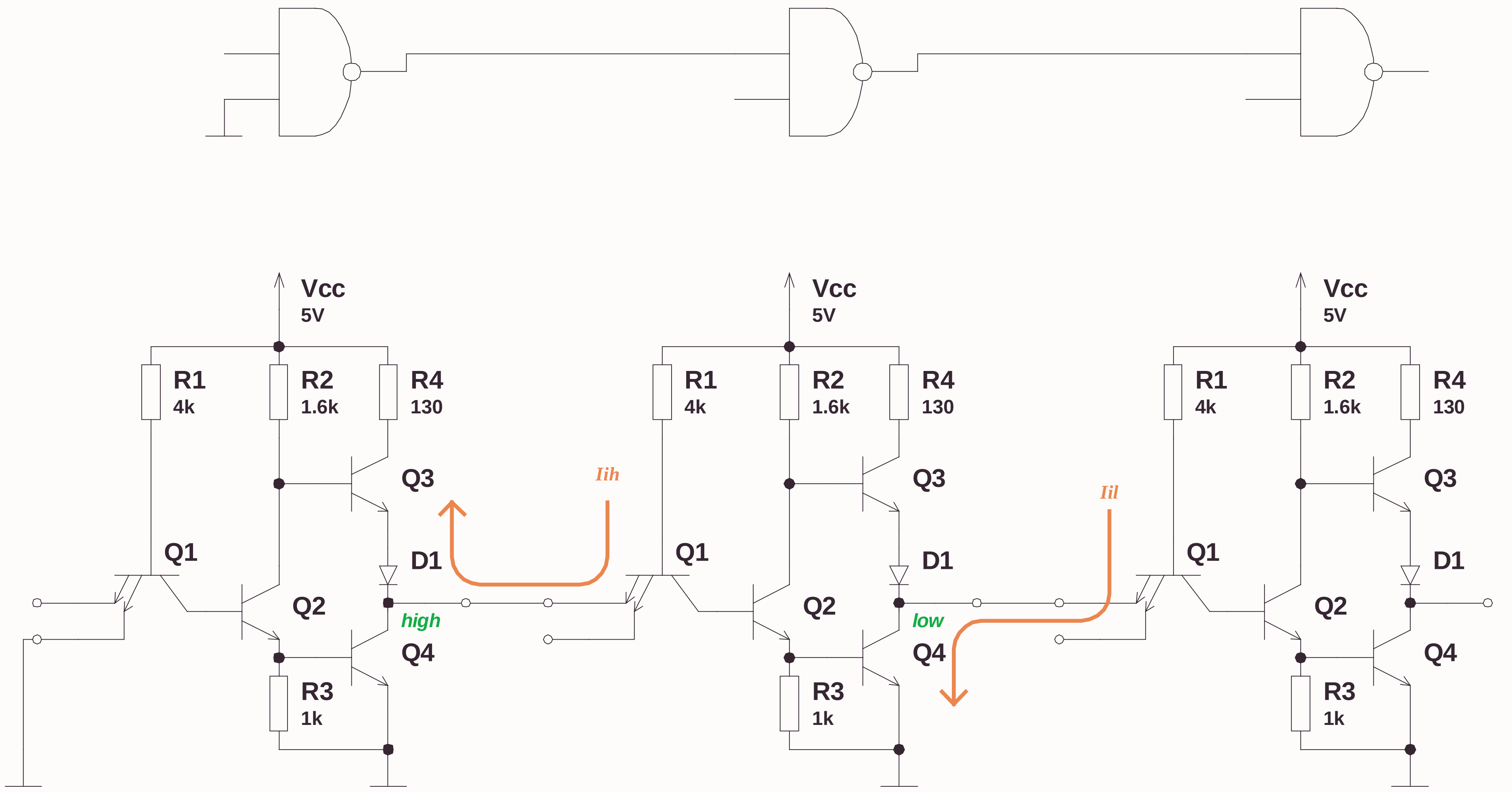


High State Analysis:

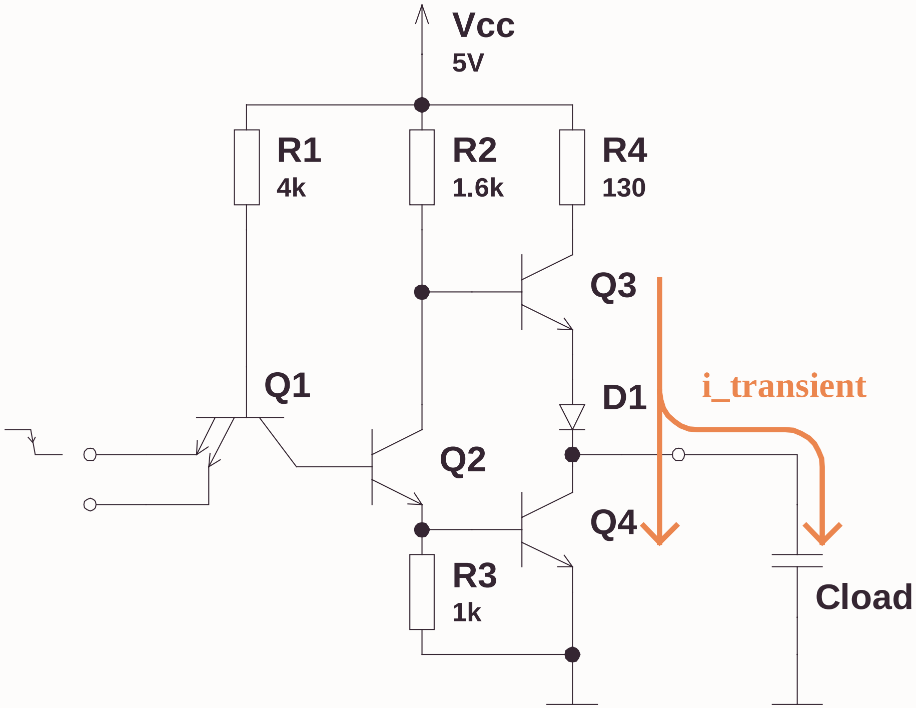
- One or both inputs low (connected to GND)
- Substantial input current (emitter current Q1) controlled by R1
- Q1 on (saturated)
- Q2 off
- Q4 off
- Q3 and D1 on
- Q3 acts as an "active pull-up"
- Non-ideal pull-up: Vbe (Q3) and Vfw (D1)
- Output high current through R4, Q3, D1
- Power dissipation in R1, Q1, R2, R4, Q3, D1
- Vcc will supply output high state current

Q3 is referred to as current-sourcing transistor or pull-up transistor

Logic Families/TTL Logic/Cascading TTL

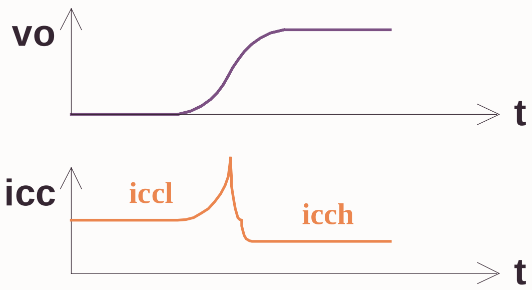


Logic Families/Supply Current Spikes



Output Low-to-High Transient:

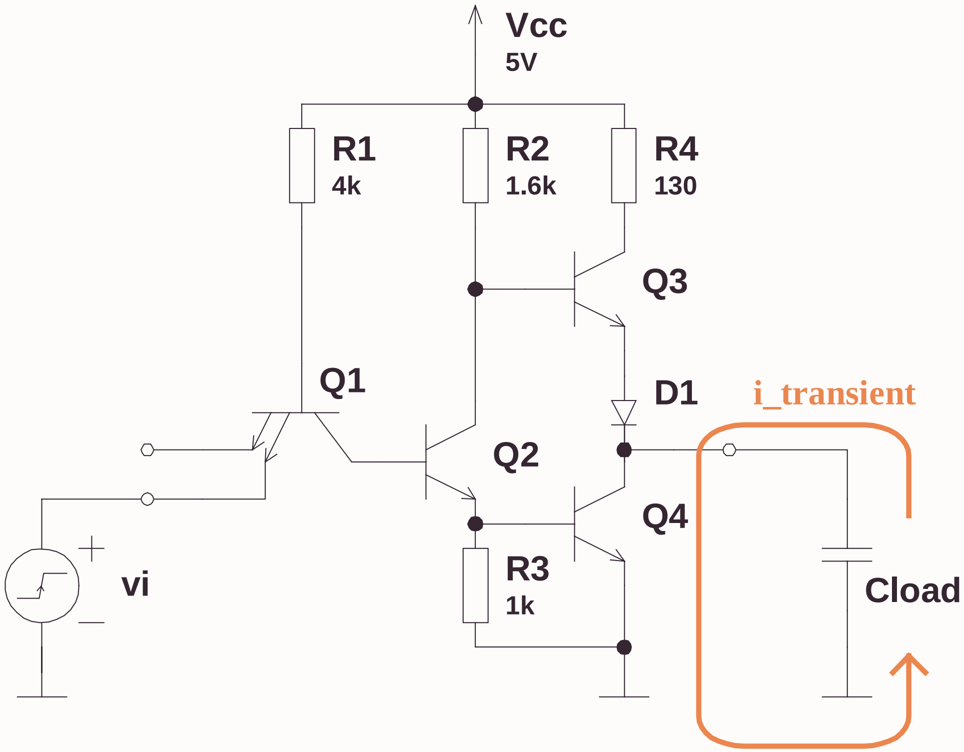
- Initially: Q3 off, Q4 on (saturated)
- Q4 turned off, Q3 turned on
- Change of state of Q4 takes longer than Q3
- During a short interval both Q3 and Q4 are conducting (cross-conduction, “shot-through”).
- Supply sees a relatively large current surge.
- Additional current surge due to load capacitance (e.g. input capacitance of following gate)



Whenever a totem-pole TTL output goes from LOW to HIGH, a current spike is drawn from the supply. Essential: POWER SUPPLY DECOUPLING!

Current spikes can cause noise problems (inductive cross-coupling). Identify loops and minimise loop areas!

Logic Families/Ground Bounce



Output High-to-Low Transient:

•Initially: Q3 on, Q4 off

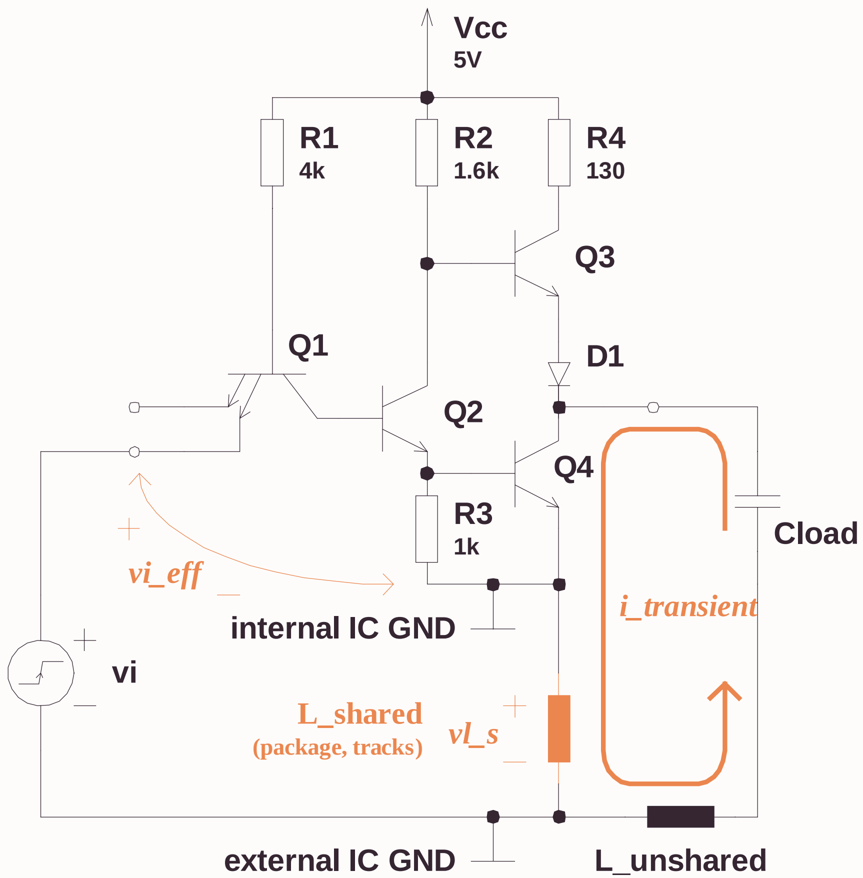
•Negligible Q3/Q4 cross-conduction

•Fast discharge of load capacitance through Q4

•Discharge current spike through IC ground pin.

Current spikes can cause noise problems (inductive cross-coupling). Identify loops and minimise loop areas!

Logic Families/Ground Bounce



Discharge current path

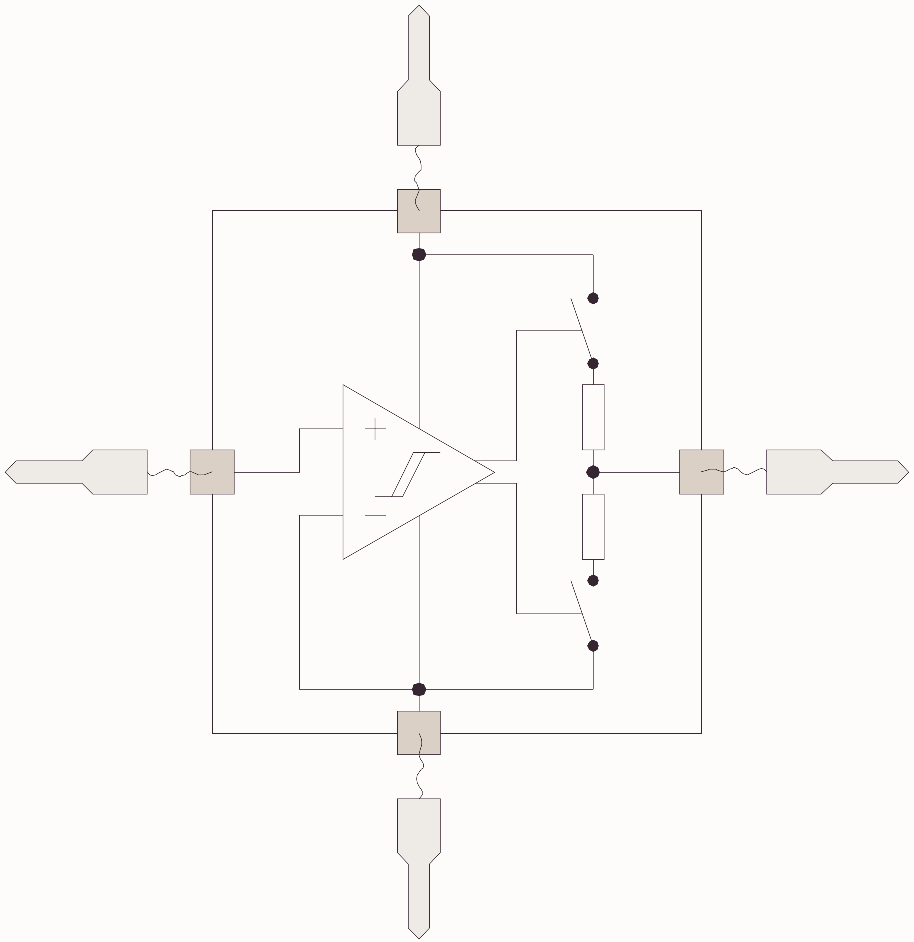
- positive electrode of load capacitance
- Q4
- bond wire
- IC pin
- tracks on PCB
- ground plane on PCB
- negative electrode of load capacitance
- sections of the discharge current path are shared with the input voltage loop

Transient currents through shared inductance (bond wire, tracking) is the cause for "ground bounce". Ground Bounce = Voltage Difference between internal and external ground

$$vl\_s = L\_shared \cdot \frac{di_{L\_shared}}{dt}$$

$$vi\_eff = vi - vl\_s$$

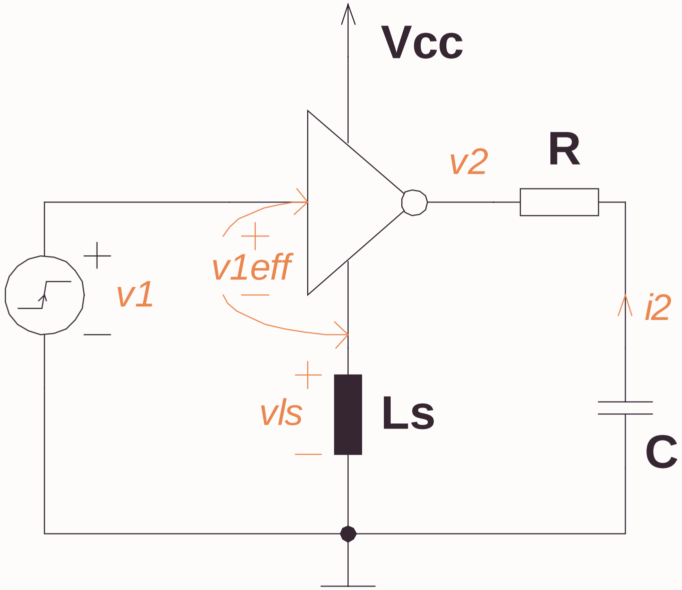
Logic Families/Ground Bounce

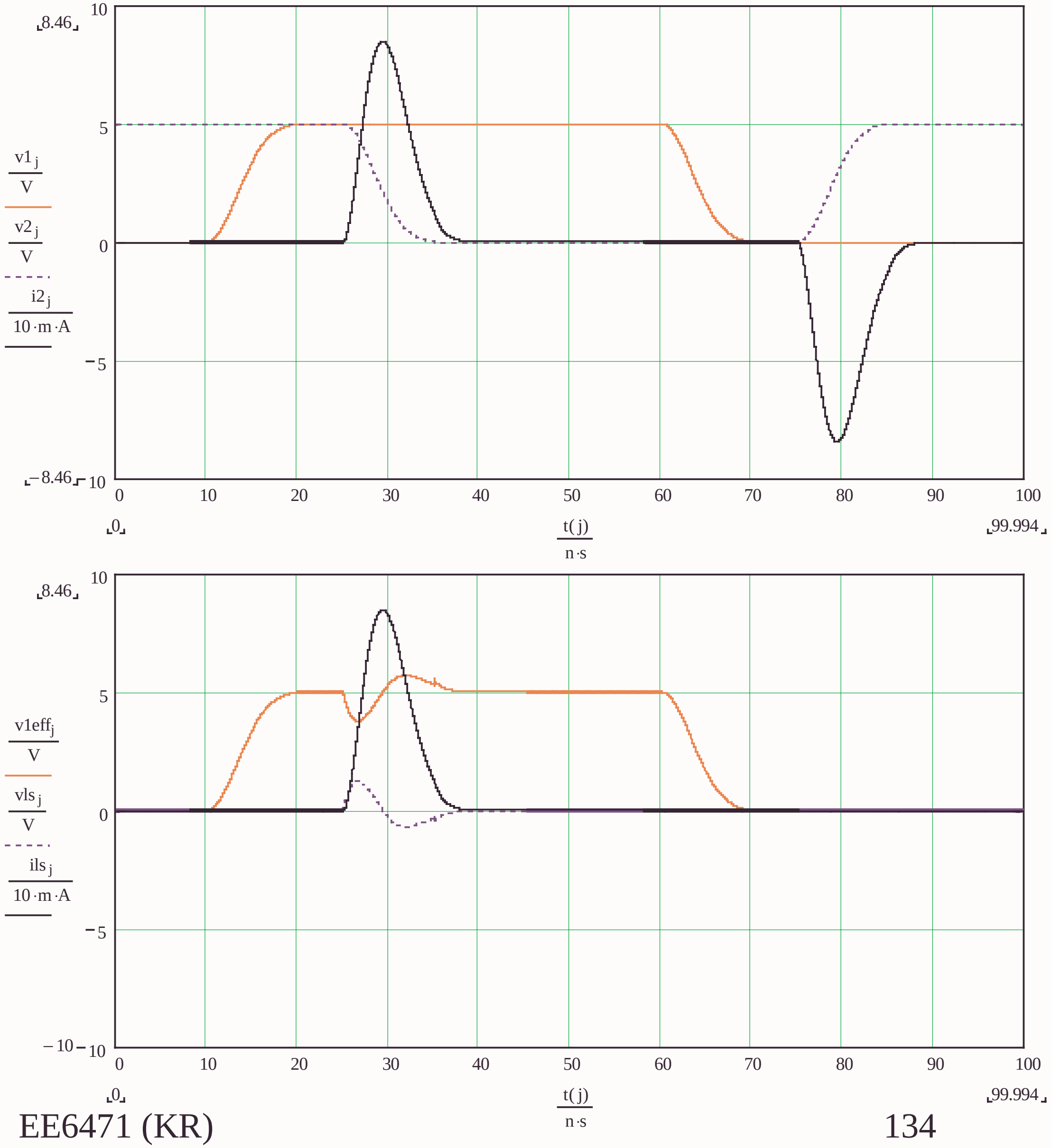


Digital logic gates are differential amplifiers!
They look at input voltages with respect to their ***internal*** ground.
Transient voltages across inductances between internal and external ground distort the input voltage and results in undesired feedback (positive or negative).
Typically ground bounce does not significantly impair the transmitted signal, but it interferes in a major way with signal reception.

What can be done to reduce ground bounce:
•Minimise di/dt by proper choice of gate family
•Minimise shared inductance (star point GND connection)
•Use ICs with separate driver and logic ground pins
•Identify current loops and minimise loop areas

Logic Families/Ground Bounce



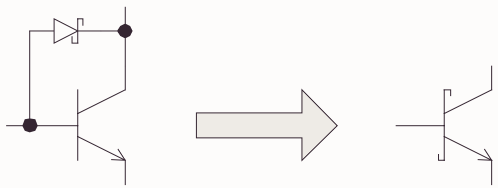


Example Parameter:

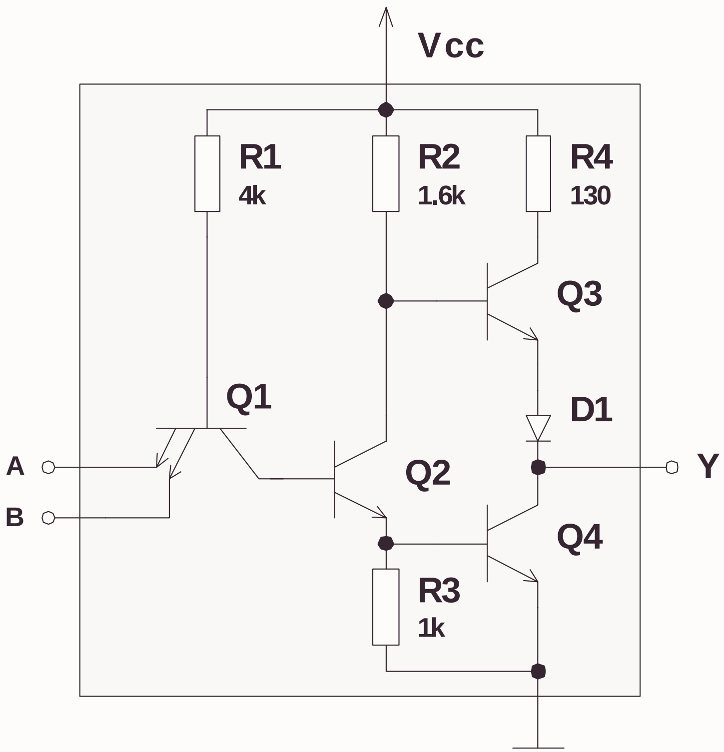
- Vcc=5V
- Tr=10ns
- Tpd=15ns
- Ls=40nH
- C=100pF
- R=10Ω

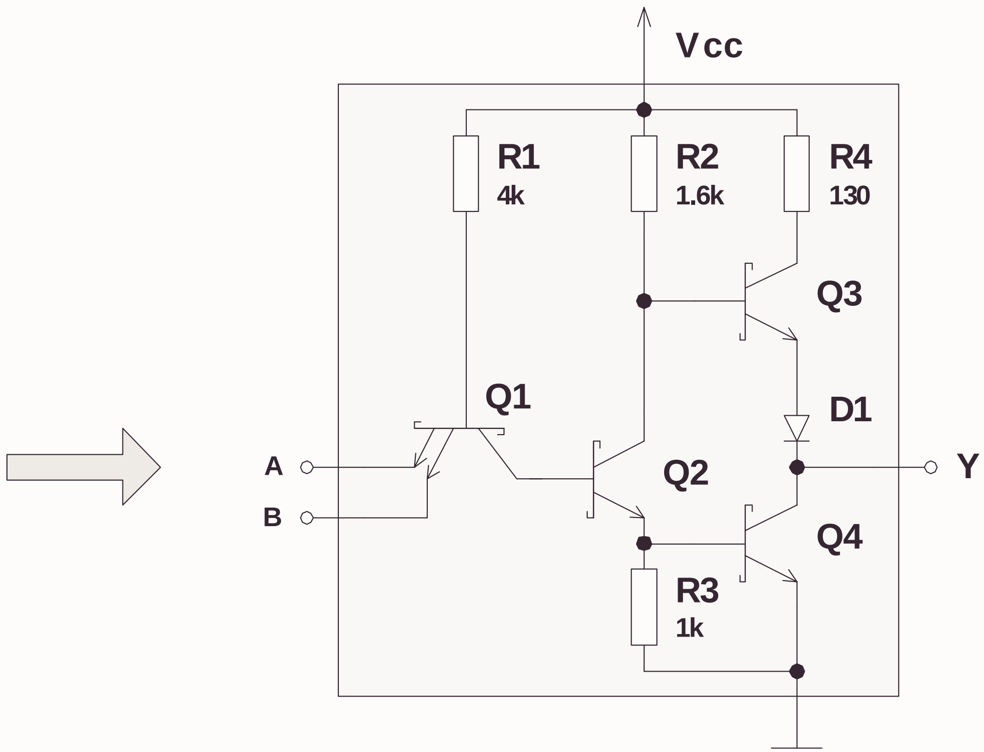
$$vls = Ls \cdot \frac{dils}{dt}$$

Logic Families/TTL/Logic Evolution

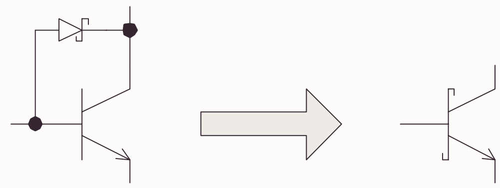


BJT (Bipolar Junction Transistor) storage time reduction by using a BC Schottky diode.
Schottky diode has a Vfw=0.25V. When BC junction becomes forward biased Schottky diode will bypass base current.





Logic Families/TTL/Logic Evolution



74 Series

Bipolar. Saturated BJTs. Practically obsolete. Don't use in new designs!

74S Series

Bipolar. Deep saturation prevented by BC Schottky Diode. Reduced storage-time delay. Practically obsolete.

74AS Series

Innovations in IC design and fabrication. Improvement in speed and power dissipation. Relatively popular. Fastest TTL available.

74LS Series

Bipolar. Lower-power slower-speed version of the 74S Series.

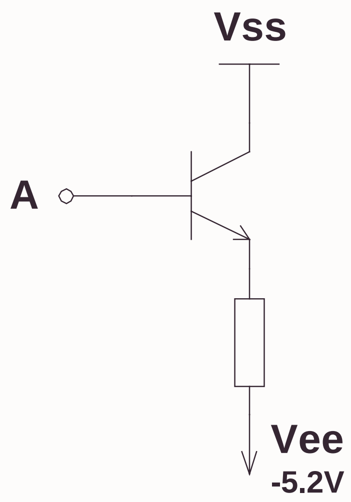
74ALS Series

Innovations in IC design and fabrication. Improvement in speed and power dissipation. Popular.

74F Series

Innovations in IC design and fabrication. Popular.

Logic Families/ECL



TTL
•BJTs operating in saturated mode
•Limited switching speed (storage time)

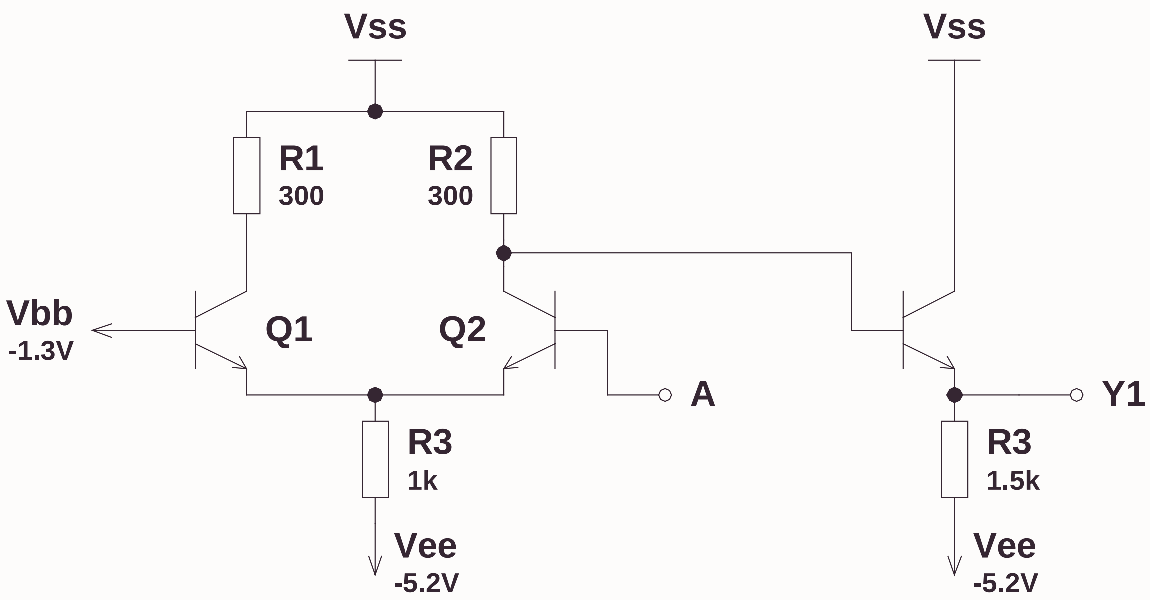
ECL (Emitter-Coupled Logic)
•BJTs operating in unsaturated mode (i.e. emitter-follower mode)
•Principle: Current switching (ECL is also sometimes called Current-Mode-Logic CML)

Advantages of ECL
•fastest logic family available

Disadvantages of ECL
•negative supply (awkward)
•high static power dissipation
•limited choice of manufacturers and devices
•low noise margin

Logic Families/ECL

ECL Inverter



ECL Logic Level Thresholds

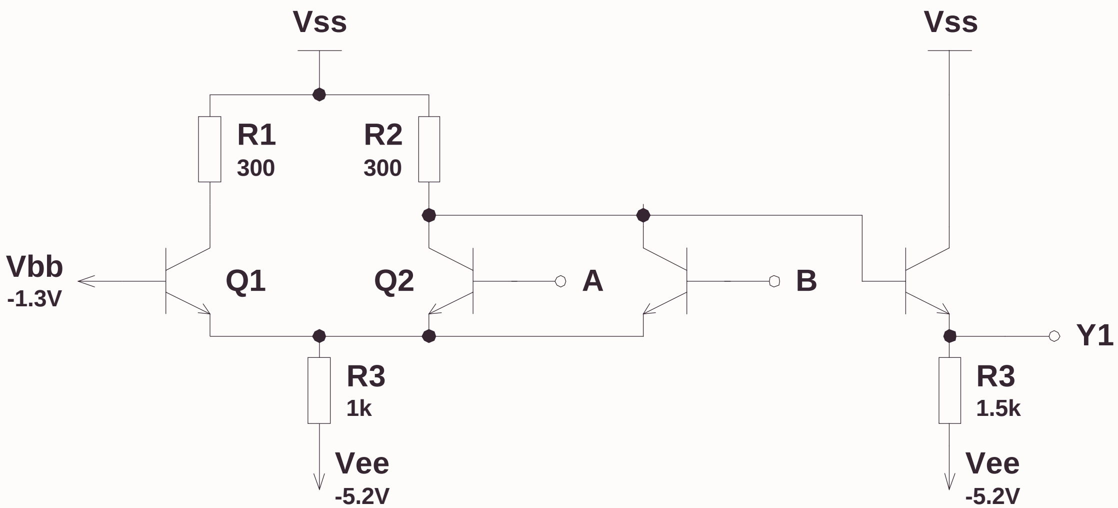
- Logic 0: -1.7V
- Logic 1: -0.8V

ECL Output

- Very low output impedance (typically 7Ω)
- Large fan-out
- Fast charge/discharge of load capacitances

Logic Families/ECL

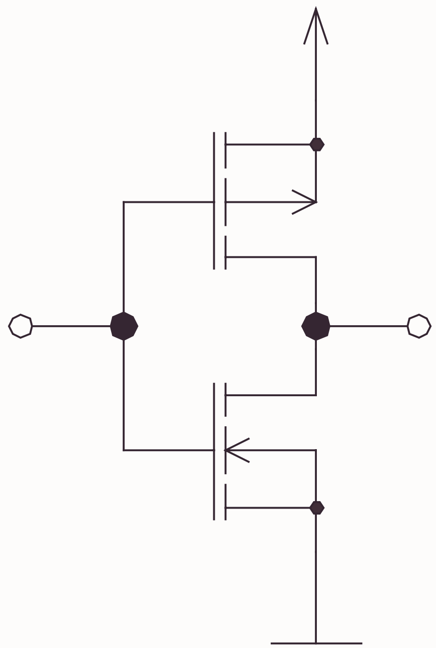
ECL NOR Gate



ECL Summary

- ECL BJTs never saturate. Typical propagation delays 1ns and below
- ECL noise margins are very low (150mV typ)
- Fan-out is high (25)
- Power dissipation remains relatively constant regardless of logic state
- No current spikes during switching transistions
- Negative supply voltages and logic levels makes it awkward to interface ECL to TTL/CMOS.

Logic Families/CMOS



First CMOS logic family CD4000 introduced in 1968.

Because of their advantages CMOS devices have become dominant in the IC market

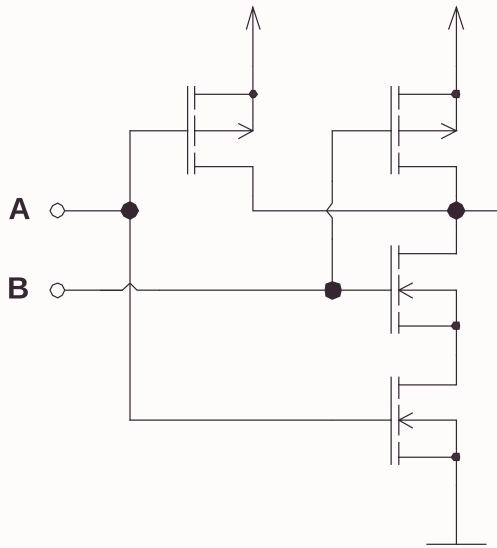
MOS Logic:
MOS: Metal-Oxide-Semiconductor (Metal-Oxide-Silicon

MOS Logic Categories:
•NMOS (obsolete)
•PMOS (obsolete)
•CMOS: complementary MOS

Advantages of MOS
•inexpensive and simple to fabricate
•high speed
•low static power consumption
•scaling of mosfets: higher integration possible
•rail-to-rail outputs

Disadvantages of MOS
•susceptibility to electro-static damage, ESD
•susceptibility to latch-up

Logic Families/CMOS



CMOS Gate Characteristics:

•No resistive elements (resistors elements require large chip areas in bipolar ICs)

•Extremely low static power consumption (Roff > $10^{10}\Omega$)

•Extremely low static input currents

•Cross-conduction and charge/discharge of internal capacitances lead to dynamic power dissipation

•Output Y swings rail-to-rail (low Ron)

•Supply voltage can be reduced to 1V and below

DO NOT leave CMOS inputs floating !

Unused CMOS inputs must be tied to a fixed voltage level (or to another input).

Logic Families/CMOS/Logic Evolution

4000 Series

CMOS. Wide supply voltage range. High noise margin. Low speed. Weak output drive. Practically obsolete.

↓

74C Series

CMOS. Pin-compatible with TTL devices. Low speed. Obsolete. Replaced by HC/HCT family.

↓

74HC/HCT Series

CMOS. Drastic increase in speed. Higher output drive capability. HCT input voltage levels compatible with TTL.

↓

74AC/ACT Series

CMOS. Functionally compatible, but not pin-compatible to TTL. Improved noise immunity and speed. ACT inputs are TTL compatible.

74AHC/AHCT Series

CMOS. Improved speed, lower power, lower drive capability.

BiCMOS Logic

CMOS/Bipolar. Combine the best features of CMOS and bipolar. Low power high speed. Bus interfacing applications (74BCT, 74ABT)

74LVC/ALVC/LV/AVC

CMOS. Reduced supply voltage.
LVC: 5V/3.3V translation
ALVC: Fast 3.3V only
AVC: Optimised for 2.5V, down to 1.2V

CMOS Logic Trend:
Reduction of dynamic losses (cross-conduction, capacitive charge/discharge cycles) by decreasing supply voltages
(12V→5V → 3.3V → 2.5V → 1.8V → 1.5V…).

Reduction of IC power dissipation is the key to:
•lower cost (packaging)
•higher integration
•improved reliability

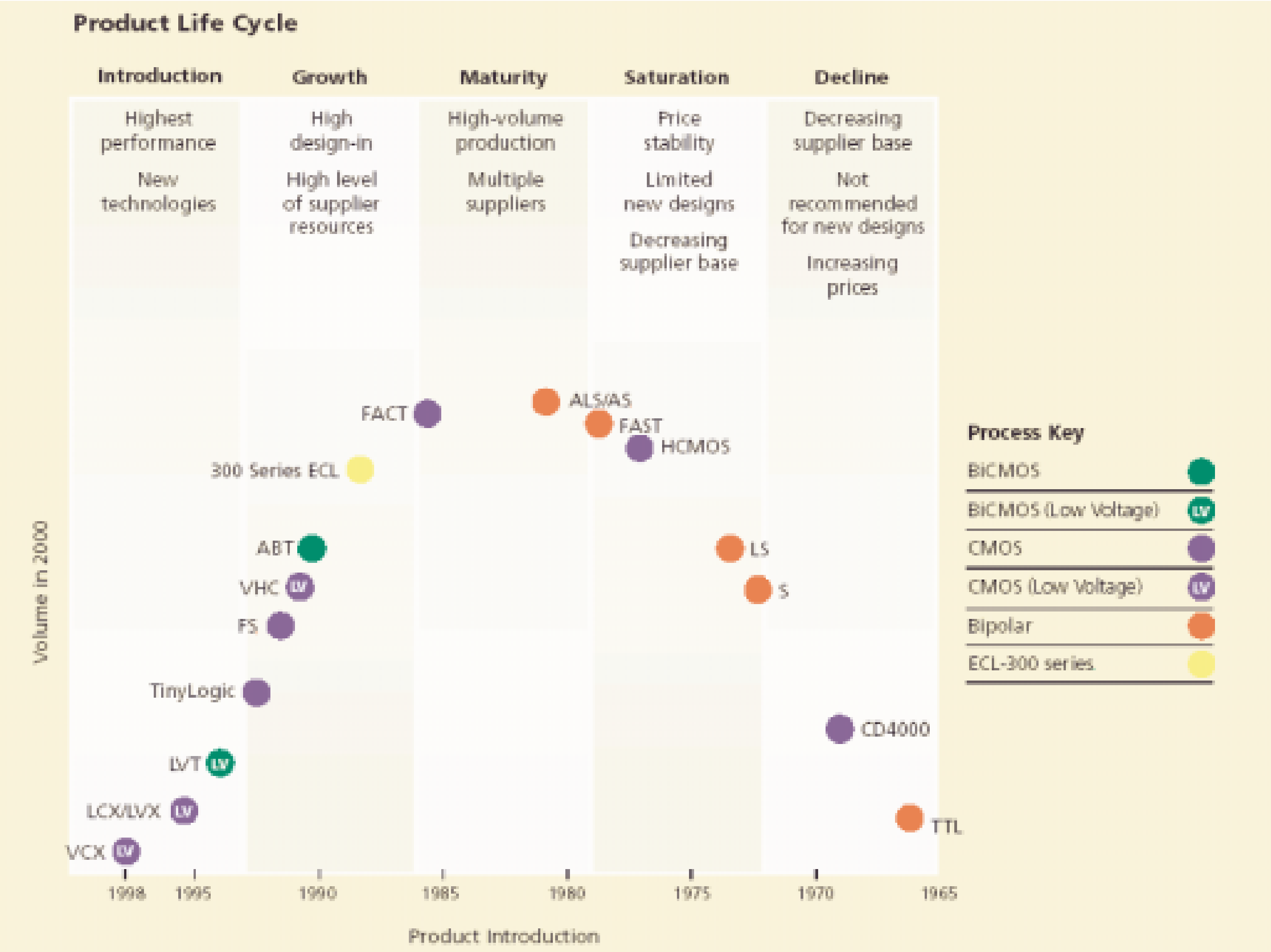
Logic Families/Overview

Logic Family	Prop. Delay	Rise/Fall Time	Vih_{min}	Vil_{max}	Voh_{min}	Vol_{max}	Noise Margin
74	22ns		2.0V	0.8V	2.4V	0.4V	0.4V
74LS	15ns		2.0V	0.8V	2.7V	0.5V	0.3V
74F	5ns	2.3ns	2.0V	0.8V	2.7V	0.5V	0.3V
74AS	4.5ns	1.5ns	2.0V	0.8V	2.7V	0.5V	0.3V
74ALS	11ns	2.3ns	2.0V	0.8V	2.5V	0.5V	0.3V
ECL	1.45ns	0.35ns	-1.165V	-1.475V	-1.025V	-1.610V	0.135V
4000	250ns	90ns	3.5V	1.5V	4.95V	0.05V	1.45V
74C	90ns		3.5V	1.5V	4.5V	0.5V	1V
74HC	18ns	3.6ns	3.5V	1.0V	4.9V	0.1V	0.9V
74HCT	23ns	3.9ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AC	9ns	1.5ns	3.5V	1.5V	4.9V	0.1V	1.4V
74ACT	9ns	1.5ns	2.0V	0.8V	4.9V	0.1V	0.7V
74AHC	3.7ns		3.85V	1.65V	4.4V	0.44V	0.55V

(Typical values for rough comparison only. Refer to datasheet. Values valid for Vcc=5V)

Care is needed when driving inputs of one logic family by outputs of a different family !
Watch voltage levels and fan-out !

Logic Families/Overview



http://www.fairchildsemi.com/collateral/lsg2000.pdf

View of a Logic IC manufacturer (Fairchild)… Biased?