

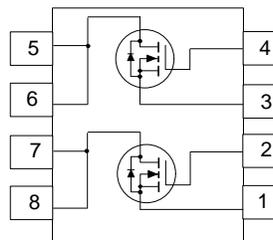
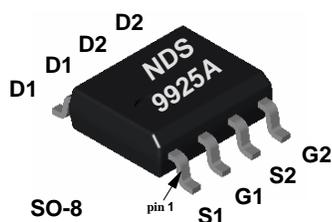
NDS9925A Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

SO-8 N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 4.5 A, 20 V. $R_{DS(ON)} = 0.060 \Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 0.075 \Omega @ V_{GS} = 2.7 \text{ V}$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

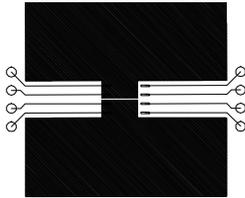
Symbol	Parameter	NDS9925A	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 8	V
I_D	Drain Current - Continuous (Note 1a)	4.5	A
	- Pulsed	15	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

Electrical Characteristics (T_A = 25°C unless otherwise noted)

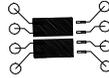
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	20			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 8 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -8 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.4		1	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 4.5 V, I _D = 4.5 A			0.06	Ω
		V _{GS} = 2.7 V, I _D = 4 A			0.075	
I _{D(on)}	On-State Drain Current	V _{GS} = 4.5 V, V _{DS} = 5 V	15			A
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Diode Forward Current				1.3	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A (Note 2)			1.2	V

Notes :

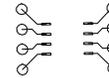
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 78°C/W on a 0.5 in² pad of 2oz copper.



b. 125°C/W on a 0.02 in² pad of 2oz copper.



c. 135°C/W on a 0.003 in² pad of 2oz copper.

- Scale 1 : 1 on letter size paper
 2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

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