FAIRCHILD SEMICONDUCTOR®

March 2008

NC7WZ07
TinyLogic® UHS Dual Buffer (Open Drain Outputs)

Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ leadless package
- Ultra High Speed: t_{PZL} 2.3ns Typ. into 50pF at 5V V_{CC}
- High I_{OL} Output Drive: +24mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

General Description

The NC7WZ07 is a dual buffer with open drain outputs from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and outputs are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 7V independent of V_{CC} operating voltage.

Ordering Information

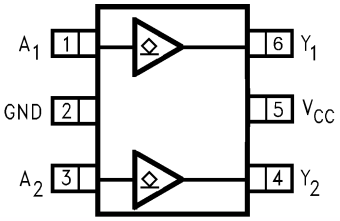
Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WZ07P6X	MAA06A	Z07	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7WZ07L6X	MAC06A	D3	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

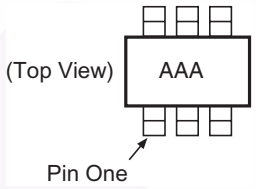
Connection Diagram

Pin Assignments for SC70



(Top View)

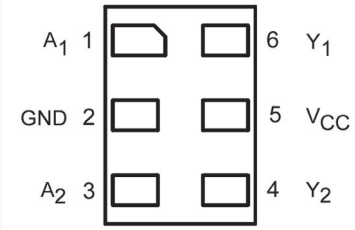
Pin One Orientation Diagram



AAA represents Product Code Top Mark – see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



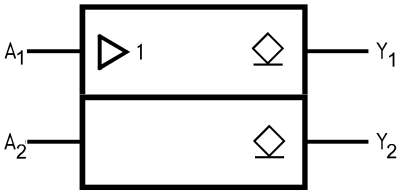
(Top Thru View)

Pin Description

Pin Names	Description
A_1, A_2	Data Inputs
Y_1, Y_2	Output

Logic Symbol

IEEE/IEC



Function Table

Y = A

Input	Output
A	**Y**
L	L
H	Z

H = HIGH Logic Level

L = LOW Logic Level

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7V
V_{IN}	DC Input Voltage	–0.5V to +7V
V_{OUT}	DC Output Voltage	–0.5V to +7V
I_{IK}	DC Input Diode Current @ V_{IN} < –0.5V	–50mA
I_{OK}	DC Output Diode Current @ V_{OUT} < –0.5V	–50mA
I_{OUT}	DC Output Current	+50mA
I_{CC}/I_{GND}	DC V_{CC}/GND Current	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature Under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation @ +85°C	180mW

Recommended Operating Conditions(1)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage Operating	1.65V to 5.5V
	Supply Voltage Data Retention	1.5V to 5.5V
V_{IN}	Input Voltage	0V to 5.5V
V_{OUT}	Output Voltage	0V to 5.5V
T_A	Operating Temperature	–40°C to +85°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 1.8V ± 0.15V, 2.5V ± 0.2V	0ns/V to 20ns/V
	V_{CC} = 3.3V ±0.3V	0ns/V to 10ns/V
	V_{CC} = 5.0V ±0.5V	0ns/V to 5ns/V
θ_{JA}	Thermal Resistance	350°C/W

Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.65–1.95		0.75 x V_{CC}			0.75 x V_{CC}		V
		2.3–5.5		0.7 x V_{CC}			0.7 x V_{CC}		
V_{IL}	LOW Level Input Voltage	1.65–1.95				0.25 x V_{CC}		0.25 x V_{CC}	V
		2.3–5.5				0.3 x V_{CC}		0.3 x V_{CC}	
I_{LKG}	HIGH Level Output Leakage Current	1.65–5.5	V_{IN} = V_{IH}, V_{OUT} = V_{CC} or GND			±5		±10	µA
V_{OL}	LOW Level Output Voltage	1.65	V_{IN} = V_{IL} I_{OL} = 100µA		0.0	0.1		0.0	V
		1.8			0.0	0.1		0.1	
		2.3			0.0	0.1		0.1	
		3.0			0.0	0.1		0.1	
		4.5			0.0	0.1		0.1	
		1.65	I_{OL} = 4mA		0.08	0.24		0.24	
		2.3	I_{OL} = 8mA		0.10	0.3		0.3	
		3.0	I_{OL} = 16mA		0.16	0.4		0.4	
		3.0	I_{OL} = 24mA		0.24	0.55		0.55	
		4.5	I_{OL} = 32mA		0.25	0.55		0.55	
I_{IN}	Input Leakage Current	0–5.5	0 ≤ V_{IN} ≤ 5.5V			±0.1		±1.0	µA
I_{OFF}	Power Off Leakage Current	0.0	V_{IN} or V_{OUT} = 5.5V			1		10	µA
I_{CC}	Quiescent Supply Current	1.65–5.5	V_{IN} = 5.5V, GND			1.0		10	µA

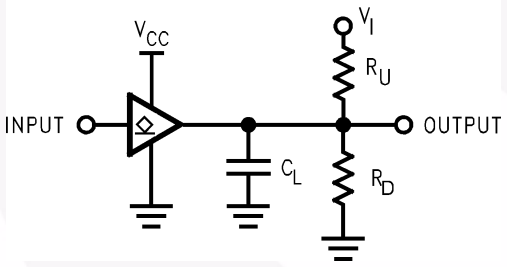
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = –40°C to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{PZL}	Propagation Delay	1.65	C_L = 50pF, RU = 500Ω, RD = 500Ω, V_I = 2 x V_{CC}	1.8	6.6	11.5	1.8	12.6	ns	Figure 1 Figure 3
		1.8		1.8	5.5	9.5	1.8	10.5		
		2.5 ± 0.2		1.2	3.7	5.8	1.2	6.4		
		3.3 ± 0.3		0.8	2.9	4.4	0.8	4.8		
		5.0 ± 0.5		0.5	2.3	3.5	0.5	3.9		
t_{PLZ}	Propagation Delay	1.65	C_L = 50pF, RU = 500Ω, RD = 500Ω, V_I = 2 x V_{CC}	1.8	5.5	11.5	1.8	12.6	ns	Figure 1 Figure 3
		1.8		1.8	4.3	9.5	1.8	10.5		
		2.5 ± 0.2		1.2	2.8	5.8	1.2	6.4		
		3.3 ± 0.3		0.8	2.1	4.4	0.8	4.8		
		5.0 ± 0.5		0.5	1.4	3.5	0.5	3.9		
C_{IN}	Input Capacitance	0			2.5				pF	
C_{OUT}	Output Capacitance	0			4.0				pF	
C_{PD}	Power Dissipation Capacitance	3.3	(2)		3				pF	Figure 2
		5.0			4					

Note:

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0MHz; t_W = 500ns

Figure 1. AC Test Circuit

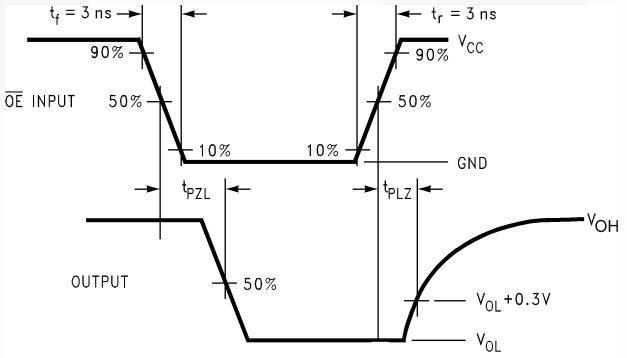
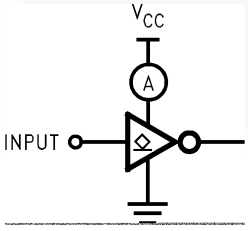


Figure 3. AC Waveforms



Input = AC Waveform; $t_r = t_f$ = 1.8ns;
PRR = 10MHz; Duty Cycle = 50%

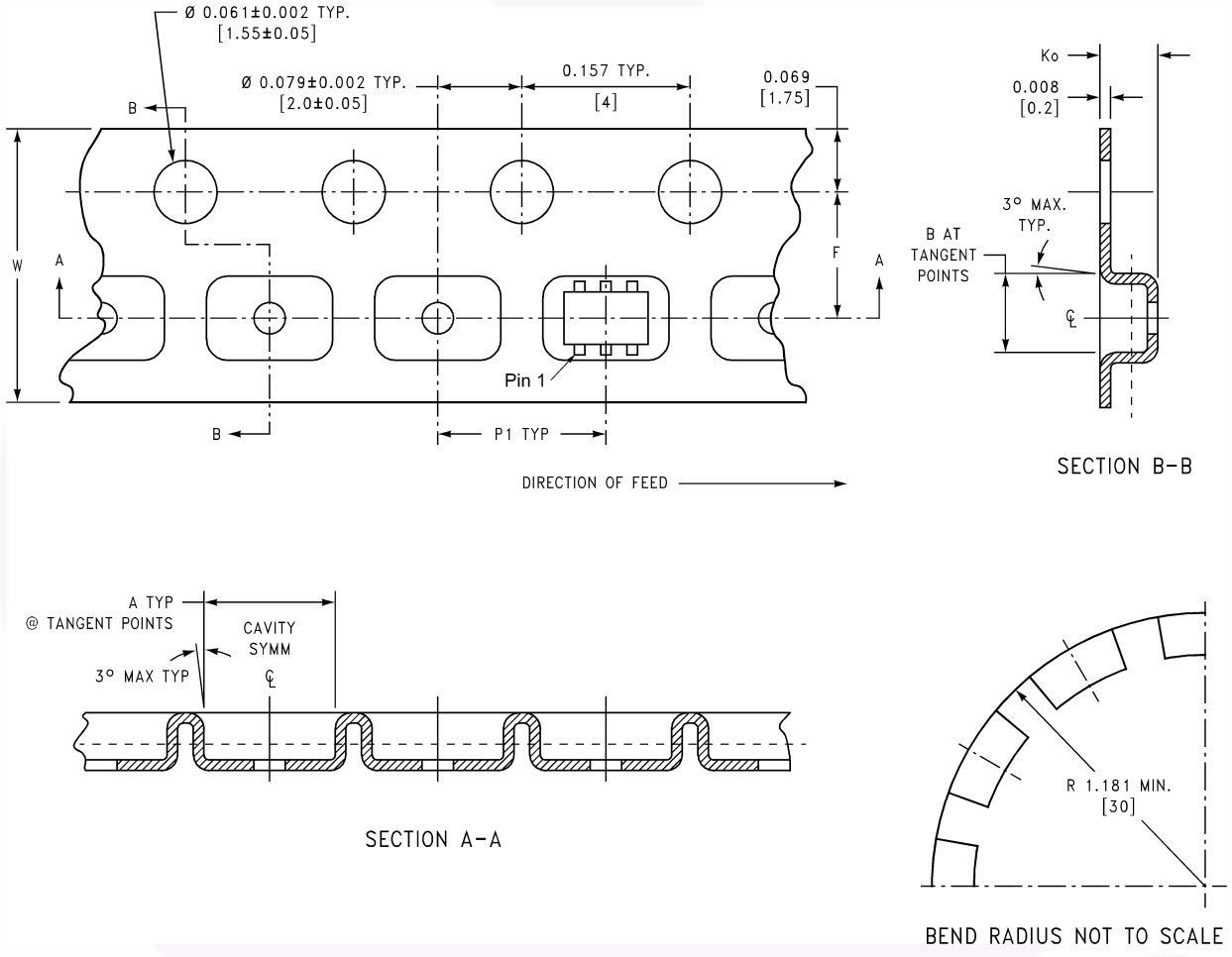
Figure 2. I_{CCD} Test Circuit

Tape and Reel Specification

Tape Format for SC70

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
P6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

Tape Dimensions inches (millimeters)

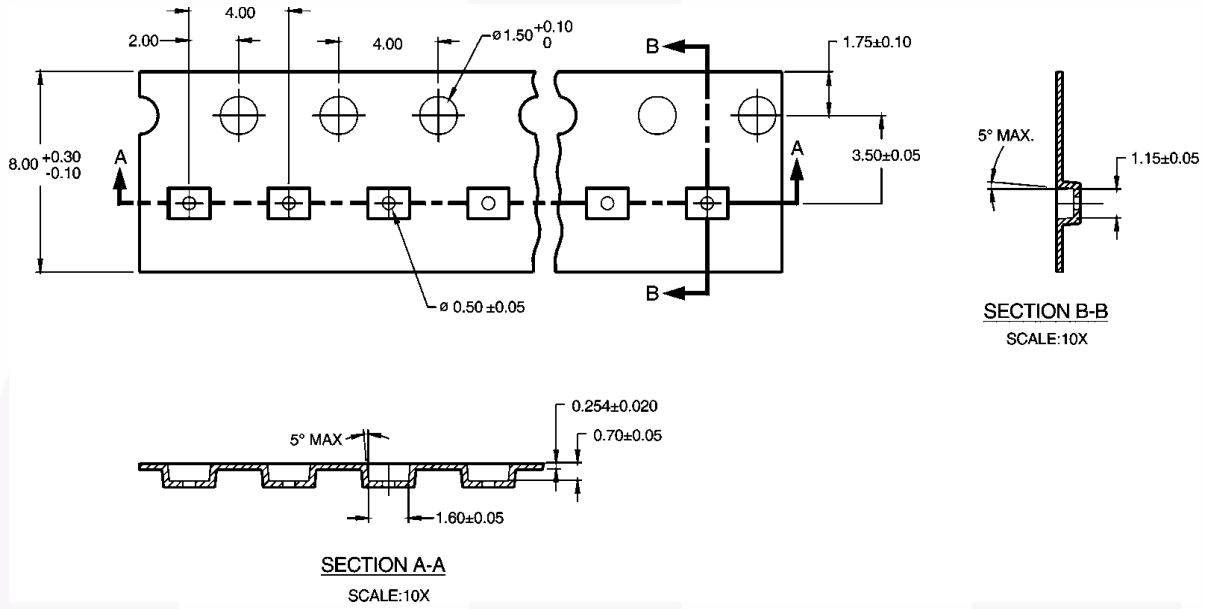


Package	Tape Size	Dim A	Dim B	Dim F	Dim K_o	Dim P1	Dim W
SC70-6	8mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)

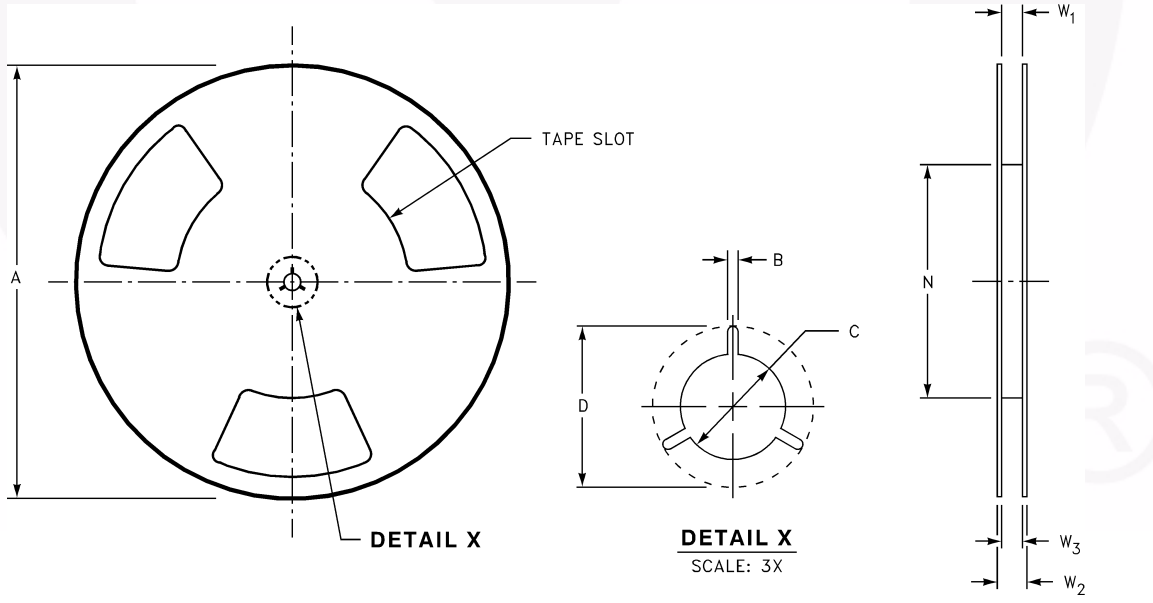
Tape and Reel Specifications

Tape Format for MicroPak

Package Designator	Tape Section	Number of Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed



Reel Dimensions inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions

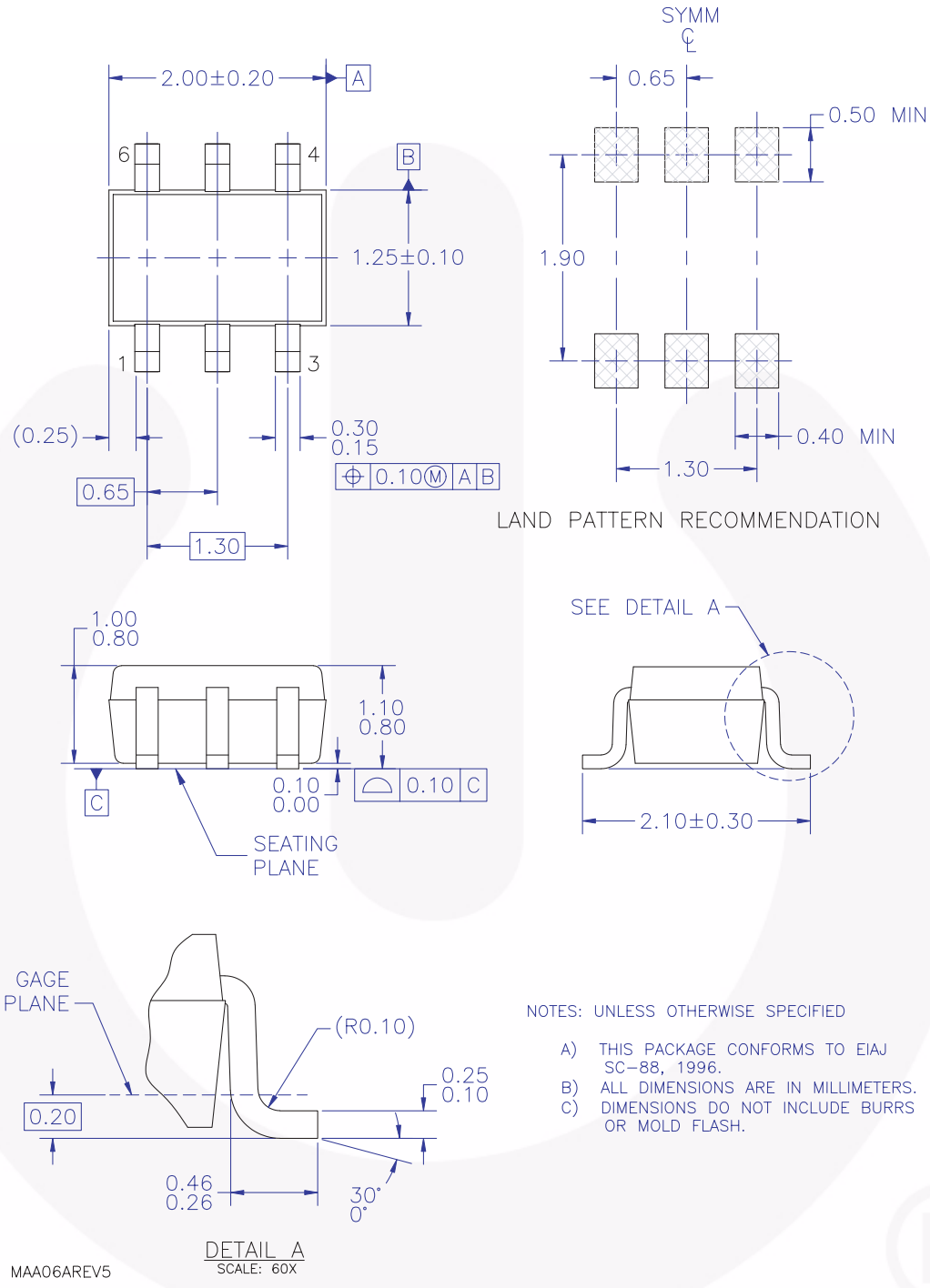


Figure 4. 6-Lead SC70, EIAJ SC88, 1.25mm Wide

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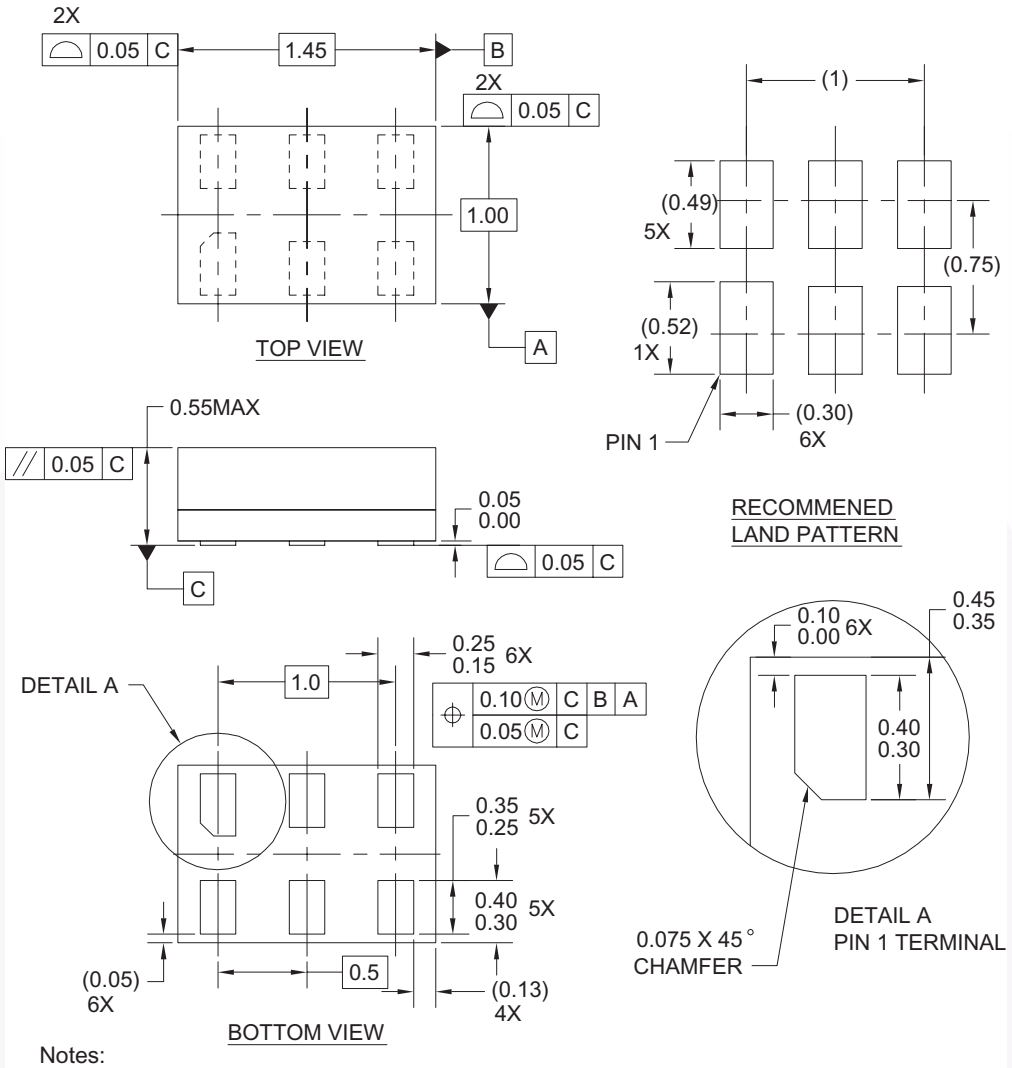
Physical Dimensions (Continued)



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 5. 6-Lead MicroPak, 1.0mm Wide

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