Nordic VLSI ASA

430MHz-950MHz Single Chip RF Transceiver

nRF903

FEATURES

- Single chip GFSK multi-channel transceiver
- 433MHz, 868MHz and 915MHz ISM/LPRD-bands compatible
- 76.8kbit/s data rate
- High bandwidth efficiency
- Easy 14-bit configuration
- Reliable communication due to superior adjacent channel selectivity
- Full output power in all ISM-bands
- Few external components required
- Standby- and power down-mode

APPLICATIONS

- Alarm and Security Systems
- Automotive
- Home Automation
- Automatic Meter Reading (AMR)
- Wireless Handsfree
- Remote Control
- Surveillance
- Wireless Communications
- Telemetry
- Toys

GENERAL DESCRIPTION

nRF903 is a true single chip multi-channel UHF transceiver designed to operate in the unlicensed 433MHz, 868MHz and 915MHz ISM-/LPRD- (Industrial Scientific Medical / Low Power Radio Device) bands. Multi-channel operation, excellent receiver selectivity and sensitivity, high bandwidth efficiency and blocking performance make the nRF903 suitable for wireless links where high reliability is a key requirement.

The device features GFSK (Gaussian Frequency Shift Keying) modulation and demodulation capability at an effective bit rate of 76.8kbit/s in 153.6kHz channel bandwidths. Transmit power can be adjusted to a maximum of 10dBm which is available for all frequency bands and channels. Antenna interface is differential and suited for low cost PCB-antennas. All necessary configuration data is programmed by a 14-bit configuration word via a Serial Peripheral Interface (SPI). nRF903 operates from a single +3V DC supply and features power down- and standby-modes which makes power saving easy and efficient.

QUICK REFERENCE DATA

Parameter		Value	Unit
Frequency bands		433.05 - 434.87 868 - 870 902-928	MHz
Datarate		76.8	kbit/s
Sensitivity @ 300Ω, BR=76.8kbit/s, BER<10^{-3}		-104	dBm
Modulation		GFSK	
Blocking performance (>1 MHz from carrier)		>50	dB
Max. RF output power @ 300Ω, 3V		10	dBm
Supply voltage		2.7 – 3.3	V
Number of available channels	433.05 - 434.87 MHz 868 - 870 MHz 902-928 MHz	10 7 169	-

Table 1. nRF903 quick reference data.

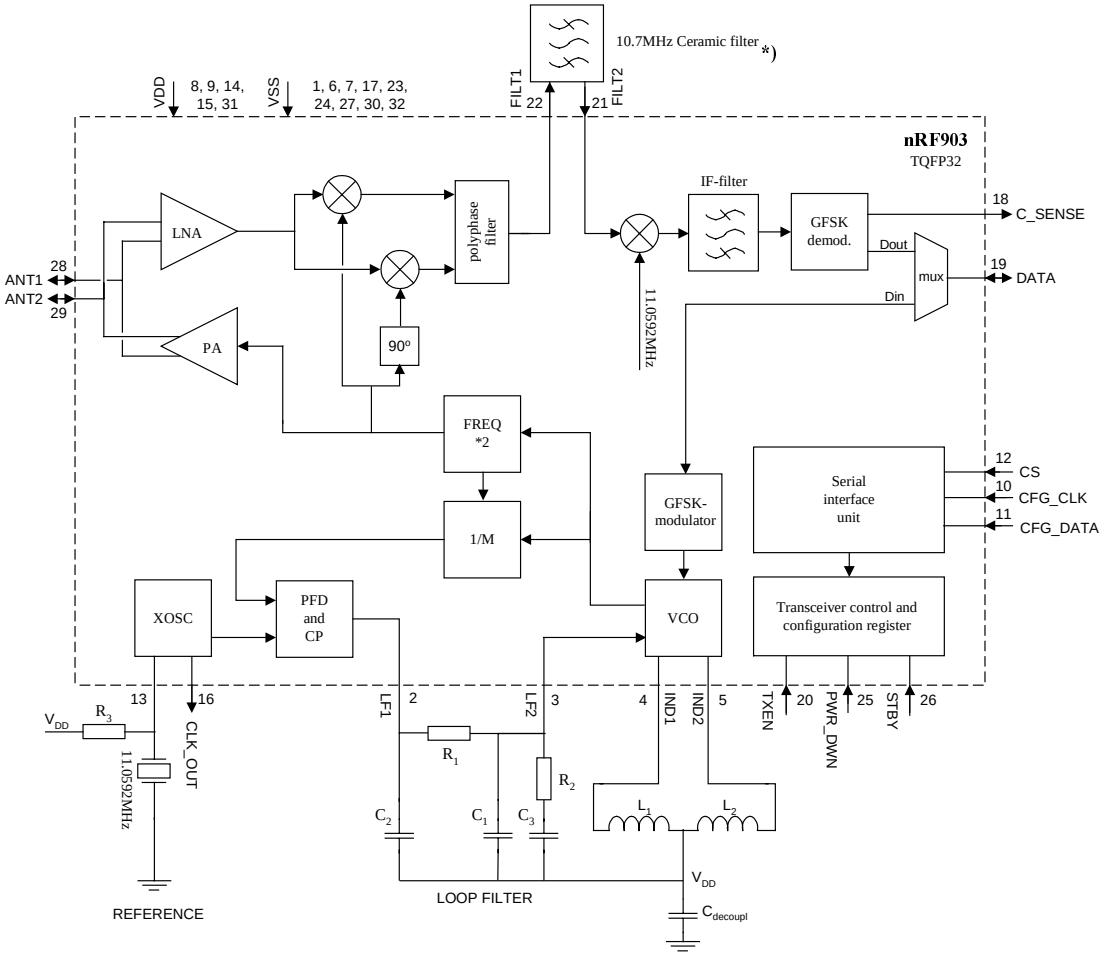
As a primary application, the transceiver is intended for UHF radio equipment in compliance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 and the US Federal Communications Commission (FCC) standard CFR47, part 15.

ORDERING INFORMATION

Type number	Description	Version
nRF903-IC	32 pin TQFP	A
nRF903-EVKIT-433	Evaluation kit (2 test PCBs)	1.0
nRF903-EVKIT-868	Suffix designate frequency band	1.0
nRF903-EVKIT-915		1.0
nRF903-DEMO	Demonstration kit (4 transceiver units)	1.0

Table 2. nRF903 ordering information.

BLOCK DIAGRAM



*) The external filter may be replaced with a 10nF capacitor at the expense of receiver performance (see page 18)

Figure 1. nRF903 block diagram with external components.

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	VSS	Ground	Ground (0V)
2	LF1	Output	Frequency synthesiser PLL loopfilter connection #1
3	LF2	Input	Frequency synthesiser PLL loopfilter connection #2
4	IND1	Input	External inductor for VCO
5	IND2	Input	External inductor for VCO
6	VSS	Ground	Ground (0V)
7	VSS	Ground	Ground (0V)
8	VDD	Power	Power supply (+3.0V DC)
9	VDD	Power	Power supply (+3.0V DC)
10	CFG_CLK	Input	Clock for programming mode
11	CFG_DATA	Input	Serial input for transceiver configuration data
12	CS	Input	Chip select CS = ”0” ⇒ transceiver normal operating mode CS = ”1” ⇒ transceiver programming mode/test mode Refer to Table 5. for mode setup
13	XC1	Input	Crystal oscillator input (11.0592MHz)
14	VDD	Power	Power supply (+3.0V DC)
15	VDD	Power	Power supply (+3.0V DC)
16	CLK_OUT	Output	Full swing clock for external microcontroller Output frequency is set by 2 bits in the configuration word f_{CLK_OUT}=11.0592MHz/*n*, where *n* is 1,2,4 or 8
17	VSS	Ground	Ground (0V)
18	C_SENSE	Output	Receiver carrier sense
19	DATA	Bidirectional	Transmitted/received data
20	TXEN	Input	Select transmit/receive mode TXEN = ”0” ⇒ Receive mode TXEN = ”1” ⇒ Transmit mode
21	FILT2	Input	Input from external 10.7MHz IF filter
22	FILT1	Output	Output to external 10.7MHz IF filter
23	VSS	Ground	Ground (0V)
24	VSS	Ground	Ground (0V)
25	PWR_DWN	Input	Power down mode Refer to Table 5. for mode setup
26	STBY	Input	Standby mode Refer to Table 5. for mode setup
27	VSS	Ground	Ground (0V)
28	ANT1	Bidirectional	Antenna terminal
29	ANT2	Bidirectional	Antenna terminal
30	VSS	Ground	Ground (0V)
31	VDD	Power	Power supply (+3.0V DC)
32	VSS	Ground	Ground (0V)

Table 3. nRF903 pin functions.

ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V DC, VSS = 0V, T_A= -40°C to +85°C

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
VDD	Supply voltage	2.7	3	3.3	V
t	Operating temperature range	-40	27	+85	°C
I_{DD}	Total current consumption:				
	Receive mode : 433MHz		18.5		mA
	: 868-928MHz		22.5		mA
	Transmit mode @ -8 dBm RF power : 433MHz		12.5		mA
	: 868-928MHz		15.5		mA
	Transmit mode @ 10 dBm RF power : 433MHz		24		mA
	: 868-928MHz		29.5		mA
	Standby mode		600		µA
	Power-down mode			1	µA
#CH	Number of available channels with fixed inductor [1]	169			
	Modulation type		GFSK		
Δf	Frequency deviation	±19	±23	±27	kHz
BR	Bit rate		76.8		kbit/s
P_{RF}	Max. RF output power @ 300Ω load		10		dBm
	Sensitivity @ 300Ω, BR=76.8kbit/s, BER < 10^{-3}		-104		dBm
CH_{BW}	Channel spacing		153.6		kHz
f_{res}	Frequency synthesizer resolution		153.6		kHz
ACS	Adjacent channel selectivity [2]; upper channel (+2):		42		dB
	upper channel (+1):		32		dB
	lower channel (-1):		21		dB
	lower channel (-2):		42		dB
MIA	Mirror image attenuation	15	30		dB
BLCK	Blocking level ($f_{blocking\ signal}$ > 1MHz from carrier)		53		dB
ACP_{GMSK}	Adjacent channel power (76.8kbit/s)		-37	-35	dBc
DR	Dynamic range		90		dB
P_{C_SENSE}	Carrier sense input power level; stable '0':		-105		dBm
	Carrier sense input power level; stable '1':		-92		
f_{IF1}	1st IF frequency		10.7136		MHz
f_{IF2}	2nd IF frequency		345.6		kHz
BW_{IF}	IF noise bandwidth		130		kHz
f_{XTAL}	Crystal frequency		11.0592		MHz
	Crystal reference frequency stability requirement				
	@ 433MHz, BR = 76.8kbit/s			±40	ppm
	@ 868-928MHz, BR = 76.8kbit/s			±20	ppm
$f_{µP\_CLK}$	External microcontroller clock output frequency [3]	1.3824		11.0592	MHz
V_{IH}	Logic "1" input voltage	$0.7 \cdot V_{DD}$		V_{DD}	V
V_{IL}	Logic "0" input voltage	0		$0.3 \cdot V_{DD}$	V
V_{OH}	Logic "1" output voltage (I_{OH} = - 1.0mA)	$0.7 \cdot V_{DD}$		V_{DD}	V
V_{OL}	Logic "0" output voltage (I_{OL} = 1.0mA)	0		$0.3 \cdot V_{DD}$	V
I_H	Logic "1" input current (V_I = VDD)			+20	µA
I_L	Logic "0" input current (V_I = VSS)			-20	µA
Z_I	Recommended antenna port differential impedance		300		Ω
	Spurious emission [4]	Compliant with ETSI EN 300-220-1 And FCC CFR47, part 15			

1): Use must be according to ETSI- and FCC frequency regulations. Table 7, page 9, lists the available channels for the three different frequency bands.

2): Refer to the *Adjacent channel selectivity (ACS)* section on page 24

3): $f_{µP\_CLK}$ may be set to 1.3824MHz, 2.7648MHz, 5.5296MHz or 11.0592MHz depending on configuration word (see Table 6)

4): Antenna and matching network must be according to recommendations

Table 4. nRF0903 electrical specifications.

ABSOLUTE MAXIMUM RATINGS

Supply voltages
VDD .....- 0.3V to +6V
VSS 0V

Input voltage
V_I.....- 0.3V to VDD + 0.3V

Output voltage
V_O.....- 0.3V to VDD + 0.3V

Power dissipation
P_D (T_A=25°C) 300mW

Temperatures
Operating Temperature…. -40°C to +85°C
Storage Temperature….. -55°C to +125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!
Electrostatic Sensitive Device
Observe Precaution for handling

PIN ASSIGNMENT

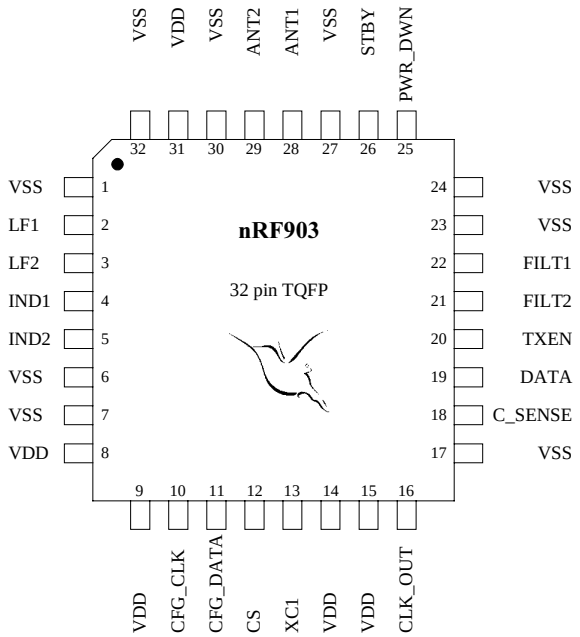
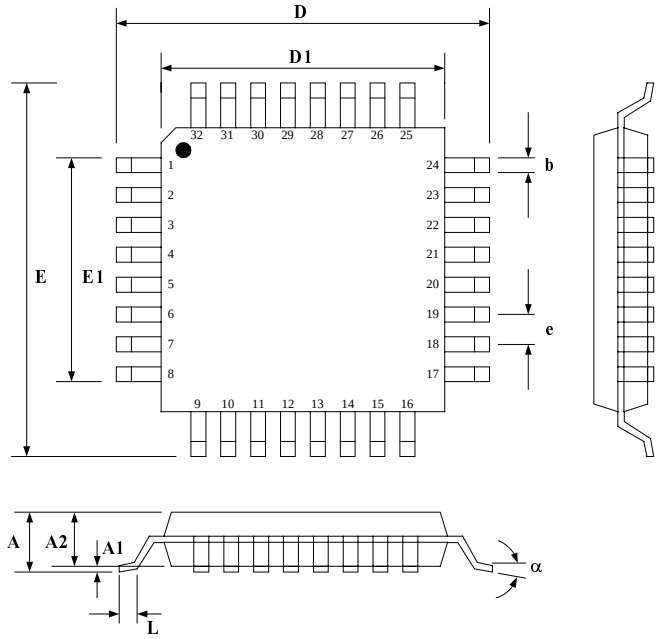


Figure 2. nRF903 pin assignment.

PACKAGE OUTLINE

nRF903, 32 pin TQFP. (Dimensions in mm.)



Package Type		E1/D1	E/D	A	A1	A2	e	b	L	α	Copl
32 pin TQFP	**Min**	7.00	9.00		0.05	1.35	0.80	0.30	0.45	0°	
	Max			1.60	0.15	1.45		0.45	0.75	7°	0.10

Figure 3. TQFP32 Package outline.

APPLICATION INFORMATION

User interface

Figure 4 shows the user interface of nRF903 which consists of a total of 9 digital input/output pins.

The interface is divided into two main functions: Configuration and Mode-control. In addition, a receiver carrier sense signal (C_SENSE) and a microprocessor clock output signal (CLK_OUT) is available.

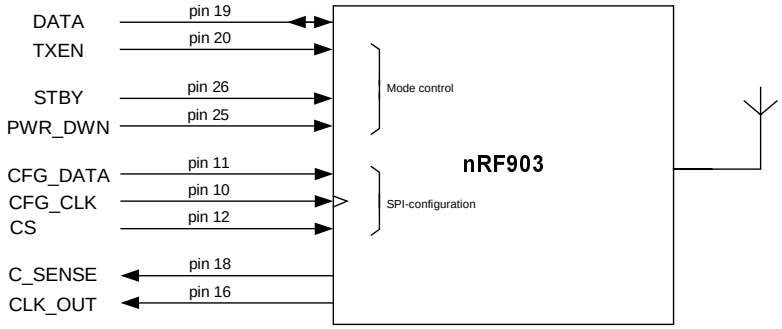


Figure 4. nRF903 user interface

C_SENSE is stable low when no carrier is detected in the received channel. As the power-level increases, the average duty-cycle of the C_SENSE signal increases to the point where it is stable high for input power levels approx. 10dB above the sensitivity limit. A positive transition on the C_SENSE-pin may be used to initiate the listening procedure in the micro-controller used to process data.

CLK_OUT is the full-swing 11.0592MHz reference frequency divided by 1,2,4 or 8. At high output frequencies the peak-to-peak voltage is reduced in order to keep switching noise down.

Configuration is performed by clocking a 14-bit configuration word into a shift-register (see Table 6).
These 14 bits are decoded into the corresponding frequency band, channel, output power and output clock frequency. The Serial Peripheral Interface (SPI) consists of the pins CFG_DATA, CFG_CLK and CS. Once configured, these pins are not used unless one or more of the parameters above need to be changed.

Modes of operation

Mode-control is set by the pins STBY, PWR_DWN, TXEN and CS. Table 5 shows the operating mode according to signal settings. For complete overview see Table 9, p. 12.

nRF903 operating mode	STBY	PWR_DWN	TXEN	CS
Normal operation: Receive mode	0	0	0	0
Normal operation: Transmit mode	0	0	1	0
Power-down mode: No circuitry active	0	1	X	X
Standby mode: Only XOSC- and Pin 16 (CLK_OUT) active. CLK_OUT frequency is 11.0592MHz before configuration	1	0	X	X

Table 5. nRF903 operational mode as a function of external signals STBY, PWR_DWN, TXEN and CS

Transceiver configuration

A total of 4 parameters are set by the user in an internal 14-bit configuration register. Table 6 shows the contents of the register. Bit 13 is the most significant bit (MSB).

Bit	Parameter	Symbol	Description	#bit
0-1	**Frequency band**	FB	"00" ⇒ Frequency band = 433.92 ± 0.87 MHz "01" ⇒ Frequency band = 869 ± 1 MHz "10" ⇒ Frequency band = 915 ± 13 MHz "11" ⇒ Not in use	2
2-9	**Channel centre position (Channel number)**	CH	$f_{centre\_433MHz} = 433.1902 \cdot 10^6 + CH \cdot 153.6 \cdot 10^3$ [Hz] $f_{centre\_868MHz} = 868.1856 \cdot 10^6 + CH \cdot 153.6 \cdot 10^3$ [Hz] $f_{centre\_915MHz} = 902.1696 \cdot 10^6 + CH \cdot 153.6 \cdot 10^3$ [Hz]	8
10-11	**Output power**	P_{OUT}	Output power setting "00" ⇒ P_{out} = -8dBm "01" ⇒ P_{out} = -2dBm "10" ⇒ P_{out} = 4dBm "11" ⇒ P_{out} = 10dBm	2
12-13	**µP-external clock frequency output**	$f_{\mu P\_clk}$	"00" ⇒ µP system clock = $f_{X\text{-}tal}$ MHz "01" ⇒ µP system clock = $f_{X\text{-}tal}/2$ MHz "10" ⇒ µP system clock = $f_{X\text{-}tal}/4$ MHz "11" ⇒ µP system clock = $f_{X\text{-}tal}/8$ MHz	2
Total configuration data package size				14

Table 6. nRF903 Configuration word

Channel placement for the three available frequency bands is shown in Table 7. Allowed transmission duty-cycle is shown in brackets. Channels not compliant with FCC/ETSI regulations (as of datasheet revision date) are shown shaded.

Channel #	Frequency band		
	433.05MHz - 434.79MHz [1)]	**868MHz - 870MHz [2)]**	**902MHz - 928MHz [3)]**
0	433.1904 (up to 100% / <10%)	868.1856 (<1%)	902.1696 (100%)
1	433.3440 (up to 100% / <10%)	868.3392 (<1%)	902.3232 (100%)
2	433.4976 (up to 100% / <10%)	868.4928 (<1%)	902.4768 (100%)
3	433.6512 (up to 100% / <10%)	-	902.6304 (100%)
4	433.8048 (up to 100% / <10%)	868.8000 (<0.1%)	902.7840 (100%)
5	433.9584 (up to 100% / <10%)	868.9536 (<0.1%)	902.9376 (100%)
6	434.1120 (up to 100% / <10%)	869.1072 (<0.1%)	903.0912 (100%)
7	434.2656 (up to 100% / <10%)	-	903.2448 (100%)
8	434.4192 (up to 100% / <10%)	-	903.3984 (100%)
9	434.5728 (up to 100% / <10%)	-	903.5520 (100%)
10	-	-	903.7056 (100%)
11	-	869.8752 (100%)	903.8592 (100%)
12	-	-	904.0128 (100%)
...	-	-	...
168	-	-	927.9744 (100%)

1): European regulatory restrictions. 100% TX-duty cycle is allowed for applications with <0dBm e.r.p. 10% is allowed for applications up to 10dBm e.r.p.
2): European regulatory restrictions
3): US regulatory restrictions. 100% TX-duty cycle is allowed for applications with <-1.25dBm e.r.p. Refer to FCC CFR47, part 15 for frequency hopping and spread spectrum applications

Table 7. Channel placement for nRF903

Output power is set by bit 10 and 11 in the configuration word (ref. Table 6).
4 settings are available; 10dBm, 4dBm, -2dBm and -8dBm.

Figure 5 shows the total chip DC current consumption in transmit-mode plotted as a function of power level setting and frequency band. Antenna matching according to recommendations is assumed.

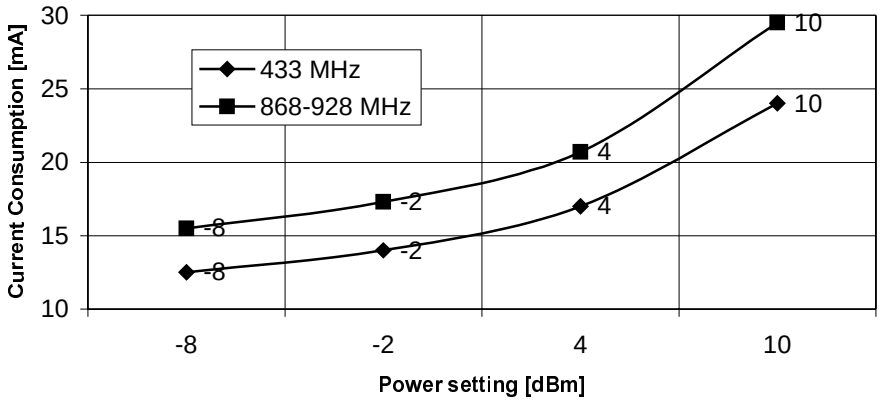


Figure 5. Total current consumption vs. power setting (typical values)

Transceiver parameters are clocked into the data shift register in the internal configuration unit by using the three-pin serial interface consisting of CS, CFG_CLK and CFG_DATA.
Chip select (CS) is used to enable the transceiver configuration mode. Figure 6 illustrates the serial interface block diagram.

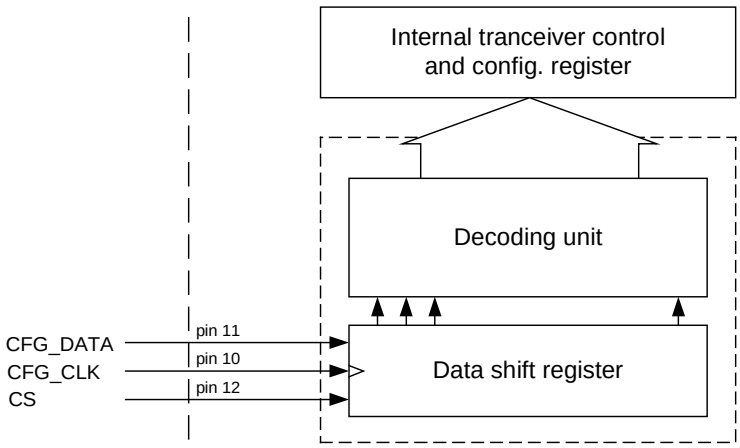


Figure 6. Serial Pheripheral Interface (SPI) for chip configuration

During configuration, CS is set high and the configuration word is clocked in with the MSB first. After the configuration word has been clocked into the shift register, CS is set low and the new configuration setup is initialised.

Timing diagram is shown in Figure 7. CFG_DATA bitrate may not exceed 1Mbit/s.

Once configured, device behaviour is set by the external signals TXEN, PWR_DWN, STBY and DATA (DATA is an input pin in transmit-mode, output in receive-mode).

Configuration may be performed in all modes except standby and power down mode.

Register content is still valid after power down and standby mode operation. Configuration data is lost only when supply voltage has been removed.

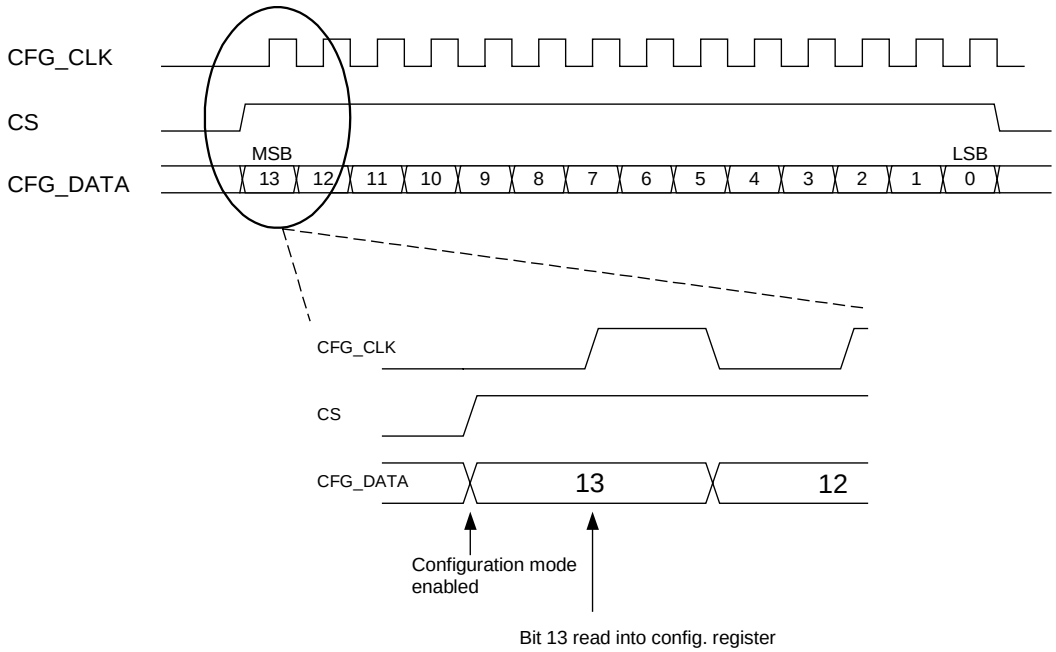


Figure 7. Timing diagram for chip configuration

Test mode

A pre-programmed channel (868.1856MHz) is available without using the SPI-configuration procedure. While in test mode (ref. Table 8.), the 868.1856MHz channel is activated with maximum power setting and an output clock frequency of 1.3824MHz. This feature has been included to ease debugging of micro-controller software and to allow measurements of RF-performance without use of SPI configuration software.

nRF903 operating mode	STBY	PWR_DWN	TXEN	CS
Test mode - receive: SPI-unit override, 868MHz, Channel #0, 1.3824MHz output clock frequency	0→1	1	0	1
Test mode - transmit: SPI-unit override, 868MHz, Channel #0, 10dBm output power, 1.3824MHz output clock frequency	0→1	1	1	1

Table 8. nRF903 testmodes

Operation mode summary

nRF903 modes	Inputs						Bidir	Outputs	
	STBY	PWR_DWN	TXEN	CS	CFG_CLK	CFG_DATA	DATA	C_SENSE	CLK_OUT
Receive (RX)	0	0	0	0	X	X	DOUT	C_SENSE	CLK_OUT [2)]
Transmit (TX)	0	0	1	0	X	X	DIN	0	CLK_OUT [2)]
Standby	1	0	0	0	X	X	HiZ	0	CLK_OUT [2)]
Power down	0	1	X	X	X	X	HiZ	0	0
Configuration mode [1)]	0	0	0	1	CFG_CLK	CFG_DATA	DOUT	C_SENSE	CLK_OUT [2)]
Configuration mode [1)]	0	0	1	1	CFG_CLK	CFG_DATA	DIN	0	CLK_OUT [2)]
Test mode RX	0→1	1	0	1	X	X	DOUT	C_SENSE	CLK_OUT [3)]
Test mode TX	0→1	1	1	1	X	X	DIN	0	CLK_OUT [3)]

1): Configuration mode can be entered from RX or TX. Old programming is maintained during program sequence, new content of configuration register is loaded at the negative edge of CS.
2): Clock frequency set by configuration register
3): Clock frequency = 1.3824MHz

Table 9. Summary of nRF903 operation modes

Definitions:

0/1:	Pin (must be/is) forced high or low
X:	Don't care
HiZ:	High impedance.
Signal name :	Pin is functional
0→1 :	Transition from low to high

Baseband DATA encoding

A UART is recommended for handling baseband data.

When transmitting wireless data, information should be divided into separate data packages. Each package usually contains preamble, address, data-payload and a checksum. Please refer to Application note nAN400-07, *'nRF Radio Protocol Guidelines'* for details.

Always aim to obtain zero DC-level (equal number of logic '0's and '1's) in the transmitted data packages. Long sequences without transitions should be avoided.

If the user allows efficient scrambling or biphase (Manchester) encoding of data, startup- and switching times may be lowered at the expense of increased data redundancy. Generally, a system with short packages and low transmission duty-cycle will benefit from a lower overall energy consumption per package even if biphase encoding is used. Note that chosen data encoding protocol influence on the choice of PLL loop filter (refer to the *PLL loop filter* chapter p. 18 and the *Timing information* chapter p. 14).

The preamble is actually a training sequence for the demodulator in the receiver. The purpose of the preamble is to retrieve the correct DC level of the modulation signal before the address and data bits are demodulated. In addition, the UART must also be synchronised to the recieved datastream. To obtain synchronisation of the UART, a sequence that locates the start and stop bits uniquely must be transmitted before the address and data bits.

The preamble sequence that gives the most rapid settling in the nRF903 demodulator is a repeated '0011' sequence at 76.8kbit/s with a total length of 40 bits.

However, if a microcontroller with a UART is used, the receiving UART will not be able to locate what is the start and stop bits in this sequence. The preamble data should therefore be modified to the following sequence: '0xCC 0xCC 0xCC 0xCC 0xF0' i.e. four bytes of '11001100' followed by '11110000'.
The F0-byte makes it possible for the UART to locate the correct position of the start and stop bits (see Figure 8). Please note that the data bits in the figure have been reversed compared to what is specified above. This is due to the fact that UARTs normally reverse data before adding startbit (0) and stopbit (1) to each byte.

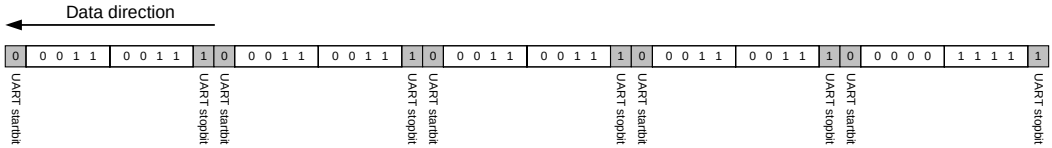


Figure 8. Recommended nRF903 preamble

Timing information

Table 10 contains the timing information for the nRF903 transceiver.

The listed values in Table 10 assume the device has been configured. Configuration time is equal to ($14 \cdot 1/f_{CFG\_DATA}$). This time must be added if the device is configured when the operation mode changes below are initiated.

Mode/operation			No data encoding	Biphase encoding of data	Unit
Power down[1)]	→	Standby	0.8	0.8	ms
Transmit Ch. #X	→	Transmit Ch. #X±1	2.6	1.0	ms
	→	Transmit Ch. #X±2	3.1	1.3	ms
	→	Transmit Ch. #X±10	5.0	2.0	ms
Receive Ch. #X	→	Receive Ch. #X±1	2.6	1.0	ms
	→	Receive Ch. #X±2	3.1	1.3	ms
	→	Receive Ch. #X±10	5.0	2.1	ms
Transmit → Receive			6.0	2.1	ms
Receive	→	Transmit	6.0	2.0	ms
Standby	→	Transmit	7.9	4.0	ms
Power down*	→	Transmit	8.6	4.7	ms
Standby	→	Receive	8.9	5.5	ms
Power down*	→	Receive	9.6	6.2	ms
f_{CFG_DATA}			<1	<1	MHz

1): Same as applying power (VDD) when set to Receive/Transmit/Standby-mode

Table 10. Timing data for nRF903

If the user allows efficient scrambling or biphase (Manchester) encoding of data, startup and switching times may be lowered at the expense of increased data redundancy. Generally, a system with short packages and low transmission duty-cycle will benefit from a lower overall energy consumption pr. package even if biphase encoding is used (refer to the *PLL loop filter* chapter p. 18 and the *Baseband DATA encoding* chapter p. 13).

Mode/operation	Definition
Power down → Standby:	The time required until a stable reference clock signal is available at the CLK_OUT-pin when the device is set from power down mode to standby mode.
Transmit Ch. #X → Transmit Ch. #X±Y	The time required for a correct transmitted data spectrum to appear at the ANT1- and ANT2-pins when the device is shifted Y-channels up (or down) to a new channel in transmit mode. No data transitions may occur during this time interval.
Receive Ch. #X → Receive Ch. #X±Y	The time required for the receiver to be able to demodulate data when the device is shifted Y-channels up (or down) to a new channel in receive mode.
Transmit → Receive	The time required for the receiver to be able to demodulate data when the device is set from transmit mode to receive mode.
Receive → Transmit	The time required for a correct transmitted data spectrum to appear at the ANT1- and ANT2-pins when the device is set from receive mode to transmit mode. No data transitions may occur during this time interval.
Power down (Standby) → Transmit	The time required for a correct transmitted data spectrum to appear at the ANT1- and ANT2-pins when the device is set from power down (standby) mode to transmit mode. No data transitions may occur during this time interval.
Power down (Standby) → Receive	The time required for the receiver to be able to demodulate data when the device is set from power down (standby) mode to receive mode.
f_{CFG_DATA}	Configuration clock frequency. May be chosen arbitrarily.

Table 11. Timing definitions

EXTERNAL COMPONENTS

Below the specifications for the nRF903 external components are listed. It should be noted that the part numbers and vendors listed are suggestions only, and that other vendors may offer compatible components. Availability, price and delivery times may differ for the different vendors.

VCO inductors (L_1, L_2)
Important notice: The VCO inductor value decides the PLL-tuning range and must be according to specifications in order to guarantee functionality for all channels in a given band (of utmost importance for the 902MHz to 928MHz range). *Always make sure that the inductors supplied by your vendor yield the correct loopfilter voltage for your layout.* Loopfilter voltage is measured at the center frequency in the band of operation (VDD=3V, room temperature). Correct loopfilter voltages are;

915MHz: 1.8V ±0.2V
868MHz: 1.8V ±0.2V
433MHz: 2.2V ±0.2V

Verify that your secondary inductor source is within the same loopfilter voltage range, unless product functionality might suffer.

Operated in the 433 MHz range, $L_1 = L_2 = 91$nH, tolerance ±2%, Q > 40 @ 217MHz. Table 12 lists inductors (0603) suitable for use with nRF903.

Vendors	WWW address	Part. no., 91 nH inductors, 0603 size
muRata	www.murata.com	LQW18AN91NG00

Table 12. Vendors and part no. for suitable inductors (433MHz operation).

Operated in the 868 MHz range, $L_1 = L_2 = 22$nH, tolerance ±2%, Q > 40 @ 434MHz. Table 13 lists inductors (0603) suitable for use with nRF903.

Vendors	WWW address	Part. no., 22 nH inductors, 0603 size
Coilcraft	www.coilcraft.com	0603CS-22NXGBC
muRata	www.murata.com	LQW18AN22NG00
Pulse	www.pulseeng.com	PE-0603CD220GTT

Table 13. Vendors and part no. for suitable inductors (868MHz operation).

Operated in the 915 MHz range, $L_1 = L_2 = 18$nH, tolerance ±2%, Q > 40 @ 460MHz. Table 14 lists inductors (0603) suitable for use with nRF903.

Vendors	WWW address	Part. no., 18 nH inductors, 0603 size
Coilcraft	www.coilcraft.com	0603CS-18NXGBC
muRata	www.murata.com	LQW18AN18NG00
Pulse	www.pulseeng.com	PE-0603CD180GTT

Table 14. Vendors and part no. for suitable inductors (915MHz operation).

11.0592MHz Crystal reference

When specifying a crystal, keep in mind that the frequency deviation requirement is ±20ppm for 868/915MHz operation and ±40ppm for 433MHz operation. This accounts for both frequency tolerance (Δf/f) and temperature variations in the crystal frequency.
Example: For a 868MHz system, a crystal frequency tolerance (Δf/f) of ±15ppm, leaves ±5ppm for drift due to temperature variations.

As temperature characteristics are closely related to crystal cost, it is advisable not to exaggerate the crystal specification. Note that it is *the maximum relative difference between the receiver and transmitter reference frequency* that set the crystal oscillator requirement. If the transmitter and receiver will not be operating at opposite temperature extremes at the same time (maximum difference), the requirements towards temperature characteristics may be relaxed accordingly.

Note that frequency difference between the transmitter and receiver will result in sensitivity loss, which is proportional to the total frequency offset. Figure 9 shows sensitivity as a function of total frequency offset.

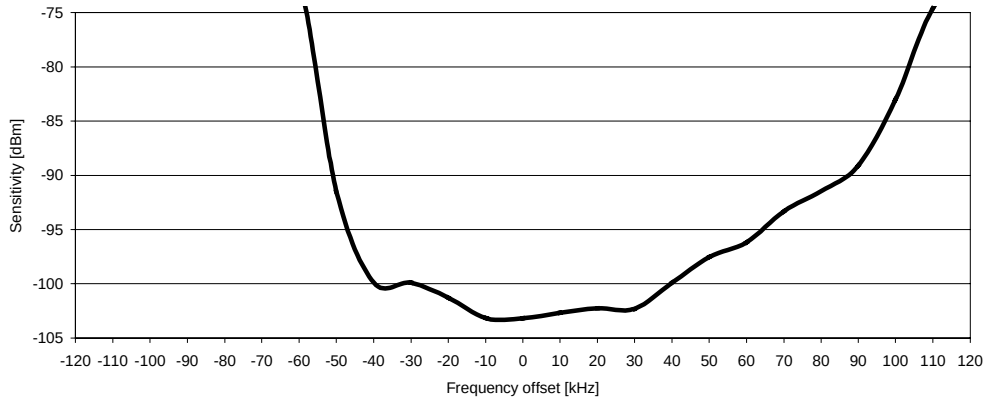


Figure 9. Sensitivity vs. total TX/RX frequency offset (Typical)

The key parameters for the nRF903 crystal reference are as follows:

f_c=11.0592MHz
ESR_{max}=60Ω
$C_{0,max}$=7pF
C_L=12pF (nRF903 internal load is 11.5pF ± 8%. Application layout on page 29 adds approx. 0.5pF load)

Vendors	WWW address	Part. no., SMD-package
Chequers electronic	www.chequers-electronic.com	CQ11.0592 / SMD0705
Epson	www.epson-electronics.de	MA-406H SA-315H / 315HZ
Raltron	www.raltron.com	H10S
Golledge	www.golledge.com	GSX-2
Fox Electronics	www.foxonline.com	FD
Jauch	www.jauch.de	JXS 75

Table 15. Vendors and part no. for suitable 11.0592MHz crystals

10.7MHz Ceramic filter

The external 1st IF-filter is a piezoelectric ceramic filter with 330Ω input/output impedance. Center frequency should be positioned at 10.7MHz, and bandwidth should not be less than the channel spacing. 180kHz is a suitable bandwidth. Note that variations in absolute center frequency and bandwidth may differ for different vendors.

Vendors	WWW address	Part. no. 10.7MHz filter, 180kHz BW
Chequers electronic	www.chequers-electronic.com	LTCV10.7MS3A10-A (SMD-package)
muRata	www.murata.com	SFECV10.7MS3S-A-TC (SMD-package)
TDK	www.tdk.co.jp	FFE1070MS (Through-mount)

Table 16. Vendors and part no. for suitable 10.7MHz ceramic filters.

This filter may be replaced with a 10nF capacitor between the FILT1- and FILT2-pins, at the expense of sensitivity (approx. 3dB degradation), blocking performance and adjacent channel selectivity. In this case, only the internal (second) IF-filter is used. The image frequency resulting from the second mixing will then appear in the baseband. This image is centered at 691kHz above the signal of interest.

PLL loop filter

The synthesiser loopfilter is an external, single-ended third order lag-lead filter as shown in Figure 10.

The startup and switching times of the transceiver is dependent on the loopfilter bandwidth. A high loopfilter bandwidth reduces switching time, but necessitates efficient scrambling or biphase (Manchester) encoding of data.
If a filter with lower bandwidth is chosen, normal data may be transmitted without scrambling requirements at the expense of longer switching times.

The recommended filter component values are listed in Table 17.

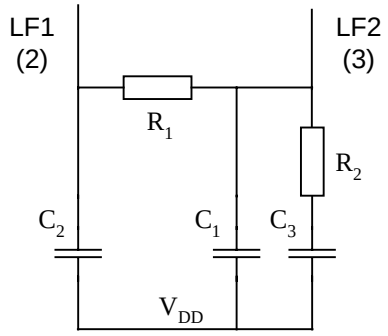


Figure 10. Loopfilter configuration

Data encoding	C_1 [pF]	C_2 [pF]	C_3 [nF]	R_1 [kΩ]	R_2 [kΩ]
No encoding	470 (±5%)	220 (±5%)	6.8 (±5%)	150 (±1%)	150 (±1%)
Biphase/Manchester encoding	27 (±5%)	12 (±5%)	0.47 (±5%)	330 (±1%)	330 (±1%)

Table 17. Loopfilter component values and tolerances

Antenna input/output

The ANT1 and ANT2 pins provide RF input to the LNA (Low Noise Amplifier) when nRF903 is in receive mode, and RF output from the PA (Power Amplifier) when nRF903 is in transmit mode. The antenna connection to nRF903 is differential and the recommended load impedance at the antenna port is 300Ω.

Figure 19 shows a typical application schematic with a differential loop antenna on a Printed Circuit Board (PCB). The PA output stage consists of two open collector transistors in a differential pair configuration. VDD to the PA must be supplied through the collector load. When connecting a differential loop antenna to the ANT1/ANT2 pins, VDD should be supplied through the centre of the loop antenna as shown in Figure 19.

A single ended antenna or 50Ω test instrument may be connected to nRF903 by using a differential to single ended matching network (BALUN) as shown in Figure 11.

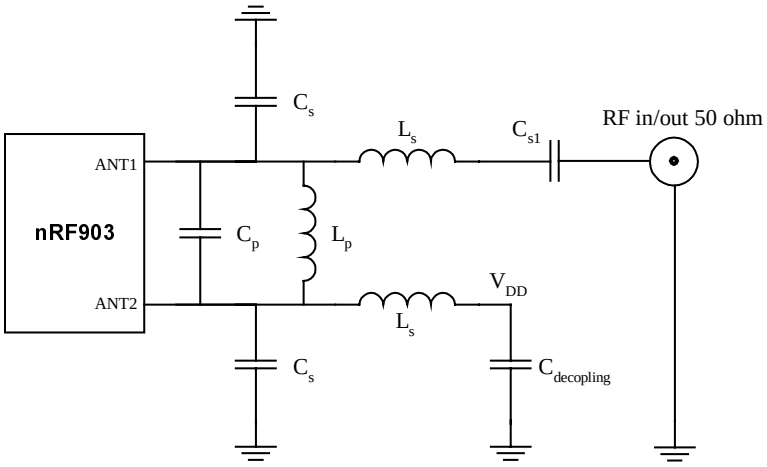


Figure 11. Connecting the nRF903 to a single ended antenna by using a differential to single-ended matching network.

The series-inductors L_s in Figure 11, need to have a Self Resonance Frequency (SRF) well above the transmit/receive frequency to be effective. Suitable component values are listed in Table 18. Gerber layout files of the matching network is available at **www.nvlsi.no**. Component tolerances are ±2% for the inductors, ±5% for $C_{decoupling}$ and C_{s1}, and ±0.1pF for C_p and C_s.

Frequency band [MHz]	L_p [nH]	L_s [nH]	C_p [pF]	C_s [pF]	C_{s1} [pF]	$C_{decoupling}$ [pF]
433.92 ± 0.87	22	39	1.8	8.2	6.8	100
869 ± 1 915 ± 13	12	12	-	3.9	4.7	33

Table 18. Single-ended matching network components values for nRF903

PCB layout and decoupling guidelines

A well-designed PCB is necessary to achieve good RF performance. Keep in mind that a poor layout may lead to loss of performance, or even functionality, if due care is not taken. A fully qualified RF-layout for the nRF903 and its surrounding components, including antennas and matching networks, can be downloaded from **www.nvlsi.no**.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF903 DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors, see Table 19. It is preferable to mount a large surface mount capacitor (e.g. 4.7µF tantalum) in parallel with the smaller value capacitors. The nRF903 supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the nRF903 IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. One via hole should be used for each VSS pin.

Full swing digital data or control signals should not be routed close to the PLL loop filter components, the external VCO inductors or the power supply lines.

The placement of the VCO inductors is important. Optimum placement of the VCO inductors yields a PLL loop filter voltage in the order of 1.8 ± 0.2V for the 868/915MHz bands and 2.2 ± 0.2V for the 433MHz band. The loopfilter voltage can be measured at LF2 (pin 3). Figure 12 shows the recommended layout and inductor placement for a PCB compatible with all three frequency bands. For 868MHz operation, the inductors should be placed according to Figure 12 a., and for 433MHz and 915MHz operation as shown in Figure 12 b. Please refer to the **Important notice** section in the *External components* chapter p. 16 regarding inductor specifications. See also the *VCO inductor* chapter in the *External Components* section on the nRF™ Support Pages.

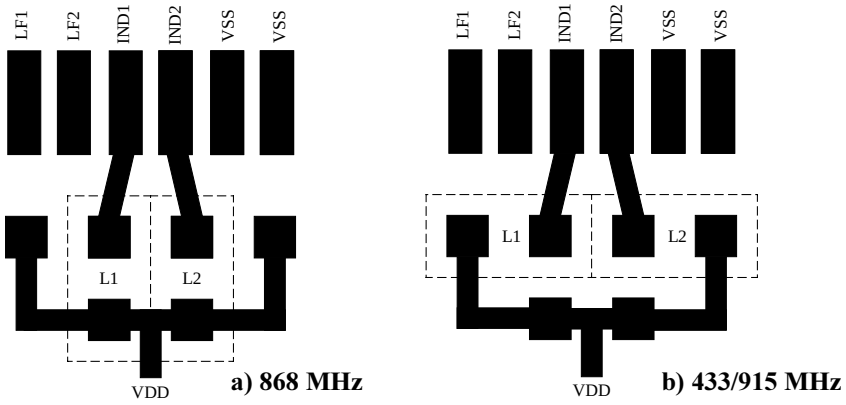


Figure 12. Inductor placement for 868MHz and 433/915MHz operation.

PERFORMANCE PARAMETERS

Data modulation

The DATA pin is the input to the digital modulator of the transmitter while in TX-mode, and demodulated data output while in RX-mode. The input signal to this pin should be standard CMOS logic levels at 76.8kbit/s datarate.

The demodulated digital output data appear at the DATA-pin at standard CMOS logic levels.

nRF903 uses GFSK modulation of data for optimum modulation bandwidth efficiency. This type of modulation is an enhanced version of FSK in which each of the two logic levels corresponds to a frequency value;

$$DATA_{FSK} = \text{“1”} \rightarrow f_{'1'} = f_{centre} + \Delta f$$
$$DATA_{FSK} = \text{“0”} \rightarrow f_{'0'} = f_{centre} - \Delta f$$

In Gaussian Frequency Shift Keying (GFSK), the data is filtered through a gaussian filter before modulating the carrier. Figure 13 shows the general principle. This results in a narrower power spectrum of the modulated signal, which in turn allows a higher bitrate to be transferred in the same channel bandwidth. This is often referred to as bandwidth efficiency, and is given in bits/Hz. The nRF903 bandwidth efficiency is thus 0.5 bit/Hz. Figure 14 shows the difference between the nRF903 GFSK output spectrum and a comparable FSK-spectrum at 76.8kbit/s. It should also be noted that a GFSK system *emits less noise in the neighbouring channels* and thus reduces the risk of destructive interference in a system with multiple nodes.

Gaussian Minimum Shift Keying (GMSK) is the term used for a GFSK signal where the bitrate is four times the frequency deviation.

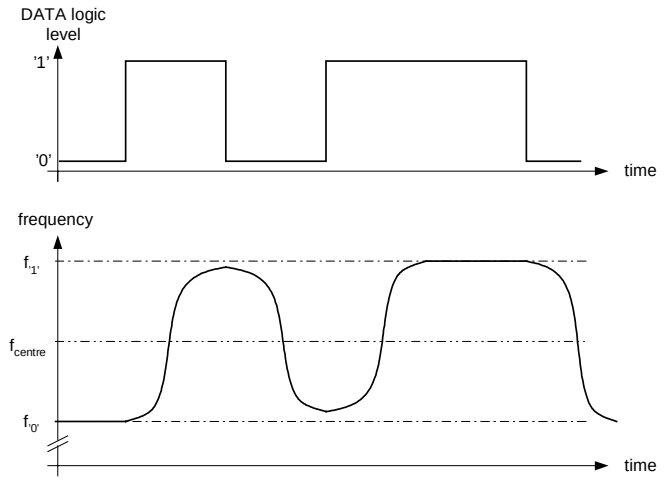


Figure 13. Principle of Gaussian filtering of transmitted data

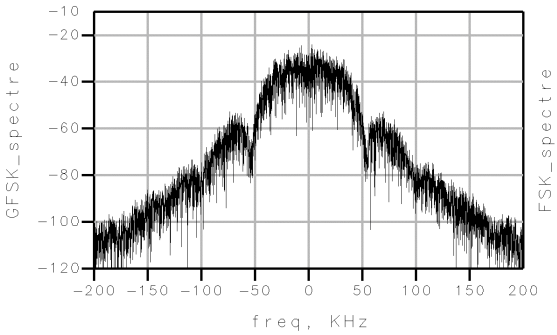


Figure 14 a). Transmitted nRF903 spectrum
(Δf = 23kHz, BR = 76.8kbit/s, BT_{GFSK} = 0.5)

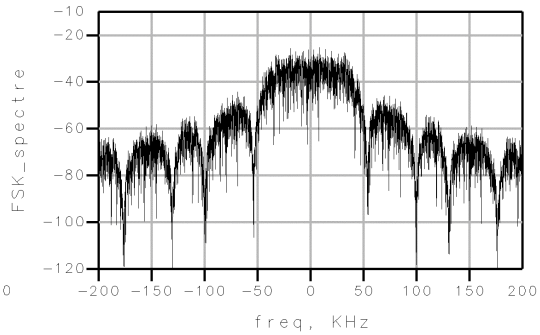


Figure 14 b). Comparable FSK spectrum
(Δf = 23kHz, BR = 76.8kbit/s)

Mirror image attenuation

A cost-saving feature of the nRF903 transceiver is on-chip mirror image cancellation. All heterodyne receivers have a mirror image frequency for a given channel, which may cause in-band interference.

The nRF903 mirror image frequency is always positioned 21.4272MHz below the received channel, regardless of channel number or frequency band. As the nRF903 mirror image is attenuated by use of an on-chip quadrature cancellation technique, a costly external SAW/crystal-filter may be avoided.

Typical attenuation of the mirror image frequency is 30dB.

Blocking

Blocking performance is the term used to describe the receivers ability to function under the influence of a strong interfering RF-signal. Figure 15 a. and b. show the nRF903 blocking characteristic without antenna or SAW-/High-Q filtering (Evaluation board measurement). A signal present 1MHz from the receiving channel may have approx. 50dB higher power than the received signal before communication is lost (receiver operating at sensitivity limit +3dB).

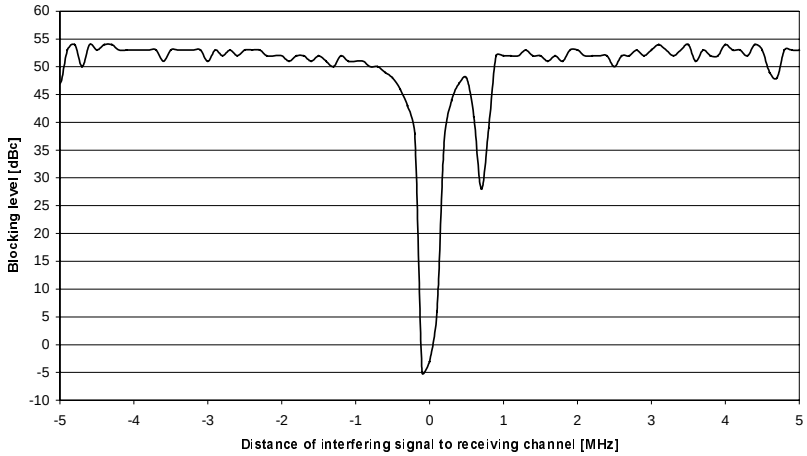


Figure 15 a). nRF903 narrowband blocking characteristic at 868MHz (typical)

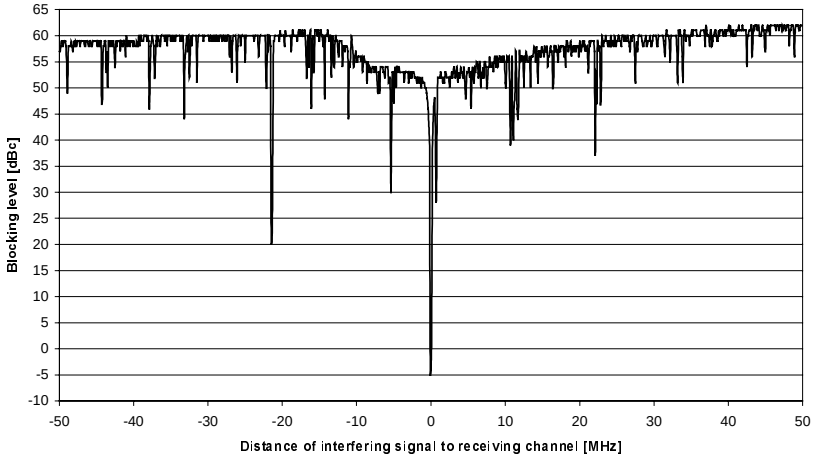


Figure 15 b). nRF903 wideband blocking characteristic at 868MHz (typical)

Adjacent channel selectivity (ACS)

nRF903 is a true multi-channel transceiver, enabling simultaneous operation of multiple nRF903 devices in the same environment. This is possible due to high-Q filtering of the received channel. The IF-filters attenuate the signal power of the neighbouring channels, thus significantly reducing the risk of jamming and loss of communication due to nearby traffic. Channel filtering is performed by the external 10.7MHz filter combined with an internal band-pass filter.

The adjacent channel selectivity of a receiver is defined in ETSI EN 300-220-1 as the ability to demodulate a received signal at the sensitivity limit, with the presence of a sine component centred in the adjacent channel (see Figure 16). The received power level of the neighbouring channels, depends on the transmitted power and the distance to the receiver. Note that the ETSI definition is merely meant as a comparative figure. The *system* ACS is usually lower, as the adjacent channel is not likely to be a sine component, but a modulated spectrum. As the nRF903 is a GFSK-device, the transmitted adjacent channel power is approx. 25dB *less* than for a comparable FSK system with the same frequency deviation and datarate, greatly reducing the risk of destructive interference (Refer to Figure 14 in the *DATA modulation* chapter p. 22). Figure 17 shows typical ACS for the 4 closest channels as a function of input power.

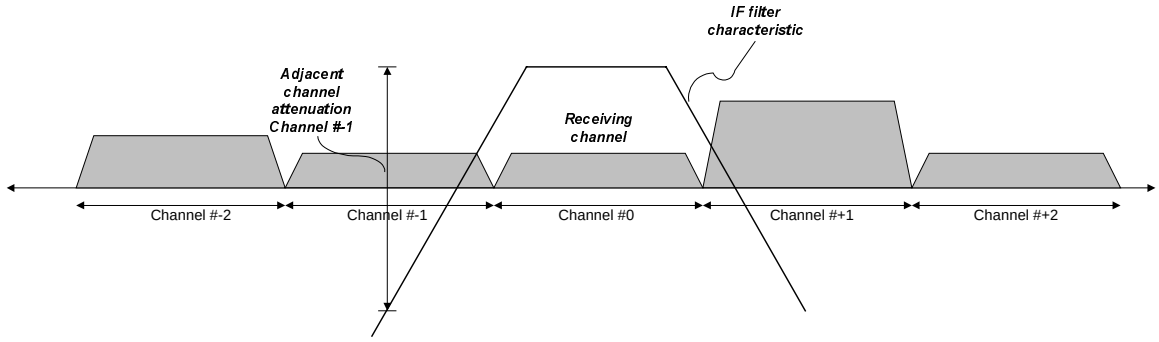


Figure 16. Adjacent channel power attenuation obtained due to IF-filter passband characteristic (ETSI-def.)

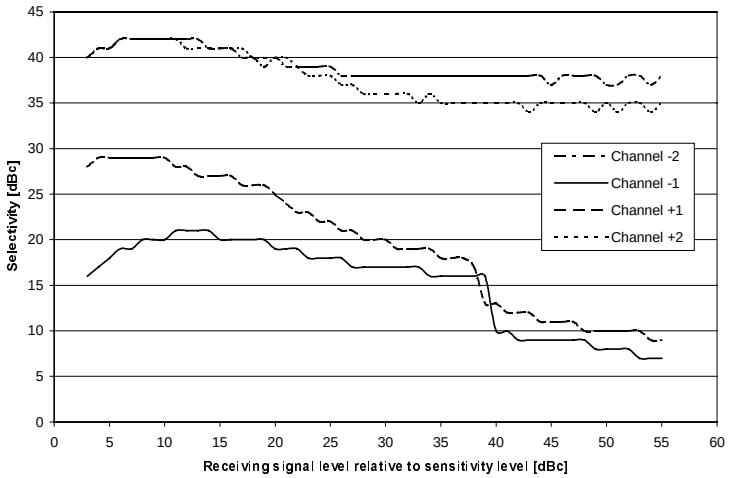


Figure 17. Adjacent channel selectivity as function of channel spacing and input power level (typical)

APPLICATION EXAMPLE, 868MHz

Configuration:

A 868MHz system module is to be designed. The operating channel of the unit is channel #5. The transceiver units are operating within a small confined area. System channel organisation and ETSI frequency allocations are shown in Figure 18.

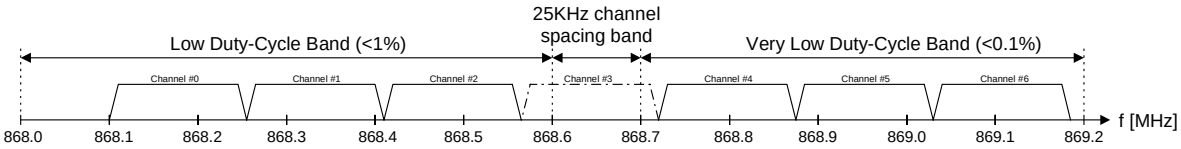


Figure 18. 868MHz LPRD-band, channel organisation

The same crystal is shared by the micro-controller and transceiver. When applying power, nRF903 is set to Standby-mode (STBY = '1', PWR_DWN = '0'), a 11.0592MHz system clock is then available to the micro-controller at the CLK_OUT-pin after 0.8 ms (see Table 10).

The micro-controller then sets the transceiver to normal operation, receive mode (STBY = '0', PWR_DWN = '0', TXEN = '0') for configuration (Receive mode is chosen during configuration in order to avoid unintentional transmission at an unwanted frequency).

The configuration word is calculated as follows (refer to Table 6);

1. Setting frequency band:

   The system operates in the 868MHz LPRD-band, and FB is thus set to $\underline{01}_b$.

2. Calculating channel frequency location:

   The center frequency of Channel #5 is 868.9536MHz.

   CH is found by solving for CH in the equation given in Table 6;

   $$CH = (f_{centre\_868MHz} - 868.1856 \cdot 10^6) / 153.6 \cdot 10^3$$

   CH=5 ($\underline{00000101}_b$)

3. Setting output power

   The operational range is limited, and the output power is therefore reduced to a minimum in order to minimise current consumption in transmit mode. P_{out} is set to 0 ($\underline{00}_b$), resulting in an output power of -8dBm.

4. Setting the external microprocessor frequency

   A microprocessor that can perform all system functions at a system clock frequency of at least 4MHz is used. $f_{\mu P\_clk}$ is therefore set to $\underline{01}_b$, resulting in a clock frequency of 5.5296MHz.

   The resulting 14-bit configuration word is then;
   ($\underline{01\ 00\ 00000101\ 01}_b$) where MSB is the leftmost bit.

The configuration word is clocked in according to Figure 7. On the falling edge of CS, the internal decoding unit sets the frequency synthesiser to the wanted frequency. 8.9/5.5ms must be allowed for the synthesiser to stabilise before data may be demodulated (see Table 10).

APPLICATION SCHEMATIC, 868MHz

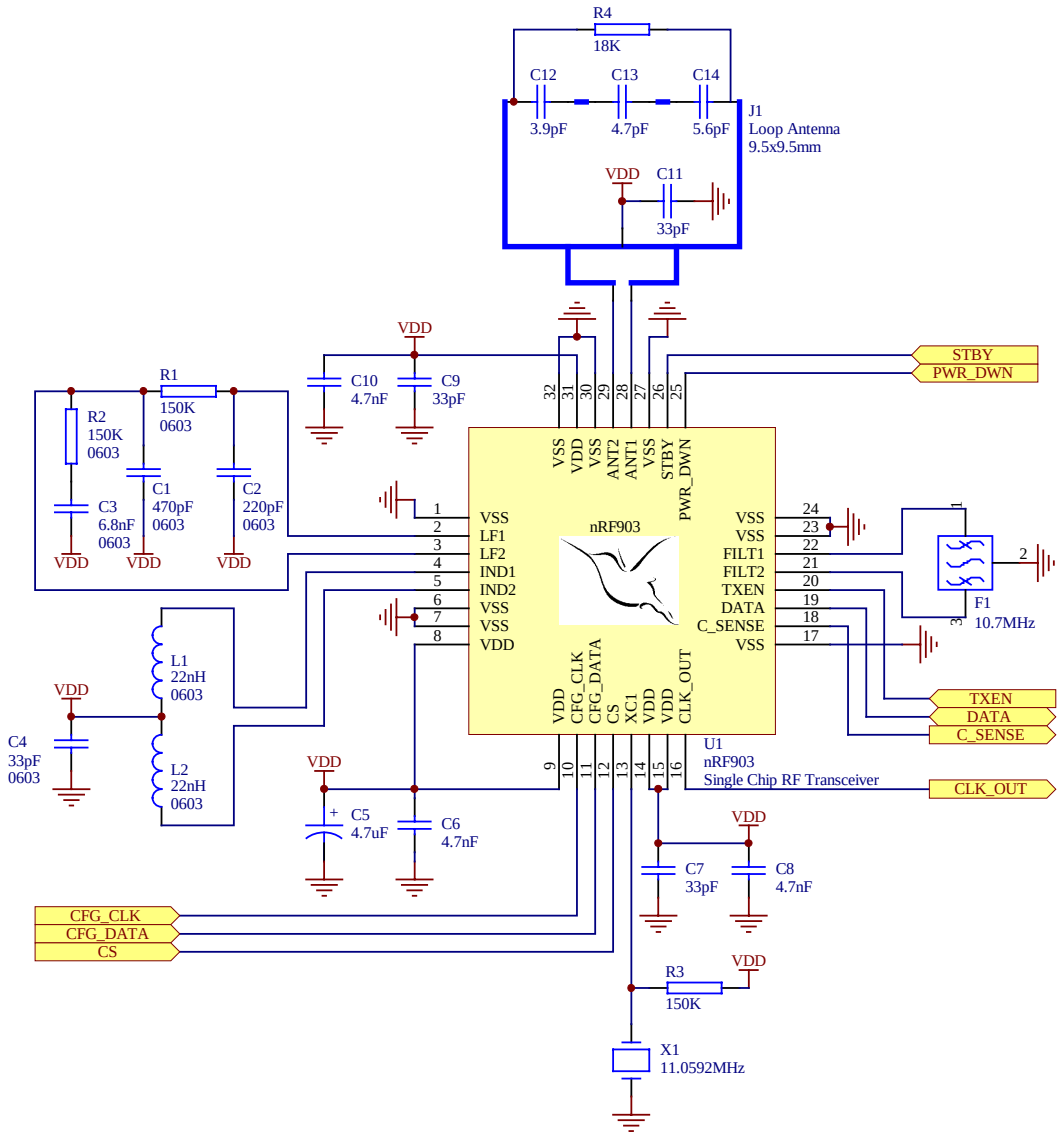


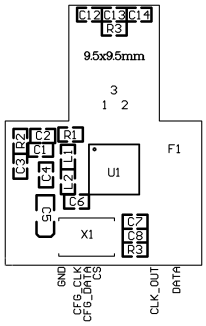
Figure 19. nRF903 application schematic (868MHz).

Component	Description	Size	Value	Tol.	Units
C1	NP0 ceramic chip capacitor, (PLL loop filter)	0603	470	±5%	pF
C2	NP0 ceramic chip capacitor, (PLL loop filter)	0603	220	±5%	pF
C3	X7R ceramic chip capacitor, (PLL loop filter)	0603	6.8	±5%	nF
C4	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C5	Tantalum chip capacitor, (Supply decoupling)	3216	4.7	±20%	µF
C6	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C7	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C8	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C9	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C10	X7R ceramic chip capacitor, (Supply decoupling)	0603	4.7	±10%	nF
C11	NP0 ceramic chip capacitor, (Supply decoupling)	0603	33	±5%	pF
C12	NP0 ceramic chip capacitor, (Antenna tuning)	0603	3.9	±0.1	pF
C13	NP0 ceramic chip capacitor, (Antenna tuning)	0603	4.7	±0.1	pF
C14	NP0 ceramic chip capacitor, (Antenna tuning)	0603	5.6	±0.1	pF
L1	VCO inductor (see *External components* section)	0603	22	±2%	nH
L2	VCO inductor (see *External components* section)	0603	22	±2%	nH
R1	0.1W chip resistor, (PLL loop filter)	0603	150	±1%	kΩ
R2	0.1W chip resistor, (PLL loop filter)	0603	150	±1%	kΩ
R3	0.1W chip resistor, (Crystal oscillator bias)	0603	150	±1%	kΩ
R4	0.1W chip resistor, (Antenna Q reduction)	0603	18	±1%	kΩ
F1	Ceramic filter (see *External components* section)	-	10.7		MHz
X1	Crystal (see *External components* section)	-	11.0592		MHz

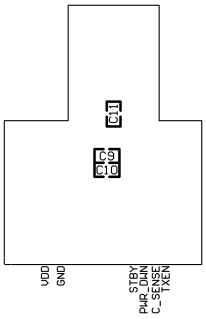
Table 19. Recommended External Components (868MHz).

PCB layout example

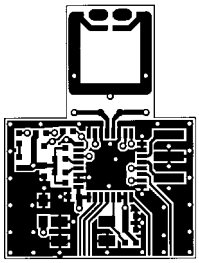
Figure 20 shows a PCB layout example for the application schematic in Figure 19. A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane beneath the antenna.



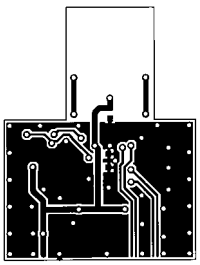
a) Top silk screen



b) Bottom silk screen



c) Top view



d) Bottom view

Figure 20. PCB layout example for nRF903 with loop antenna (868MHz)

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 20. Definitions**.**

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Product specification: Revision Date: 10.12.2002.

Datasheet order code: 101202nRF903

YOUR NOTES

Nordic VLSI - World Wide Distributors

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