Nordic VLSI ASA

Single chip 433MHz RF Transceiver **nRF0433**

FEATURES

- True single chip FSK transceiver
- On chip UHF synthesiser, 4MHz crystal reference
- 433MHz ISM band operation
- Few external components required
- Up to 10mW transmit power
- No setup/configuration

APPLICATIONS

- Alarm and Security Systems
- Home Automation
- Remote Control
- Surveillance
- Automotive
- Telemetry
- Toys
- Wireless Communication

GENERAL DESCRIPTION

nRF0433 is a true single chip UHF transceiver designed to operate in the 433MHz ISM (Industrial, Scientific and Medical) frequency band. It features Frequency Shift Keying (FSK) modulation and demodulation capability. nRF0433 operates at bit rates up to 9600 bit/s. Transmit power can be adjusted to a maximum of 10dBm. It features a differential antenna interface and an internal transmit/receive switch. nRF0433 operates from a single +5V DC supply.

As a primary application, nRF0433 is intended for design of UHF transceivers in compliance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 V1.2.1.

QUICK REFERENCE DATA

Parameter	Value	Unit
Frequency	433.936	MHz
Modulation	FSK	
Frequency deviation	±15	kHz
Max. RF output power @ 400Ω	10	dBm
Sensitivity @ 400Ω, BR=1200 bps, BER<10^{-3}	-103	dBm
Maximum baud rate	9600	bit/s
Supply voltage DC	5	V
Receive supply current	23	mA
Transmit supply current @ -2 dBm RF output power	33	mA

Table 1. nRF0433 quick reference data.

ORDERING INFORMATION

Type number	Description	Version
nRF0433-IC	20 pin SOIC	i-2
nRF0433-EVKIT	Evaluation kit with nRF0433 IC on board	e-2

Table 2. nRF0433 ordering information.

BLOCK DIAGRAM

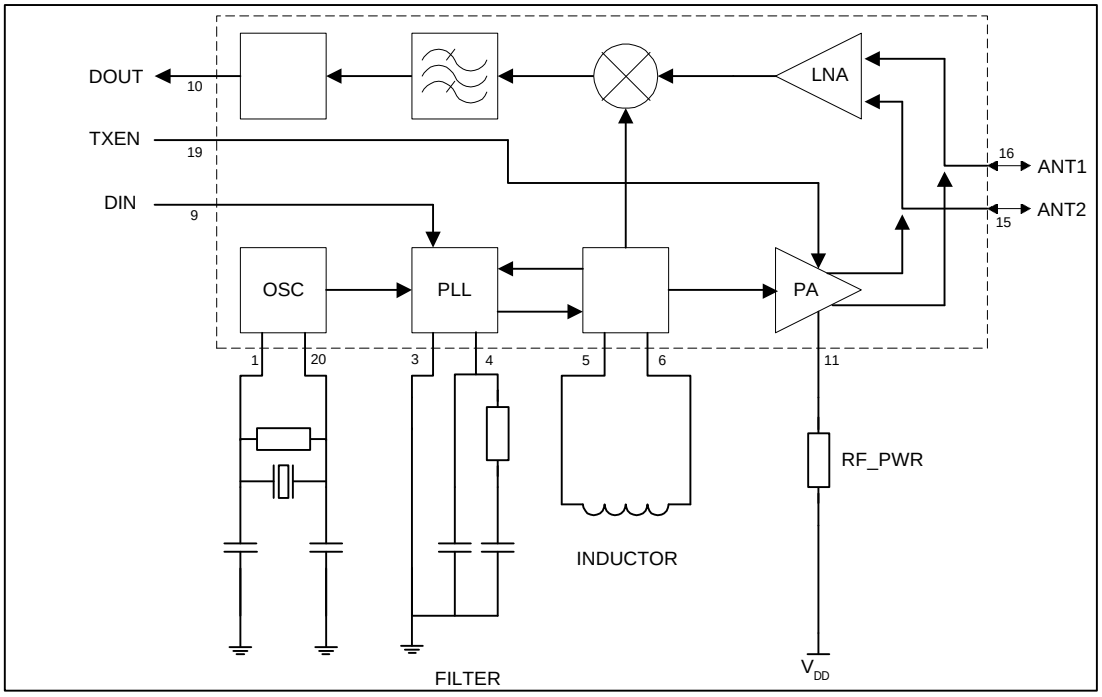


Figure 1. nRF0433 block diagram with external components.

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	XC1	Input	Crystal oscillator input
2	VDD	Power	Power supply +5V DC
3	FILT2	Input	Loop filter ground (0V)
4	FILT1	Input	Loop filter
5	VCO1	Input	External inductor for VCO
6	VCO2	Input	External inductor for VCO
7	VSS	Ground	Ground (0V)
8	VDD	Power	Power supply +5V DC
9	DIN	Input	Data input
10	DOUT	Output	Data output
11	RF_PWR	Input	Transmitter power setting
12	VSS	Ground	Ground (0V)
13	VDD	Power	Power supply +5V DC
14	VSS	Ground	Ground (0V)
15	ANT2	Input/Output	Antenna terminal
16	ANT1	Input/Output	Antenna terminal
17	VSS	Ground	Ground (0V)
18	VDD	Power	Power supply +5V DC
19	TXEN	Input	Select transmit/receive mode. TXEN = “1” ⇒ Transmit mode TXEN = “0” ⇒ Receive mode
20	XC2	Output	Crystal oscillator output

Table 3. nRF0433 pin functions.

ELECTRICAL SPECIFICATIONS

(VDD = +5V DC, VSS = 0V, f_0 = 433.936MHz, T_A= -25°C to +75°C)

Symbol	Parameter (condition)	Min.	Typ.	Max.	Units
VDD	Supply voltage DC	4.75	5	5.25	V
VSS	Ground		0		V
I_{DD}	Total current consumption Receive mode Transmit mode @ -2 dBm RF output power		 23 33		 mA mA
P_{RF}	Max. RF output power @ 400Ω load		10		dBm
V_{IH}	Logic "1" input voltage	$0.7 \cdot V_{DD}$		V_{DD}	V
V_{IL}	Logic "0" input voltage	0		$0.3 \cdot V_{DD}$	V
V_{OH}	Logic "1" output voltage (I_{OH} = - 1.0mA)	$0.7 \cdot V_{DD}$		V_{DD}	V
V_{OL}	Logic "0" output voltage (I_{OL} = 1.0mA)	0		$0.3 \cdot V_{DD}$	V
I_H	Logic "1" input current (V_I = VDD)			±20	µA
I_L	Logic "0" input current (V_I = VSS)			±20	µA
f_0	Frequency		433.936		MHz
	Modulation		FSK		
Δf	Frequency deviation		±15		kHz
f_{IF}	IF frequency		400		kHz
BW_{IF}	IF bandwidth	65		85	kHz
f_{XTAL}	Crystal frequency		4.0		MHz
	Crystal frequency stability requirement [1]			±45	ppm
	Sensitivity @ 400Ω,BR=9600 bps,BER < 10^{-3}		-103		dBm
	Baudrate			9600	bit/s
Z_I	Antenna port differential impedance		400		Ω
	Spurious emission	Compliant with EN 300-220-1 V1.2.1 [2]			

Table 4. nRF0433 electrical specifications.

[1] Maximum 5dB sensitivity degradation at temperature extremes. See also page 8.
[2] With a PCB loop antenna or a differential to single ended matching network to a 50Ω antenna.

ABSOLUTE MAXIMUM RATINGS

Supply voltages

VDD ..... - 0.3V to +6V
VSS 0V

Input voltage

V_I ..... - 0.3V to VDD + 0.3V

Output voltage

V_O ..... - 0.3V to VDD + 0.3V

Power dissipation

P_D (T_A=25°C) 250mW

Temperatures

Operating Temperature….-25°C to +85°C
Storage Temperature..- 40°C to +125°C

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic Sensitive Device
Observe Precaution for handling.

PIN ASSIGNMENT

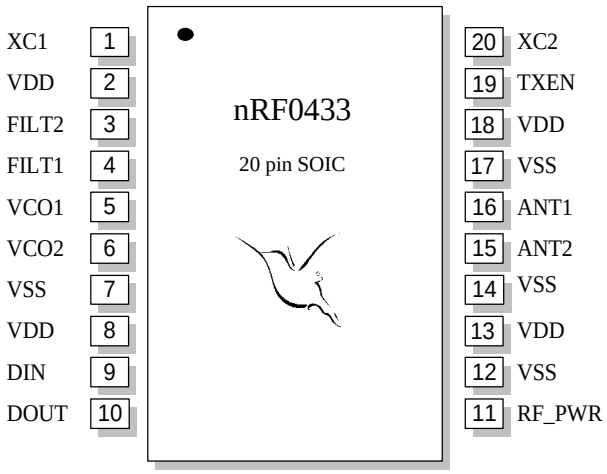
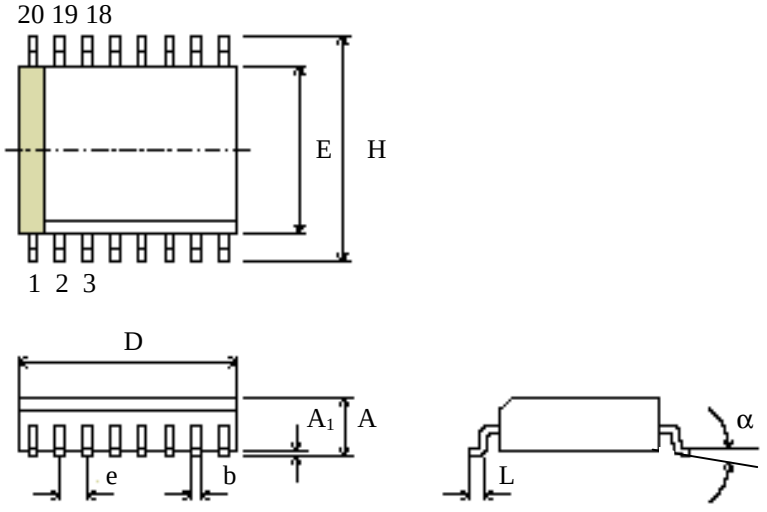


Figure 2. nRF0433 pin assignment.

PACKAGE OUTLINE

nRF0433, 20 pin SOIC. (Dimensions in mm.)



Package Type		D	E	H	A	A_1	e	b	L	Copl.	α
20 pin SOIC	**Min**	12.60	7.40	10.00	2.35	0.10	1.27	0.33	0.40		0°
(300 mil)	**Max**	13.00	7.60	10.65	2.65	0.30		0.51	1.27	0.10	8°

Figure 3. SOIC-20 Package outline.

IMPORTANT TIMING DATA

Power up time

The time from power is switched on until the synthesised frequency is stable is the power up time, t_{on}. t_{on} is 75 ms for nRF0433. Power up time can be reduced if a stable 4MHz reference signal (eg. from the driver pin of an active micro-controller) is available at the XC1 input when powering up the transceiver. In this case t_{on} is 7.5 ms. Figure 4 shows a circuit diagram of a typical application. Note that these times may vary depending on the crystal used.

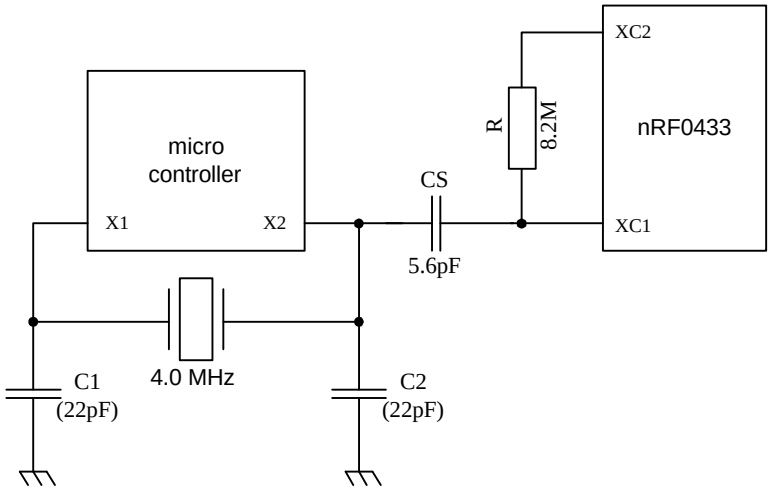


Figure 4. nRF0433 with an external reference oscillator (example).

Power up in transmit-mode

To avoid spurious emission outside the ISM-band during power-up of nRF0433, the TXEN-input must be kept low until the synthesised frequency is stable (t_{on}), see figure 5.

When enabling transmit-mode, no data should be transmitted before the TXEN-input has been high for at least 3ms (t_{data}-t_{on}).

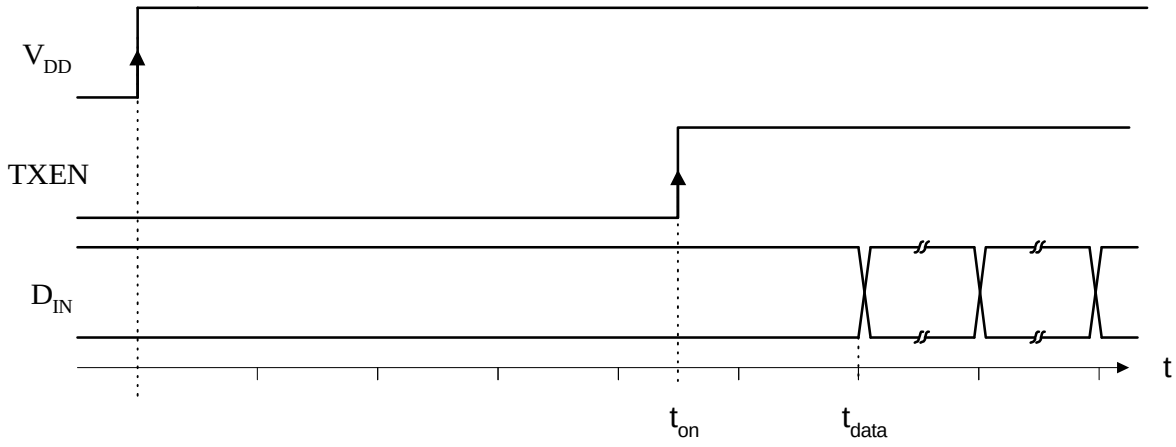


Figure 5. Power up timing diagram for nRF0433.

Power up in receive mode

During power up in receive mode, the receiver can not receive data until the VDD pins have been stable at 5V (±5%) for at least 75ms (t_{on}). If an external reference oscillator is used (figure 4), the receiver may receive data after 7.5ms.

Switching TX ↔ RX

The receiver may not receive data before the TXEN-input has been low for at least 3ms.

No data should be transmitted before the TXEN-input has been high for at least 3ms.

APPLICATION INFORMATION

Antenna input/output

The ANT1 and ANT2 pins provide RF input to the LNA when nRF0433 is in receive mode, and RF output from the PA when nRF0433 is in transmit mode. The antenna connection to nRF0433 is differential and the recommended impedance at the antenna port is 400Ω.

Figure 7 shows a typical application schematic with a differential loop antenna on a Printed Circuit Board (PCB). If a single ended 50Ω antenna is preferred, the most convenient solution is to connect the antenna to nRF0433 using an 8:1 impedance transformer as a balun, see figure 6a). The transformer must have a centre tap at the primary side (primary side connected to the ANT1/ANT2 pins), as explained below.

The output stage (PA) consists of two open collector transistors in a differential pair configuration. +5V DC to the PA must be supplied through the collector load. When connecting a differential loop antenna to the ANT1/ANT2 pins, +5V DC should be supplied through the centre of the loop antenna as shown in figure 7. When using an 8:1 impedance transformer as a balun, +5V DC to the PA should be supplied through the centre tap at the primary side of the transformer as shown in figure 6a).

A single ended antenna can also be connected to nRF0433 by using the differential to single ended matching network as shown in figure 6b). The layout of these matching networks is critical, see application note nAN400-04, “nRF0433 RF and antenna

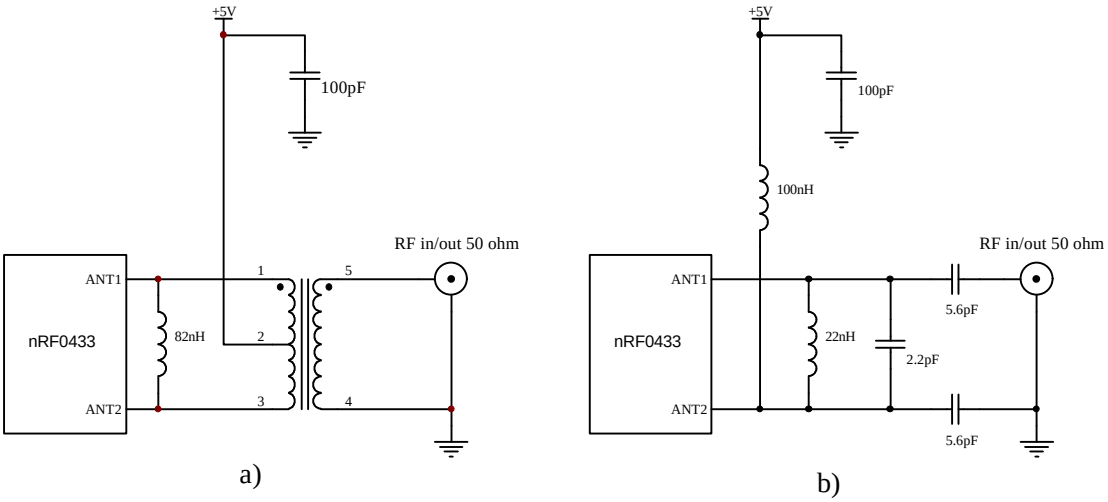


Figure 6. Connection of nRF0433 to single ended antenna by using a) a balun or b) a differential to single ended matching network.

RF output power

Output power is set by the external bias resistor R3 connected between RF_PWR and +5V as shown in figure 7. The RF output power can be set to one of four levels as shown in table 5.

Output power and DC power supply current versus external bias resistor value is shown in table 5 for a differential load of 400Ω.

Bias resistor connected between VDD and RF_PWR [kΩ]	RF output power @ 400Ω, differential [dBm]	Power supply current, I_{DD} [mA]
1000 / Open	10	46
150	4	37
100	-2	33
68	-12	31

Table 5. RF output power settings.

PLL loop filter
The PLL synthesizer loop filter is an external, single-ended second order lag/lead filter. The recommended filter component values are: C1 = 270 pF, C2 =5.6 nF, R1 = 27 kΩ.

VCO inductor
The on-chip voltage controlled oscillator (VCO) needs an external 22nH inductor connected between the VCO1 and VCO2 pins to operate. This inductor should be a high quality chip inductor, Q > 45 @ 433 MHz, with a maximum tolerance of ± 3%, see table 6. See also page 9 for PCB layout guidelines.

Vendors	WWW address	Part. no., 22 nH inductors, 0805
Predan	http://www.predan.com	CS0805-220G
Pulse	http://www.pulseeng.com	PE-0805CD220GTT PE-0805CM220GTT
Coilcraft	http://www.coilcraft.com	0805CS-220XGBC 0805HT-22NTGBC
muRata	http://www.murata.com	LQW1608A22NG00

Table 6. Vendors and part. no. for suitable 22nH inductors.

Transmit/receive mode selection
TXEN is a digital input for selection of transmit or receive mode.
TXEN = "1" selects transmit mode.
TXEN = "0" selects receive mode.

D_{IN} (data input) and D_{OUT} (data output)
The DIN pin is the input to the digital modulator of the transmitter. The input signal to this pin should be standard CMOS logic level at data rates up to 9600 bit/s.

The demodulated digital output data appear at the DOUT pin at standard CMOS logic levels. $f_0 + \Delta f \rightarrow$ "1", $f_0 - \Delta f \rightarrow$ "0".

Frequency difference between transmitter and receiver
For optimum performance, the total frequency difference between transmitter and receiver should not exceed 70 ppm (30 kHz). This yields a crystal stability requirement

of +/- 35 ppm for the transmitter and receiver. Additional frequency difference will result in a -12dB/octave drop in receiver sensitivity. The functional window of the transmission link is typically 450 ppm (200 kHz).

Example: A crystal with +/- 20 ppm frequency tolerance and +/- 25 ppm frequency stability over temperature (-25C to +75C) has a worst case frequency difference of 45 ppm. If the transmitter and receiver operate in different temperature environments, the resulting worst-case frequency difference may be as high as 90 ppm. Resulting drop in sensitivity due to the extra 20 ppm, is then approx. 5dB.

PCB layout and decoupling guidelines

A well-designed PCB is necessary to achieve good RF performance. A PCB with a minimum of two layers inclusive a ground plane is recommended for optimum performance.

The nRF0433 +5V DC supply voltage should be decoupled as close as possible to the VDD pins with a high performance RF capacitor (e.g. 100 pF ceramic). It is preferable to mount a large surface mount capacitor (e.g. 2.2 µF ceramic) in parallel with the smaller value capacitors. The nRF0433 supply voltage should be filtered separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections and VDD bypass capacitors must be connected as close as possible to the IC package. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique to connect the VSS pins to ground, is to have via holes in, or close to the VSS pad.

Full swing digital data or control signals should not be routed close to the PLL loop filter and the external VCO inductor.

The VCO inductor placement is important. The optimum placement of the VCO inductor gives a PLL loop filter voltage of 1.25 +/- 0.5 V. For a 0805 size inductor the length between the centre of the VCO1(2) pad and the centre of the inductor pad should be 2.5 mm, see figure 8 (layout, top view).

PCB layout example

Figure 8 shows a PCB layout example for the application schematic in Figure 7.
A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a continuous ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane. There is no ground plane behind the antenna.

For more layout information, please refer to application note nAN400-04, “nRF0433 RF and antenna layout”.

APPLICATION SCHEMATIC

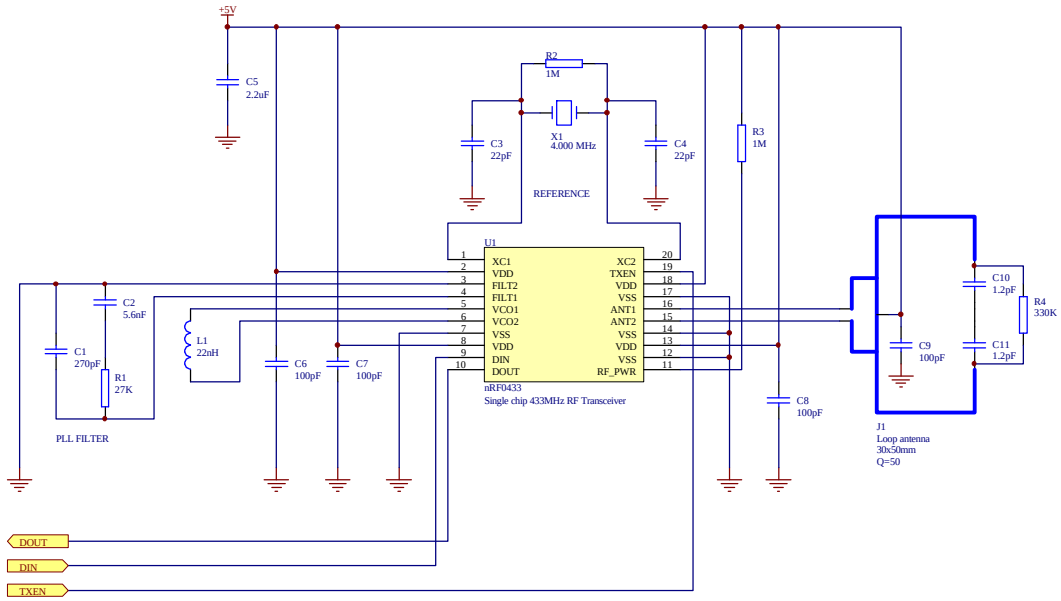
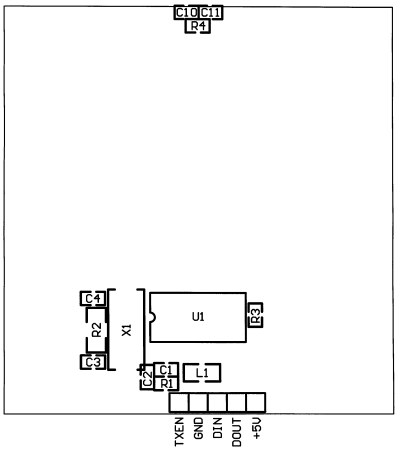


Figure 7. nRF0433 application Schematic.

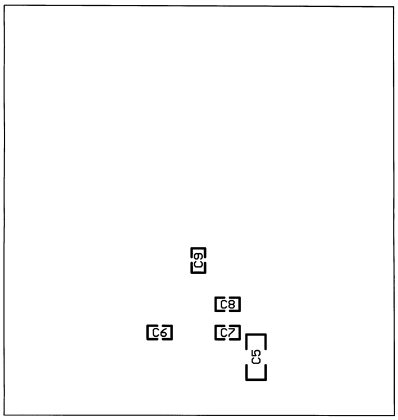
Component	Description	Value	Units
C1	NP0 ceramic chip capacitor, (PLL loop filter)	270	pF
C2	X7R ceramic chip capacitor, (PLL loop filter)	5.6	nF
C3	NP0 ceramic chip capacitor, (Crystal oscillator)	22	pF
C4	NP0 ceramic chip capacitor, (Crystal oscillator)	22	pF
C5	X7R ceramic chip capacitor, (Supply decoupling)	2.2	µF
C6	NP0 ceramic chip capacitor, (Supply decoupling)	100	pF
C7	NP0 ceramic chip capacitor, (Supply decoupling)	100	pF
C8	NP0 ceramic chip capacitor, (Supply decoupling)	100	pF
C9	NP0 ceramic chip capacitor, (Supply decoupling)	100	pF
C10	NP0 ceramic chip capacitor, (Antenna tuning)*	1.2±0.1	pF
C11	NP0 ceramic chip capacitor, (Antenna tuning)*	1.2±0.1	pF
L1	VCO inductor, tolerance ±3%, Q>45 @ 433 MHz Recommended inductor part.no.: Predan: Part.no.: CS0805-220G Pulse: Part.no.: PE-0805CD220GTT Part.no.: PE-0805CM220GTT Coilcraft: Part.no.: 0805CS-220XGBC Part.no.: 0805HT-22NTGBC muRata: Part.no.: LQW1608A22NG00	22	nH
R1	1/8W chip resistor, (PLL loop filter)	27	kΩ
R2	1/8W chip resistor, (Crystal oscillator)	1	MΩ
R3	1/8W chip resistor, (Transmitter power setting)	1	MΩ
R4	1/8W chip resistor, (Antenna Q reduction)	330	kΩ
X1	Crystal	4.000	MHz

Table 7. Recommended External Components.

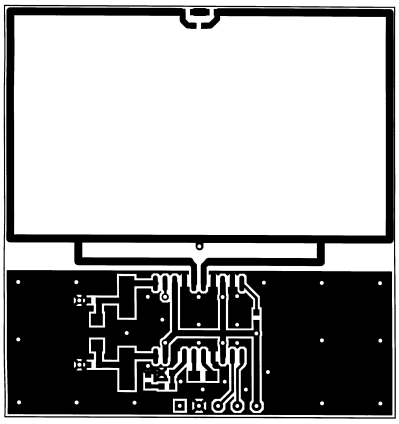
* Capacitors with larger tolerance than specified will result in de-tuning of the antenna and reduced communication distance.



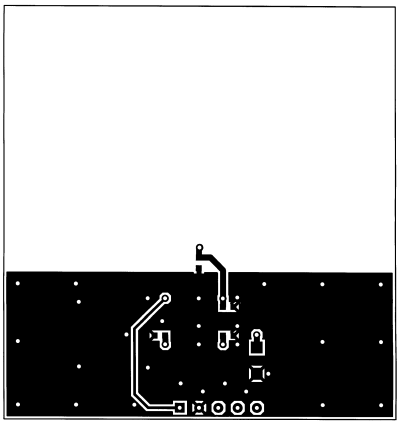
Top silk screen



Bottom silk screen



Top view



Bottom view

Figure 8. PCB layout (example) for nRF0433 with loop antenna (not actual size).

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 8. Definitions.

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

Product specification: Revision Date: 29.02.2000.

Datasheet order code: 290200-nRF0433.

YOUR NOTES

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