Revision January 2003

AR2111 Radio-on-a-Chip for 2.4 GHz Wireless LAN

General Description

The Atheros AR2111 is part of the AR5001X solution for 5 GHz and 2.4 GHz combo wireless local area networks (WLANs). When combined with AR5111 and AR5211this chip set enables a high performance, low cost, compact solution that easily fits onto a Mini PCI form factor or one side of a PC Card.

The AR5111 operates in:

- 2.412 GHz to 2.472 GHz U.S. frequency bands
- 2.484 GHz Japanese band

The device requires both 2.5 V and 3.3 V supplies.

The transmitter takes the output of the AR5111 chip, down converts it to the 2.4 GHz frequency band and drives the signal off-chip.

The receiver up converts the 2.4 GHz incoming signal to the 5 GHz signal suitable for the AR5111 input.

The frequency synthesizer requires to generate only two L.O. frequencies of 3.136 GHz and 3.168 GHz.

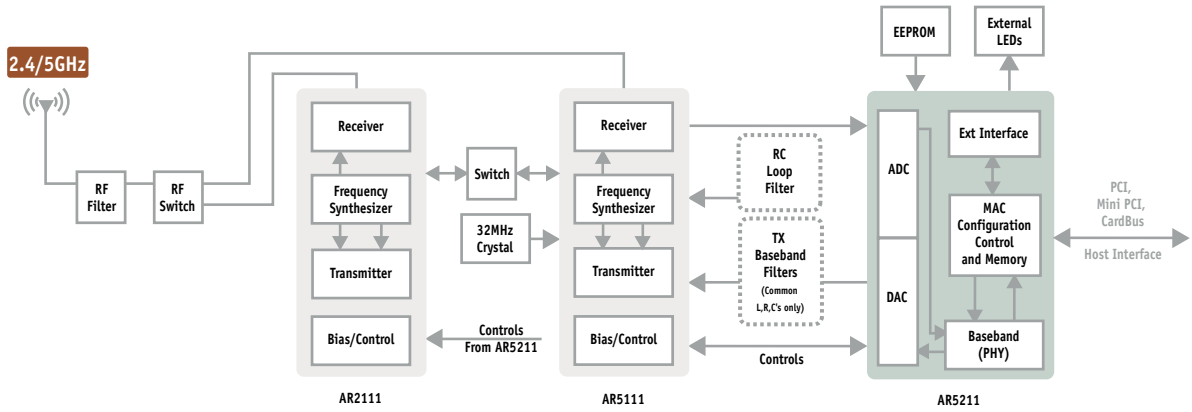
The transmitter, receiver, and frequency synthesizer functions are controlled using the AR5211 through a serial programming bus and on-chip control registers.

All internal bias currents are generated on-chip with a single external reference resistor.

Features

- No external VCOs and SAW filters needed
- 2.412 GHz to 2.484 GHz frequency band operation
- 48-pin leadless plastic chip carrier package
- Together with the AR5111 and AR5211:
  - IEEE 802.11a/b compatible
  - Supports OFDM modulation at 2.4 GHz
  - CCK, DSSS, BPSK, QPSK, 16 QAM, and 64 QAM modulation schemes supported
  - Data rates of 1 Mbps to 54 Mbps
  - Low power sleep mode controlled by the AR5211

System Block Diagram



1. Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1-1 summarizes the absolute maximum ratings and Table 1-2 lists the recommended operating conditions for the AR2111. Absolute maximum ratings are those values beyond which damage to the device can occur. Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended.

Table 1-1. **Absolute Maximum Ratings**

Symbol	Parameter	Max. Rating	Unit
V_{dd2}	Maximum supply voltage	3.0	V
V_{dd3}	Maximum I/O supply voltage	4.0	V
RF_{in}	Maximum RF input (reference to 50 Ω)	+10	dBm
T_{store}	Storage temperature	-65 to 150	°C
ESD	Electrostatic discharge tolerance	2000	V

1.2 Recommended Operating Conditions

Table 1-2. **Recommended Operating Conditions**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{dd2}	Supply voltage	±5%[1]	2.375	2.5	2.625	V
V_{dd3}	I/O voltage	±10%[1]	3.0	3.3	3.6	V
T_{case}	Case temperature	—	0	25	85	°C
T_j	Junction temperature	—	0	50	110	°C
θ_{JA}	Junction to ambient temperature	—	—	—	24	°C/W

[1]The recommended power-on sequence is to have V_{dd2} turn on before V_{dd3}.

2. Functional Description

The AR5111 radio front end (see Figure 2-1) consists of four major functional blocks:

- Receiver (RX)
- Transmitter (TX)
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)

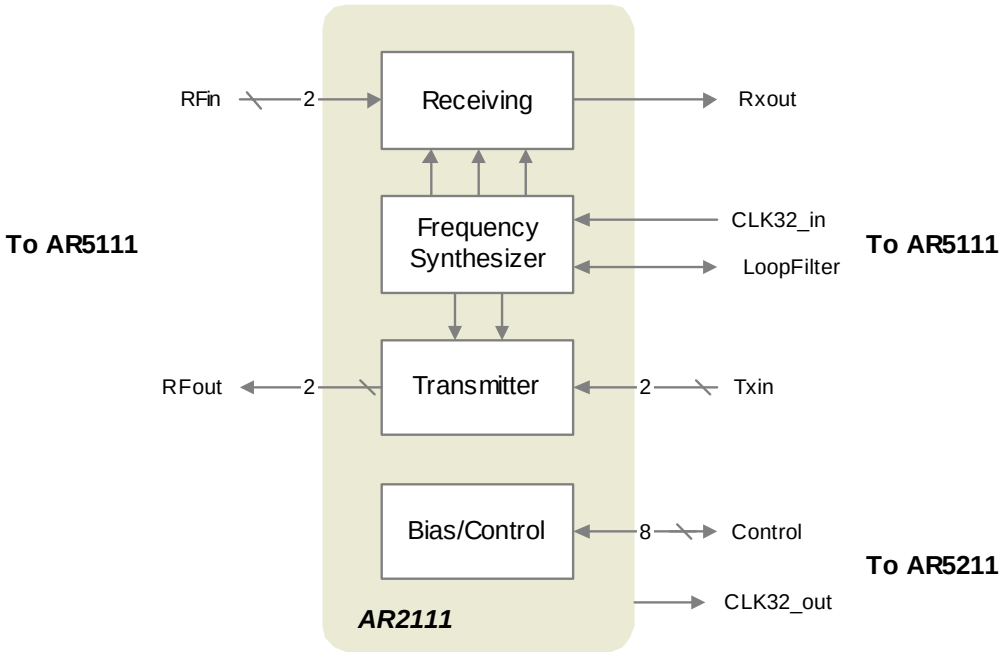


Figure 2-1. **AR2111 Functional Block Diagram**

2.1 Receiver (RX) Block

The receiver up converts a 2.4 GHz RF signal to a 5.6 GHz signal, which is subsequently down-converted to baseband by the AR5111. The input frequency range of the AR2111 receiver is 2.412 to 2.484 GHz.

The receiver topology includes a low noise amplifier (LNA), a radio frequency (RF) mixer as shown in Figure 2-2. The RF mixer converts the output of the on-chip LNA to the 5.6 GHz band. The receiver output signals are then sent to the AR5111 RoC.

The receive chain can be digitally powered down to conserve power.

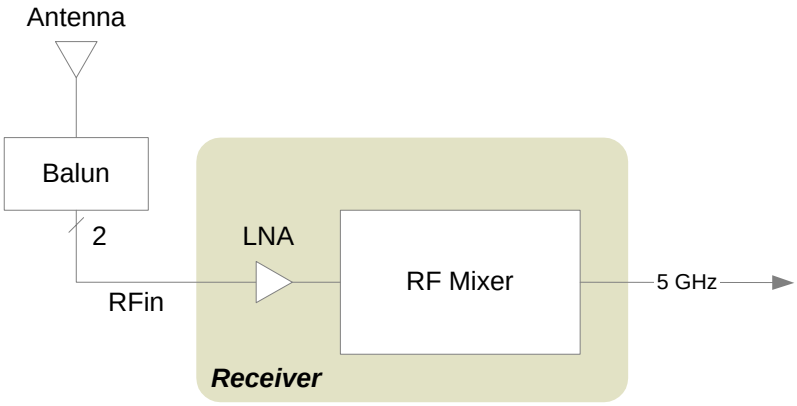


Figure 2-2. **RF Receiver Functional Block Diagram**

2.2 Transmitter (TX) Block

The transmitter converts the incoming 5.6 GHz signal from AR5111 to 2.4 GHz frequency band and transmits the resulting signal into the antenna as depicted in Figure 2-3. The inputs of the transmitter are PA outputs of the AR5111.

The radio frequency (RF) mixer converts the 5.6 GHz signals into 2.4 GHz. These signals are driven off-chip through a power amplifier. The transmit chain can be digitally powered down to conserve power.

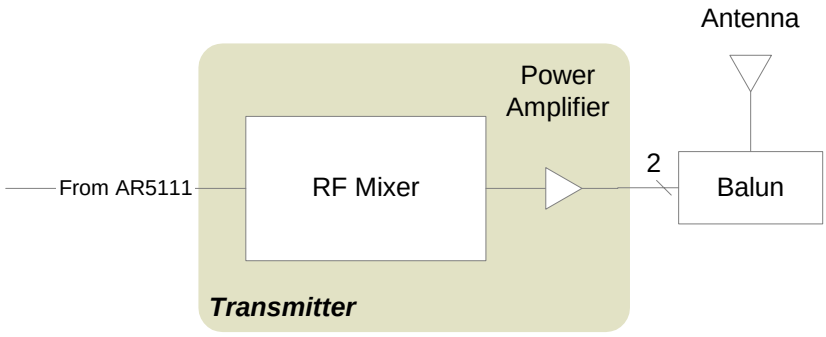


Figure 2-3. **RF Transmitter Functional Block Diagram**

2.3 Synthesizer (SYNTH) Block

The synthesizer is a phase-locked loop (PLL) that generates the local oscillator (LO) frequencies for the receiver and transmitter mixers. The topology of the synthesizer is shown in Figure 2-4. A signal generated from a 32 MHz crystal is used as the reference input for the synthesizer. See "Bias/Control (BIAS) Block" on page 5 for more details. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/frequency locked loop. An external RC network implements the loop filter. The synthesizer in conjunction with the AR5111 can generate 2.4 GHz RF outputs at 5 MHz channel spacing.

On power up or channel reselection, the synthesizer takes approximately 1 ms to settle.

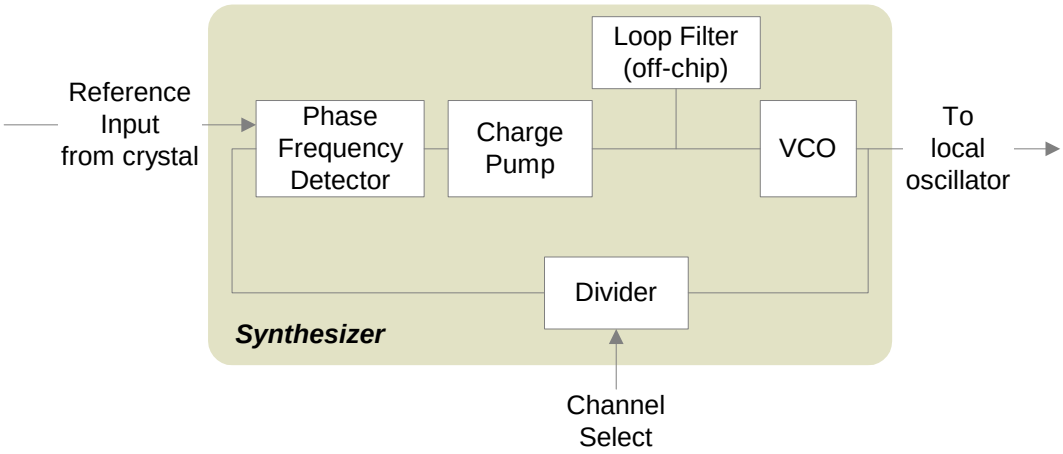


Figure 2-4. **RF Synthesizer Block Diagram**

2.4 Bias/Control (BIAS) Block

The bias/control block provides the reference voltages and currents for all other circuit blocks (see Figure 2-5). An on-chip bandgap reference circuit provides the needed voltage and current references based on an external 6.19 kΩ ±1% resistor. The state of the AR2111 is controlled through the control interface of the AR5211.

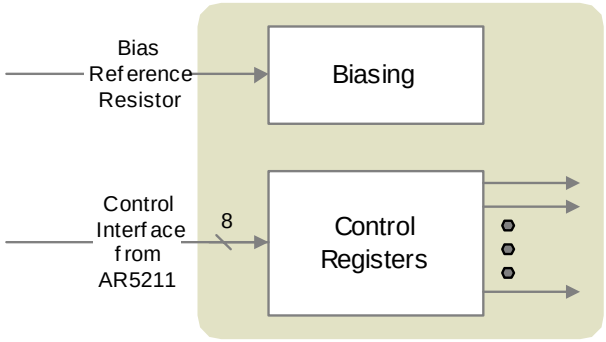


Figure 2-5. **Bias/Control Architecture**

3. Typical Application

Figure 3-1 shows a typical configuration for a transceiver built with the AR5001 chip set.

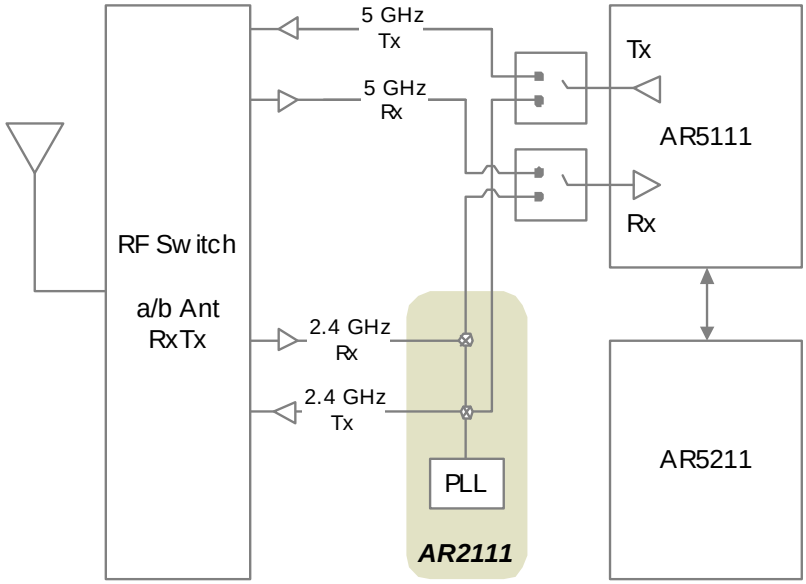


Figure 3-1. **Typical Application Block Diagram using the AR2111**

4. Package Dimensions

The AR2111 is packaged in a 48-pin leadless plastic chip carrier (LPCC). The LPCC can be sourced from any one of two package drawings. The external dimensions are identical from all sources.

The LPCC package drawings and dimensions are provided in Figure 4-1 and Figure 4-2 and Table 4-1.

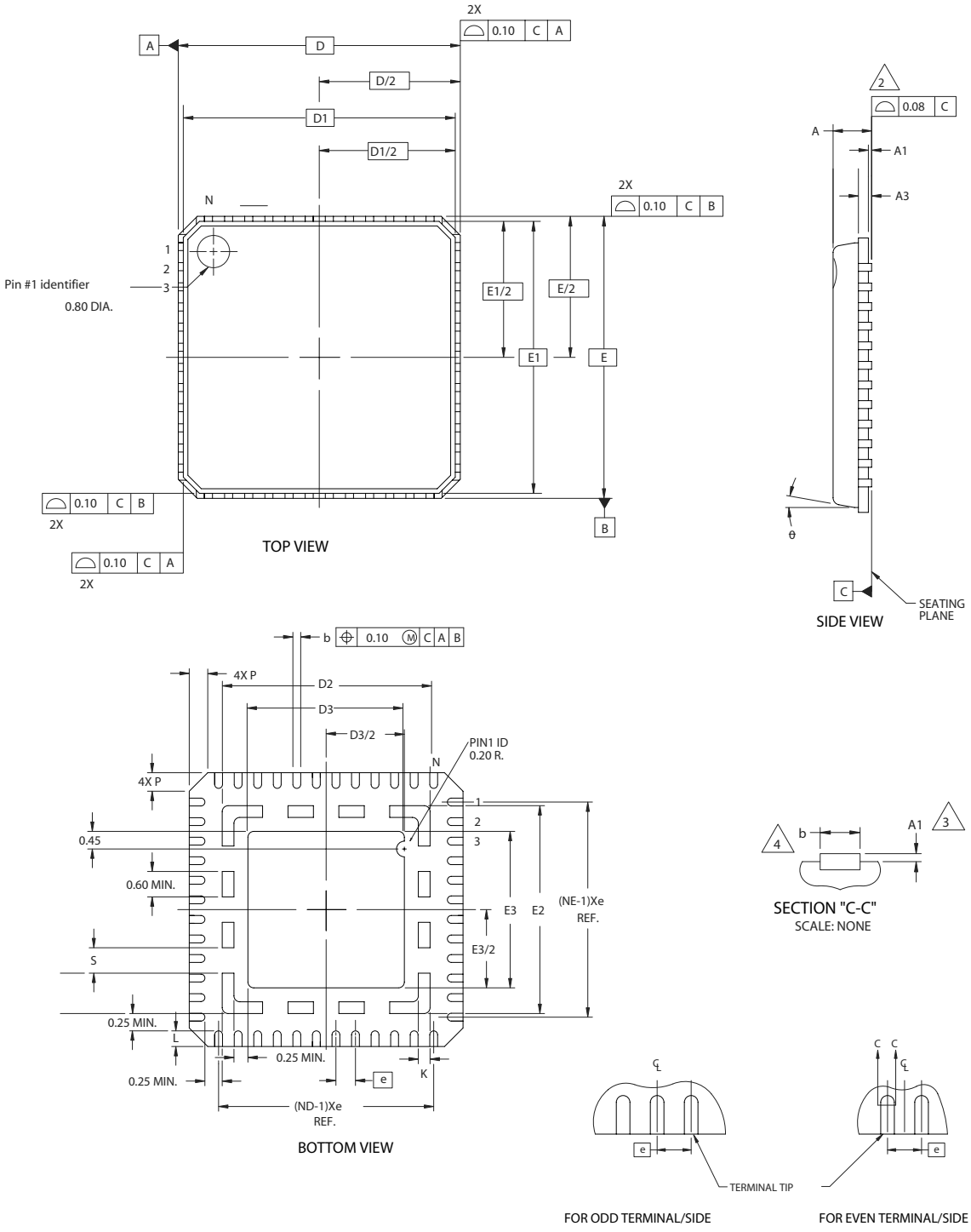


Figure 4-1. **LPCC "Package A" Drawing**

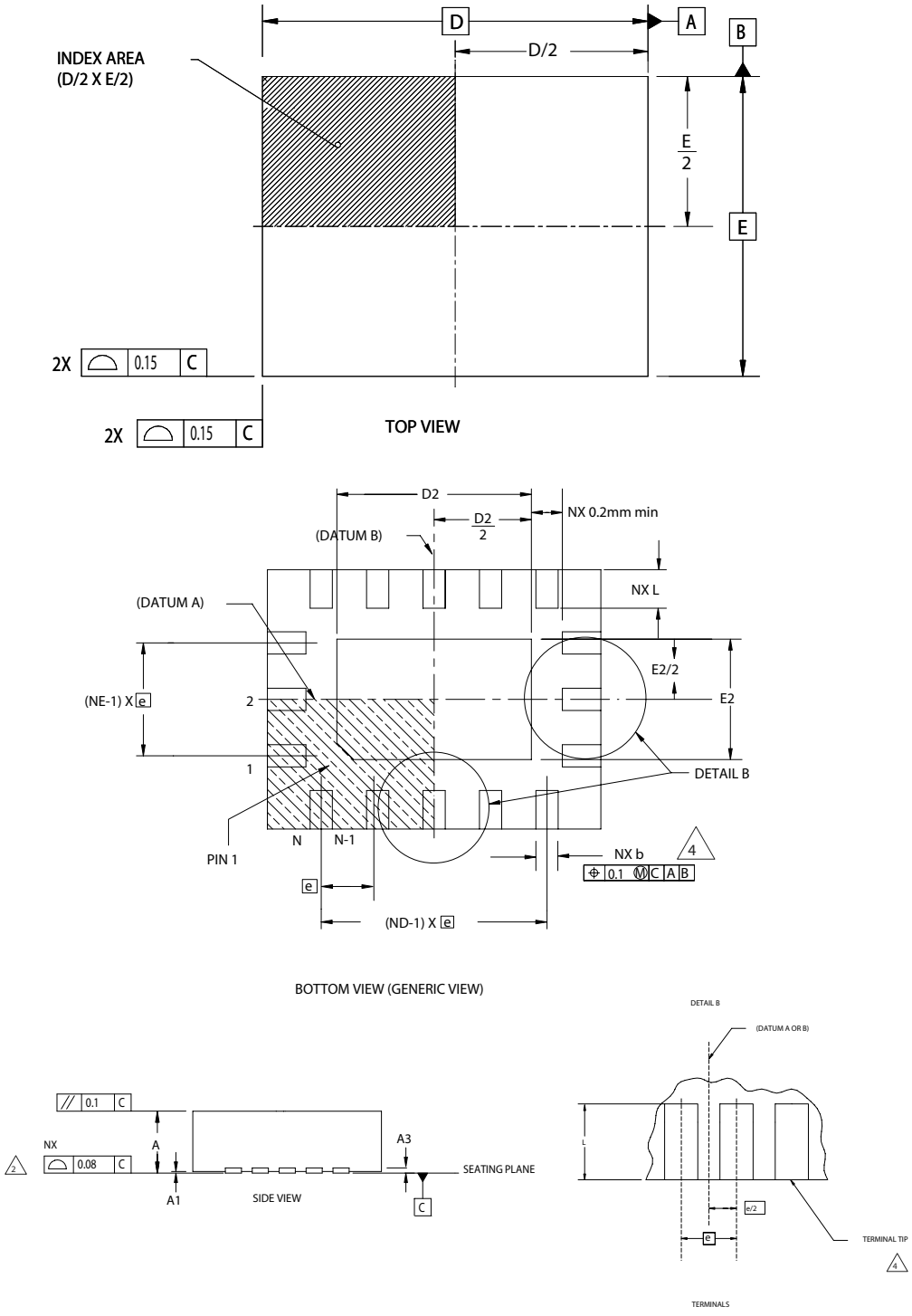


Figure 4-2. **LPCC “Package B” Drawing**

Table 4-1. **LPCC "Package A & B" Dimensions**

Dimension Label	Min.	Nom.	Max.	Unit.
A	0.80	0.90	1.00	mm
b	0.23	0.25	0.28	mm
D	6.90	7.00	7.10	mm
E	6.90	7.00	7.10	mm
A3		0.20 REF		mm
D2	5.15	5.30	5.95	mm
A1	0.00	0.01	0.05	mm
e		0.50 Basic		mm
k		0.20		mm
L	0.30	0.40	0.50	mm
N		48		Number of terminals
NE		12		Number of terminals in X-direction
ND		12		Number of terminals in Y-direction

Notes:
1. Dimension and tolerance conform to ASME Y14.5M–1994.
2. Applied to exposed pads and terminals. Exclude embedded part of exposed pads from the measurement.
3. Applied only to terminals.
4. Dimension b applies to plated terminal and is measured from the terminal tip.

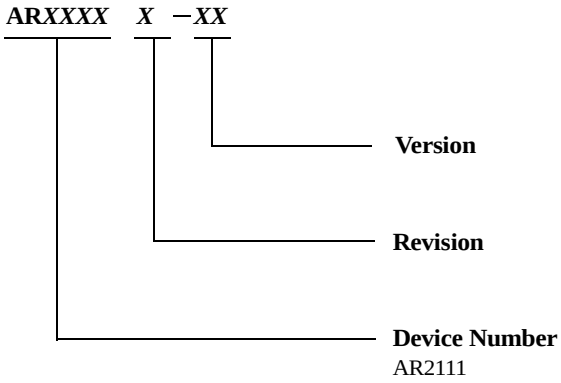
Table 4-2. **LPCC "Package A only" Dimensions**

Dimension Label	Min.	Nom.	Max.	Unit.
D1		6.75 Basic		
D3	3.85	4.00	4.14	mm
E1		6.75 Basic		mm
E3	3.85	4.00	4.15	mm
J	0.60	1.00	1.50	mm
K	0.20	0.30	0.40	mm
P	0.24	0.42	0.60	mm
S	0.50	0.60	0.65	mm
θ		12° Max		

Notes:
1. All dimensions are in millimeters, and all angles are in degrees.
2. Primary DATUM C and seating pane are defined by the spherical crowns of the solder balls.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary DATUM C.
4. There shall be a minimum clearance of 0.20 mm between the edge of the solder ball and the body edge.

Ordering Information

The order number is determined by the selection of these options. See the following example.



An order number, AR2111A-*00* specifies a current version of the AR2111.

Revision History

Revision	Description of Changes
January 2003	Initial release.

Document Number: 987-00006-001

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