FUJITSU

Jun. 2001
Edition 2.0

ASSP
Fractional-N PLL Frequency Synthesizer

MB15F86UL

■ DESCRIPTION

The Fujitsu MB15F86UL is Fractional-N Phase Locked Loop (PLL) frequency synthesizer with fast lock up funcional. The Fractional-N PLL operating up to 2500*MHz and the integer PLL operating up to 600MHz are integrated on a chip.

MB15F86UL is used charge pump which is well-balanced output current with 1.5mA and 6mA selectable by serial data, direct power save control and digital lock detector. In addition, MB15F86UL adopts a new architecture to achieve fast lock.

The new package(Thin Bump Chip Carrier20) decreases a mount area of MB15F86UL more than 30% comparing with the former B.C.C.16(for dual PLL, MB15F03SL).

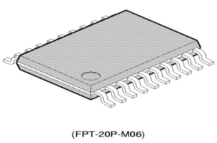
MB15F86UL is ideally suited for wireless mobile communications, such as TDMA or CDMA .

■ FEATURES

- High frequency operation: RF synthesizer : 2500*MHz max
  IF synthesizer : 600MHz max
- Low power supply voltage: V_{CC} = 2.7 to 3.6 V
- Ultra Low power supply current : I_{CC} = 5.8 mA typ. (V_{CC} = V_P=3.0V, Ta=25°C in IF, RF locking state)
- Direct power saving function : Power supply current in power saving mode
  Typ. 0.1 µA(Vcc=Vp=3.0V, Ta=25°C), Max. 10 µA(Vcc=Vp=3.0V)
- Fractional function : modulo 3 to 16 programmable(implemented in RF-PLL)
- Dual modulus prescaler : 2500*MHz prescaler(16/17 or 32/33) / 600MHz prescaler(8/9 or 16/17)
- Serial input 14-bit programmable reference divider: R =(RF section 8bit) 3 to 255, (IF section 14bit) 3 to16,383
- Serial input programmable divider consisting of:
  RF section -Binary 5-bit swallow counter: 0 to 31
  -Binary 10-bit programmable counter: 18 to 1,023
  -Binary 4-bit fractional counter numerator: 0 to 15
  IFsection -Binary 4-bit swallow counter: 0 to 15
  -Binary 11-bit programmable counter: 3 to 2,047
- On-chip phase comparator for fast lock and low noise
- Operating temperature: Ta = –40 to 85°C
- Small package Bump Chip Carrier.0(3.4mm*3.6mm*0.6mm)

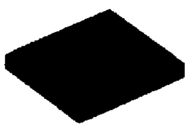
Note: In case of *fmax=2500MHz, the following conditions must be fufilled. Except for it, fmax is up to 2000MHz.
Prescaler ratio=32 (N>P) at all divide ratio of used operating frequency.
Refer to a calculation formula of divide ratio. f_{VCORF}=(P x N + A + F/Q) x fosc / R

20-pin, Plastic TSSOP



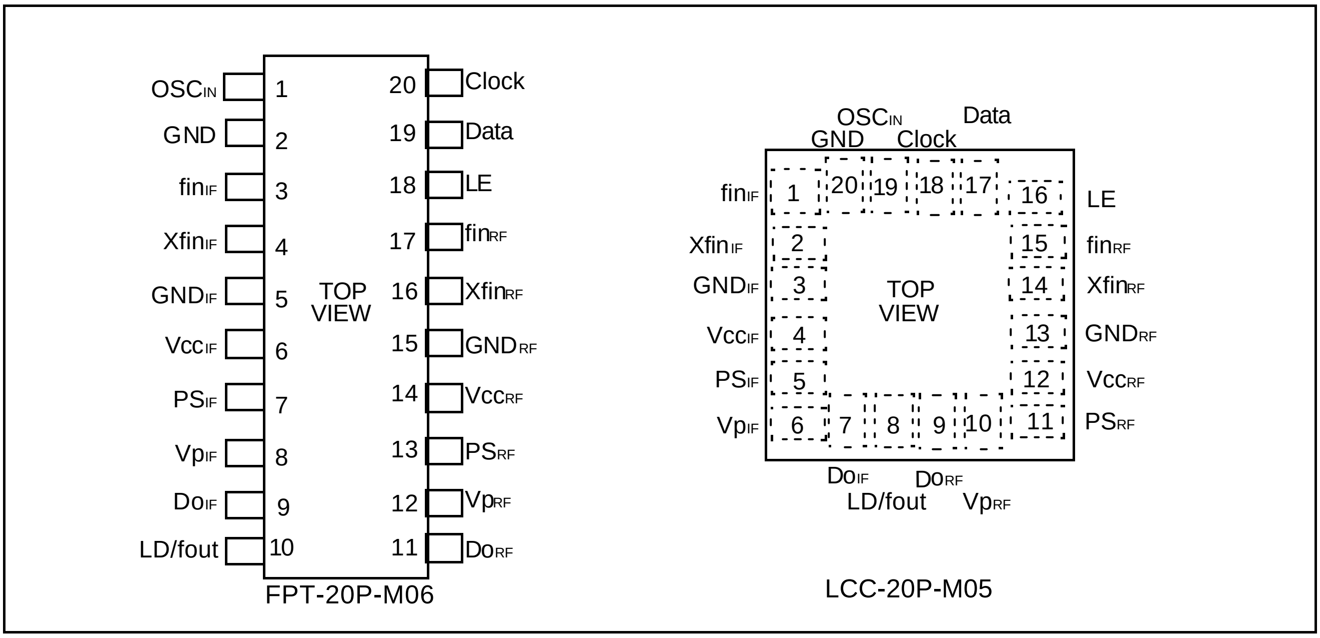
(FPT-20P-M06)

20-pad, Plastic BCC



(LCC-20P-M05)

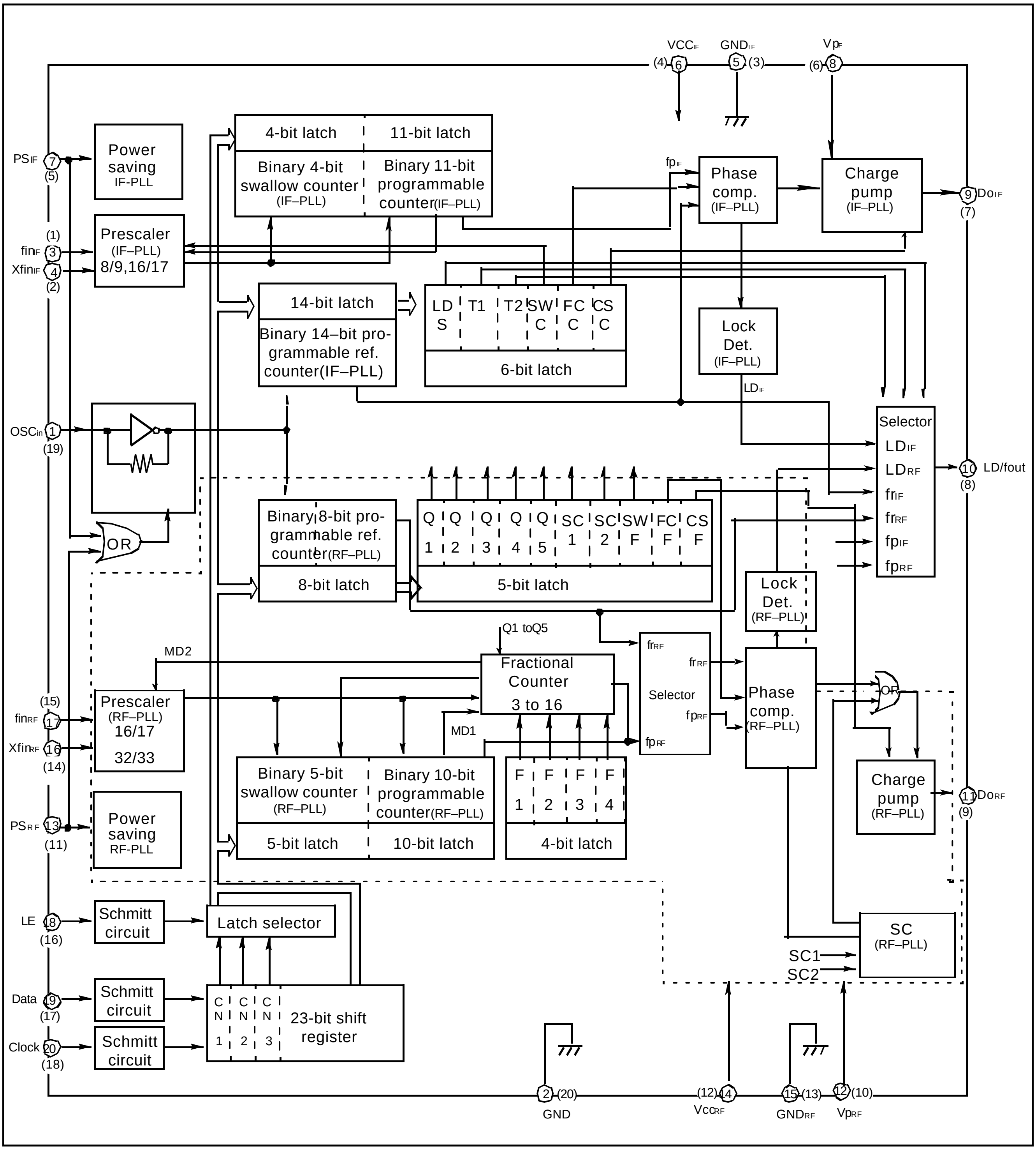
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.		Pin name	I/O	Descriptions
TSSOP	BCC			
1	19	OSC_{in}	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.
2	20	GND	-	Ground for OSC input buffer and the shift registor circuit.
3	1	fin_{IF}	I	Prescaler input pin for the IF-PLL. Connection to an external VCO should be AC coupling.
4	2	$Xfin_{IF}$	I	Prescaler complimentary input for the IF-PLL section. This pin should be grounded via a capacitor.
5	3	GND_{IF}	-	Ground for the IF-PLL section.
6	4	Vcc_{IF}	-	Power supply voltage input pin for the IF-PLL section(except for the charge pump circuit), the shift register and the oscillator input buffer. When power is OFF, latched data of IF-PLL is lost.
7	5	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at ”L” at Power-ON. (Open is prohibited.) PS_{IF} = ”H” ; Normal mode, PS_{IF} = ”L” ; Power saving mode
8	6	Vp_{IF}	-	Power supply voltage input pin for the IF-PLL charge pump.
9	7	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	8	LD/fout	O	Lock detect signal output(LD)/ phase comparator monitoring output (fout). The output signal is selected by a LDS bit in a serial data. LDS bit = "H" ; outputs fout signal, LDS bit = "L" ; outputs LD sihnal
11	9	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
12	10	Vp_{RF}	-	Power supply voltage input pin for the RF-PLL charge pump.
13	11	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at ”L” at Power-ON. (Open is prohibited.) PS_{RF} = ”H” ; Normal mode, PS_{RF} = ”L” ; Power saving mode
14	12	Vcc_{RF}	-	Power supply voltage input pin for the RF-PLL section(except for the charge pump circuit).
15	13	GND_{RF}	-	Ground for the RF-PLL section.
16	14	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
17	15	fin_{RF}	I	Prescaler input pin for the RF-PLL. Connction to an external VCO should be AC coupling.
18	16	LE	I	Load enable signal input (with the schmitt trigger circuit.) On a rising edge of load enable, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
19	17	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
20	18	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.

■ BLOCK DIAGRAM



O -- TSSOP 20
( ) -- BCC 20

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit	Remark
		Min.	Max.		
Power supply voltage	V_{CC}	–0.5	+4.0	V	
	V_p	V_{CC}	+4.0	V	
Input voltage	V_I	–0.5	V_{CC}+0.5	V	
Output voltage	V_O	GND	V_{CC}	V	LD/fout
	V_{DO}	GND	V_p	V	Do
Storage temperature	T_{stg}	–55	+125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	V_{CCRF} = V_{CCIF}
	V_p	V_{CC}	3.0	3.6	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	T_a	–40	–	+85	°C	

Handling Precautions

(1) Vcc_{RF},Vp_{RF},Vcc_{IF} and Vp_{IF} must supply equal voltage.
Even if either RF-PLL or IF-PLL is not used, power must be supplied to both Vcc_{RF},Vp_{RF},Vcc_{IF} and Vp_{IF} to keep them equal. It is recommended that the non-use PLL is controlled by power saving function.

(2) To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CCIF}*1	fin_{IF}=480MHz Vcc_{IF}=Vp_{IF}=3.0V,SWC=0	1.0	1.6	2.3	mA
		I_{CCRF}*1	fin_{RF}=2000MHz Vcc_{RF}=Vp_{RF}=3.0,SWF=1V	2.8	4.2	5.8	mA
Power saving current		I_{PSIF}	PS= ”L”	–	0.1*2	10	µA
		I_{PSRF}	PS= ”L”	–	0.1*2	10	µA
Operating frequency	fin_{IF}*3	fin_{IF}	IF PLL	100	–	600	MHz
	fin_{RF}*3	fin_{RF}	RF PLL	400	–	2000	MHz
	fin_{RF}*3,*8	fin_{RF}	RF PLL	400		2500	MHz
	OSC_{IN}	fosc	–	3	–	40	MHz
Input sensitivity	fin_{IF}	$Pfin_{IF}$	IF PLL, 50 Ω system	-15	–	+2	dBm
	fin_{RF}	$Pfin_{RF}$	RF PLL, 50 Ω system	-15	–	+2	dBm
	OSC_{IN}	V_{OSC}	–	0.5	–	V_{CC}	Vp-p
"H" level Input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	Vcc × 0.7+0.4	–	–	V
"L" level Input voltage		V_{IL}	Schmitt trigger input	–	–	Vcc× 0.3-0.4	
"H" level Input voltage	PS	V_{IH}	–	Vcc× 0.7	–	–	V
"L" level Input voltage		V_{IL}	–	–	–	Vcc× 0.3	
"H" level Input current	Data, Clock, LE, PS	I_{IH}*4	–	–1.0	–	+1.0	µA
"L" level Input current		I_{IL}*4	–	–1.0	–	+1.0	
"H" level Input current	OSC_{IN}	I_{IH}	–	0	–	+100	µA
"L" level Input current		I_{IL}*4	–	–100	–	0	
"H" level output voltage	LD/fout	V_{OH}	V_{CC}=V_p=3.0V, I_{OH}=–1mA	Vcc – 0.4	–	–	V
"L" level output voltage		V_{OL}	V_{CC}=V_p=3.0V, I_{OL}=1mA	–	–	0.4	
"H" level output voltage	Do_{IF} Do_{RF}	V_{DOH}	V_{CC}=V_p=3.0V, I_{DOH}=-0.5mA	Vp – 0.4	–	–	V
"L" level output voltage		V_{DOL}	V_{CC}=V_p=3.0V, I_{DOL}=0.5mA	–	–	0.4	
High impedance cutoff current	Do_{IF} Do_{RF}	I_{OFF}	V_{CC}=3.0V, V_{OFF}=0.5V to V_p–0.5V	–	–	2.5	nA
"H"level Output current	LD/fout	I_{OH}*4	V_{CC} = Vp = 3.0V	–	–	-1.0	mA
"L" level Output current		I_{DOL}*4	V_{CC} = Vp = 3.0V	1.0	–	–	

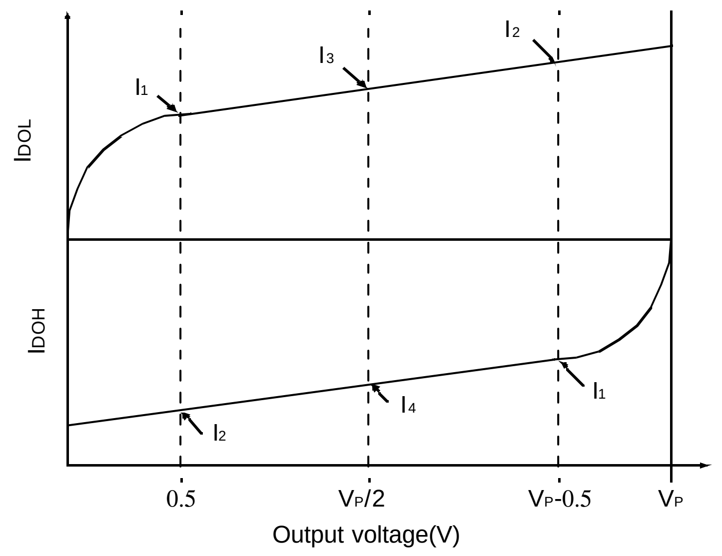
(Continued)

(Continued)

Ta =(V_{CC} = 2.7 to 3.6 V, Ta = –40 to +85°C)

Parameter		Symbol	Condition		Value			Unit
					Min.	Typ.	Max.	
"H"level Output current	Do_{IF} Do_{RF}	I_{DOH}*4	$V_{CC}=V_p$ =3.0 V $V_{DOH}=V_p$ /2 Ta= 25°C	CS bit ="H"	–8.2	–6.0	–4.1	mA
				CS bit ="L"	–2.2	–1.5	–0.8	
"L" level Output current		I_{DOL}	$V_{CC}=V_p$ =3.0 V $V_{DOL}=V_p$ /2 Ta= 25°C	CS bit ="H"	4.1	6.0	8.2	
				CS bit ="L"	0.8	1.5	2.2	
Charge pump current rate	I_{DOL}/I_{DOH}	I_{DOMT}*5	$V_{DO}=V_p/2$		–	3	–	%
	vs V_{DO}	I_{DOVD}*6	0.5V ≤ V_{DO} ≤ V_p-0.5V		–	10	–	%
	vs Ta	I_{DOTA}*7	-40°C ≤ Ta ≤ 85 °C, $V_{DO}=V_p/2$		–	5	–	%

*1: Conditions; fosc=13MHz, Ta = 25°C in locking state.
*2: $Vcc_{IF}=Vp_{IF}=Vcc_{RF}=Vp_{RF}$=3.0V, fosc=13MHz, Ta = 25°C, in power saving mode.
*3: AC coupling. 1000pF capacitor is connected.
*4: The symbol "-"(minus) means direction of current flow.
*5: Vcc=Vp=3.0V, Ta=25°C ($||I_3| - |I_4||$) / [($|I_3| + |I_4|$)/2] x 100(%)
*6: Vcc=Vp=3.0V, Ta=25°C [($||I_2| - |I_1||$) /2] / [($|I_1| + |I_2|$)/2] x 100(%) (Applied to each I_{DOL}, I_{DOH})
*7: Vcc=Vp=3.0V, [($||I_{DO(85C)}| - |I_{DO(-40C)}||$) /2] / [($|I_{DO(85C)}| + |I_{DO(-40C)}|$) /2] x 100(%) (Applied to each I_{DOL}, I_{DOH})
*8: In case of *fmax=2500MHz, the following conditions must be fufilled. Except for it, fmax is up to 2000MHz.
Prescaler ratio=32 (N>P) at all divide ratio of used operating frequency.
Refer to a calculation formula of divide ratio. $fvco_{RF}$=(P x N + A + F/Q) x fosc / R



■ FUNCTIONAL DESCRIPTIONS

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF-PLL sections, programmable reference dividers of IF/RF-PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On a rising edge of clock, one bit of serial data is transferred into the shift register. On a rising edge of load enable signal , the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit **(CN3=1 is prohibited)**

Control bit			Destination of serial data
CN1	CN2	CN3	
0	0	0	The programmable reference counter for the IF-PLL.
1	0	0	The programmable counter and the swallow counter for the IF-PLL
0	1	0	The programmable reference counter for the RF-PLL.
1	1	0	The programmable counter and the swallow counter for the RF-PLL

Table2. Serial data format

LLSB **Direction of data shift** → **MSB**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
0	0	0	Rc 1	Rc 2	Rc 3	Rc 4	Rc 5	Rc 6	Rc 7	Rc 8	Rc 9	Rc 10	Rc 11	Rc 12	Rc 13	Rc 14	LD S	T 1	T 2	Sw c	FC c	CS c
1	0	0	Ac 1	Ac 2	Ac 3	Ac 4	0	0	0	Nc 1	Nc 2	Nc 3	Nc 4	Nc 5	Nc 6	Nc 7	Nc 8	Nc 9	Nc 10	Nc 11	X	X
0	1	0	RF 1	RF 2	RF 3	RF 4	RF 5	RF 6	RF 7	RF 8	0	Q 1	Q 2	Q 3	Q 4	Q 5	0	SC 1	SC 2	Sw F	FC F	CS F
1	1	0	AF 1	AF 2	AF 3	AF 4	AF 5	NF 1	NF 2	NF 3	NF 4	NF 5	NF 6	NF 7	NF 8	NF 9	NF 10	F 1	F 2	F 3	F 4	0

Control bit (CN3)
Control bit (CN2)
Control bit (CN1)

Rc1 to Rc14	:Divide ratio setting bits for the reference counter of the IF(3 to 16383)
Ac1 to Ac4	:Divide ratio setting bits for the swallow counter of the IF (0 to 15, A<N)
Nc1 toNc11	:Divide ratio setting bits for the programmable counter of the IF(3 to 2047)
LDS,T1,T2	:Select bits for the lock detect output or a monitoring phase comparison frequency
SWc	:Divide ratio setting for the prescaler of the IF
FCc	:Phase control bit for the phase detector of the IF
CSc	:Charge pump current select bit of the IF
RF1 to RF8	:Divide ratio setting bits for the reference counter of the RF(3 to 255)
Q1 to Q5	:Fractional-N increment setting bit (3 to 16)
AF1 to AF5	:Divide ratio setting bits for the swallow counter of the RF (0 to 31, A<N-2)
NF1 to NF10	:Divide ratio setting bits for the programmable counter of the RF(18 to 1023)
F1 to F4	:Fractional-N increment setting bit for the fractional accumulator (0 to 15, F<Q)
SC1,SC2	:Spurious cancel set bit of the RF.
SWF	:Divide ratio setting for the prescaler of the RF
FCF	:Phase control bit for the phase detector of the RF.
CSF	:Charge pump current select bit of the RF
X	:Dummy bit(Set "0" or "1")

Note:Data input with MSB first

1)RF synthesizer Data Setting(Fractional-N)

The divide ratio can be calculated using the following equation:

$$f_{vcoRF} = N_{TOTAL} \times f_{osc} / R$$

$$N_{TOTAL} = P \times N + A + F/Q \qquad (A<N-2,\ F<Q)$$

f_{vcoRF} :Output frequency of external voltage controlled oscillator(VCO)
N_{TOTAL} :Total division ratio from prescaler input to the phase detector input
fosc :Output frequency of the reference frequency oscillator
R :Preset divide ratio of binary 8bit reference counter(3 to 255)
P :Preset divide ratio of modlus prescaler(16 or 32)
N :Preset divide ratio of binary 10bit programmable counter(18 to 1023)
A :Preset divide ratio of binary 5 bit swallow counter(0 to 31)
F :A numerator of fractional-N.(0 to 15)
Q :A denominator of fractional-N. modulo 3 to 16
Note: When Q is set more than 10, a prescaler ratio should be set 32.

Table3. Binary 9-bit Programmable Reference Counter Data Setting(RF1 to RF8)

Divide ratio (R)	RF 8	RF 7	RF 6	RF 5	RF 4	RF 3	RF 2	RF 1
3	0	0	0	0	0	0	1	1
4	0	0	0	0	0	1	0	0
-	-	-	-	-	-	-	-	-
52	0	0	1	1	0	1	0	0
-	-	-	-	-	-	-	-	-
255	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table4. Fractional-N increment of the fractional accumulator Data setting(F1 to F4)

Setting value(F)	F4	F3	F2	F1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
-	-	-	-	-
15	1	1	1	1

Note: • F<Q

Table5. Fractional-N denominator of the fractional accumulator Data setting(Q1 to Q5)

Setting value(F)	Q5	Q4	Q3	Q2	Q1
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
-	-	-	-	-	-
16	1	0	0	0	0

Note: • F<Q

Table.6 Binary 10-bit Programmable Counter Data Setting(NF1 to NF10)

Divide ratio (N)	NF 10	NF 9	NF 8	NF 7	NF 6	NF 5	NF 4	NF 3	NF 2	NF 1
18	0	0	0	0	0	1	0	0	1	0
19	0	0	0	0	0	1	0	0	1	1
-	-	-	-	-	-	-	-	-	-	-
32	0	0	0	0	1	0	0	0	0	0
-	-	-	-	-	-	-	-	-	-	-
1023	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 18 is prohibited.

Table.7 Binary 4-bit Swallow Counter Data Setting(AF1 to AF4)

Divide ratio (N)	AF 5	AF 4	AF 3	AF 2	AF 1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
-	-	-	-	-	-
31	1	1	1	1	1

Note: • A<N-2

Table.8 Charge pump current select Bit Setting

CSF	Current value
1	+/-6.0mA
0	+/-1.5mA

Table.9 Spurious cancel Bit Setting

Spurious cancel amount	SC1	SC2
Large	0	0
Midium	0	1
Small	1	0

Table.10 Prescaler Data Setting(SWF)

SWc	Prescaler divide ratio
1	16/17
0	32/33

2)IF synthesizer Data Setting(Integer)

The divide ratio can be calculated using the following equation:

f_{vcoIF}=[(P x N) + A] x fosc / R   (A<N)

fvcoIF :Output frequency of external voltage controlled oscillator(VCO)
P :Preset divide ratio of modlus prescaler(8 or 16)
N :Preset divide ratio of binary 11bit programmable counter(3 to 2047)
A :Preset divide ratio of binary 4 bit swallow counter(0 to 15)
fosc :Output frequency of the reference frequency oscillator
R :Preset divide ratio of binary 14bit reference counter(3 to 16383)

Table11. Binary 14-bit Programmable Reference Counter Data Setting(RC1 to RC14)

Divide ratio (R)	Rc 14	Rc 13	Rc 12	Rc 11	Rc 10	Rc 9	Rc 8	Rc 7	Rc 6	Rc 5	Rc 4	Rc 3	Rc 2	Rc 1
3	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	1	0	0
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table.12 Binary 11-bit Programmable Counter Data Setting (NC1 to NC11)

Divide ratio (N)	Nc 11	Nc 10	Nc 9	Nc 8	Nc 7	Nc 6	Nc 5	Nc 4	Nc 3	Nc 2	Nc 1
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
-	-	-	-	-	-	-	-	-	-	-	-
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 3 is prohibited.

Table.13 Binary 4-bit Swallow Counter Data Setting(AC1 to AC4)

Divide ratio (N)	Ac 4	Ac 3	Ac 2	Ac 1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
-	-	-	-	-
15	1	1	1	1

Note: • A<N

Table. 14 Prescaler Data Setting(SWC)

SWc	Prescaler divide ratio
1	8/9
0	16/17

Table. 15 Charge pump current select Data Setting(CSC)

CSC	Do current
1	+/-6.0mA
0	+/-1.5mA

3)Common setting

Table. 16 LD/fout Output Select Data Setting

LD/fout		LDS	T1	T2
LD output		0	-	-
fout output	fr_{IF}	1	0	0
	fr_{RF}	1	1	0
	fp_{IF}	1	0	1
	fp_{RF}	1	1	1

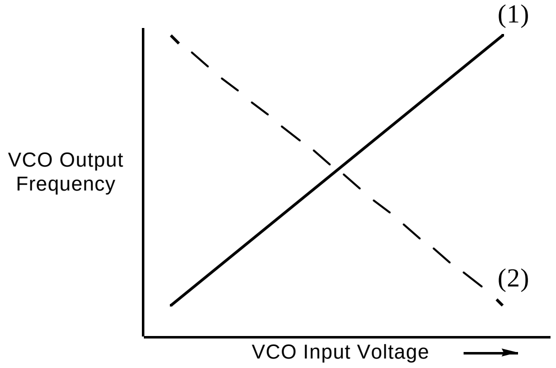
Table. 17 Phase Comparator Phase Switching Data Setting

	$FC_{F/C}$ = H	$FC_{F/C}$ = L
	$Do_{IF,RF}$	
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	1	2

Note:
- Z = High–impedance
- Depending upon the VCO and LPF polarity, FC bit should be set.

When designing a synthesizer, the FC bit setting depends onthe VCO and LPF characteristics

When the LPF and VCO characteristics are similar to (1),
set FC bit" High".
When the VCO characteristics are similar to (2),
set FC bit "Low"



4. Power Saving Mode (Intermittent Mode Control)

Table 18. PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

The intermittent mode control circuit reduces the PLL power consumption.

By setting the PS pin low, the device enters into the power saving mode, reducing the current consumption. See the Electrical Characteristics chart for the specific value.

The phase detector output, Do, becomes high impedance.

For the dual PLL, the lock detector, LD, is as shown in the LD Output Logic table.

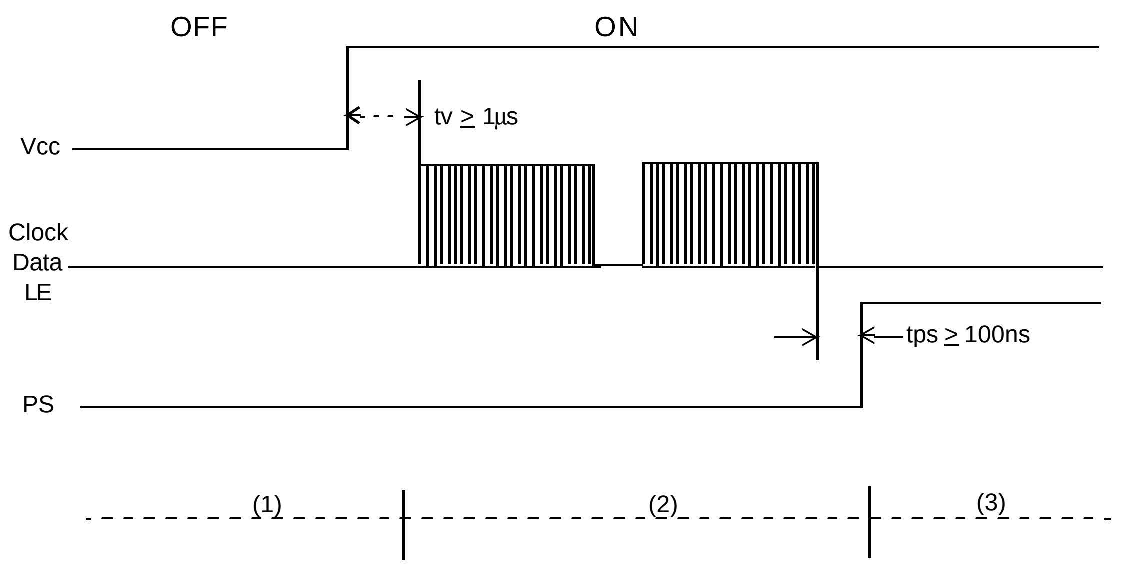
Setting the PS pin high, releases the power saving mode, and the device works normally.

The intermittent mode control circuit also ensures a smooth startup when the device returns to normal operation. When the PLL is returned to normal operation, the phase comparator output signal is unpredictable. This is because of the unknown relationship between the comparison frequency (fp) and the reference frequency (fr) which can cause a major change in the comparator output, resulting in a VCO frequency jump and an increase in lockup time.

To prevent a major VCO frequency jump, the intermittent mode control circuit limits the magnitude of the error signal from the phase detector when it returns to normal operation.

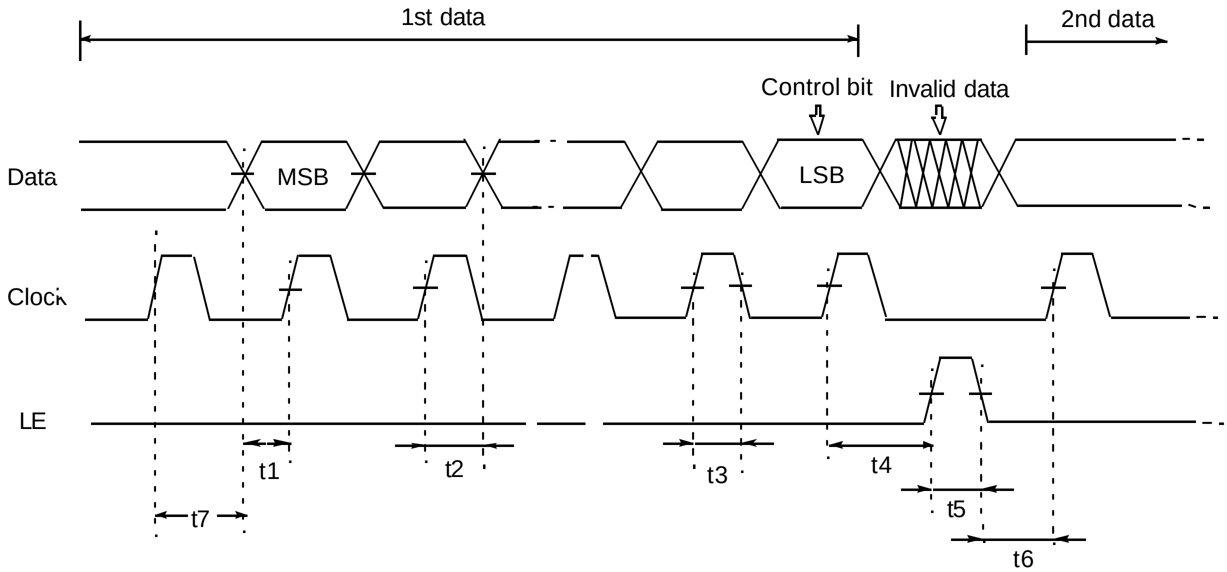
Note: Note: When power (V_{CC}) is first applied, the device must be in standby mode, PS=Low, for at least 1µs.

Note: PS pin must be set at “L” for Power ON.



(1) PS = L (power saving mode) at Power ON
(2) Set serial data at least 1µs after power supply becomes stable(Vcc ≥ 2.2V).
(3) Relase power saving mode (PS: L → H) at least 100ns after setting serial data.

■ SERIAL DATA INPUT TIMING



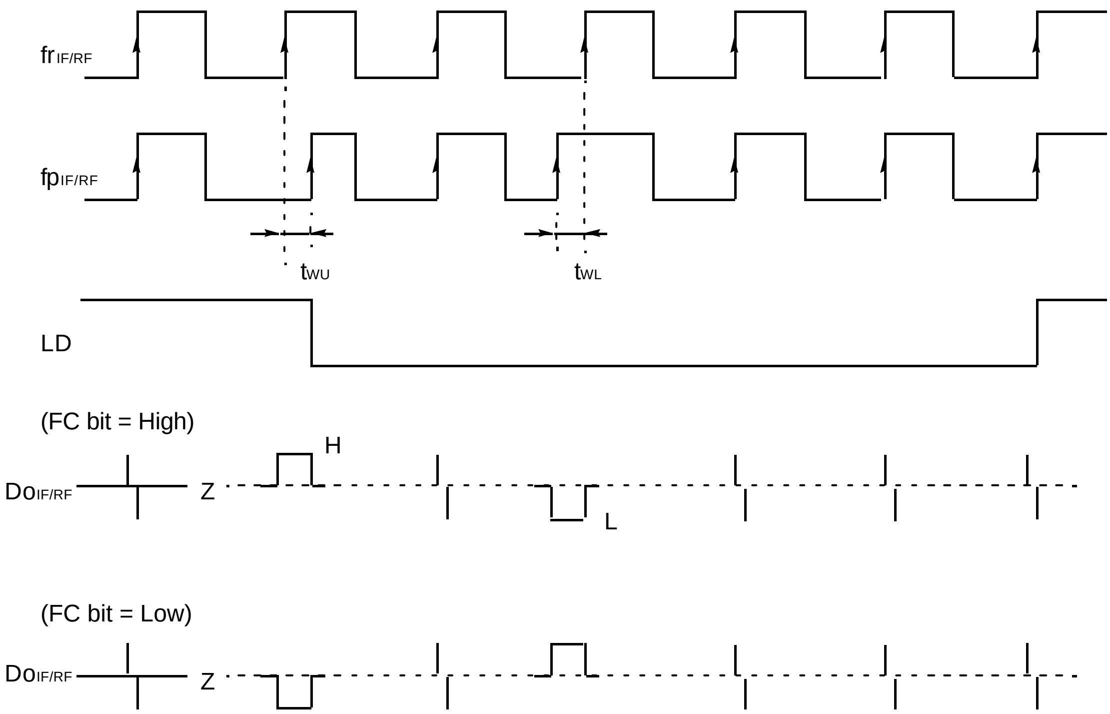
On the rising edge of the clock, one bit of data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	30	–	–	ns

Parameter	Min.	Typ.	Max.	Unit
t5	100	–	–	ns
t6	20	–	–	ns
t7	100	–	–	ns

Note: LE should be "L" when the data is transferred into the shift register.

■ PHASE DETECTOR OUTPUT WAVEFORM

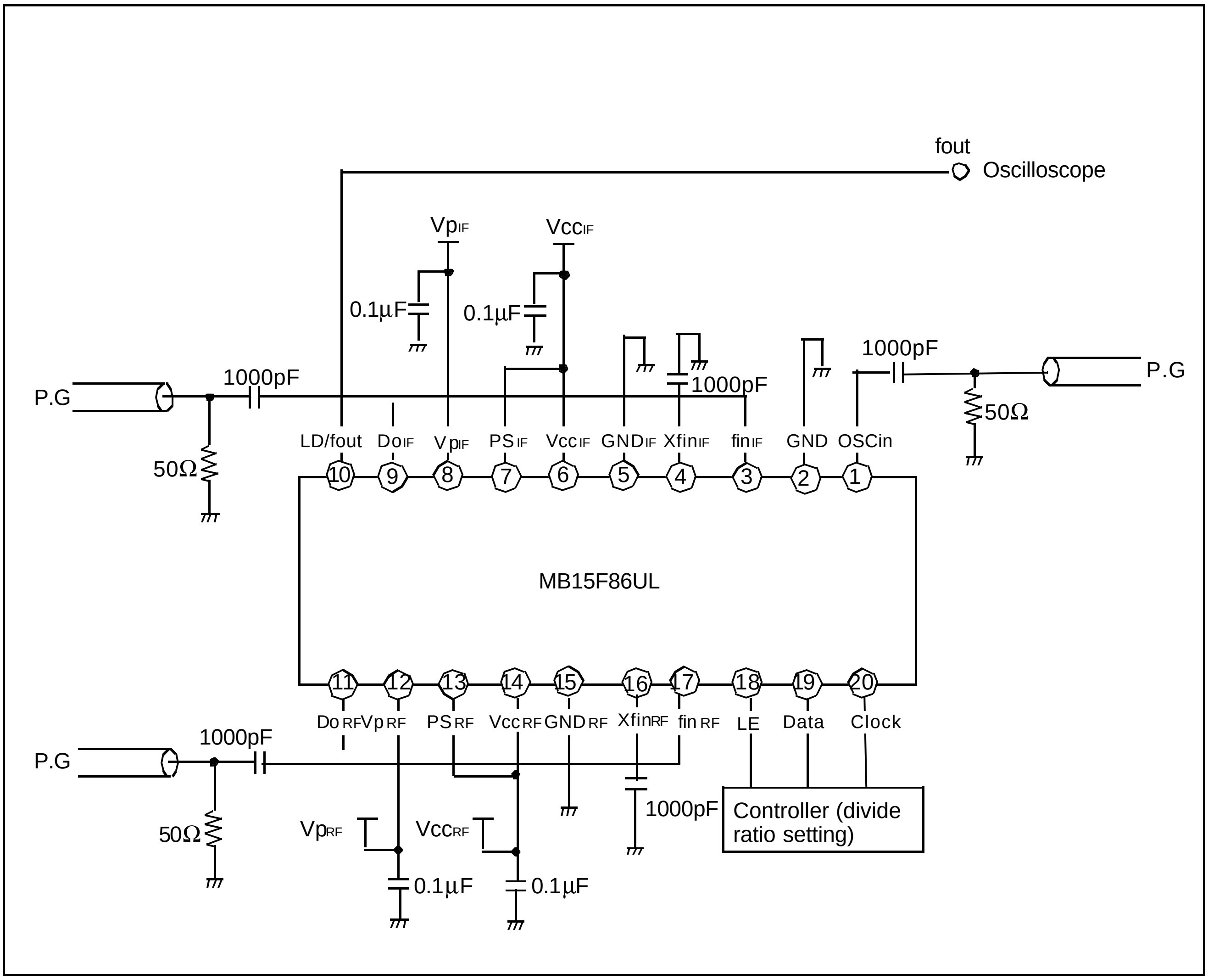


LD Output Logic Table

IF−PLL section	RF−PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

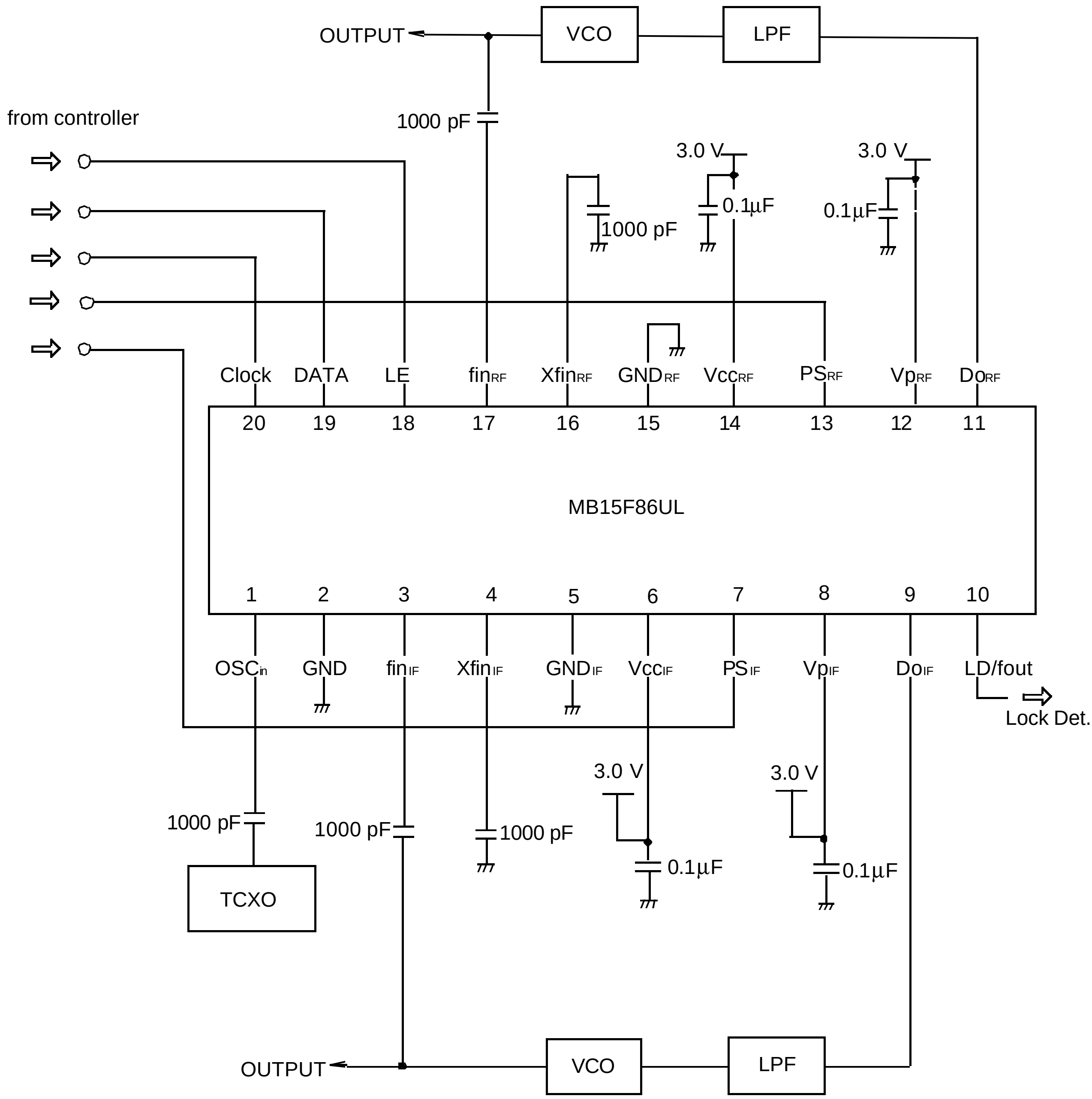
Note:
- Phase error detection range = -2π to $+2\pi$
- Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
- LD output becomes low when phase error is t_{WU} or more.
- LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on OSCin input frequency as follows.
  $t_{WU} \geq$ 2/fosc: i.e. $t_{WU} \geq$ 153.8ns when foscin = 13.0 MHz
  $t_{WL} \leq$ 4/fosc: i.e. $t_{WL} \leq$ 307.7ns when foscin = 13.0 MHz

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



Note : TSSOP-20

■ APPLICATION EXAMPLE



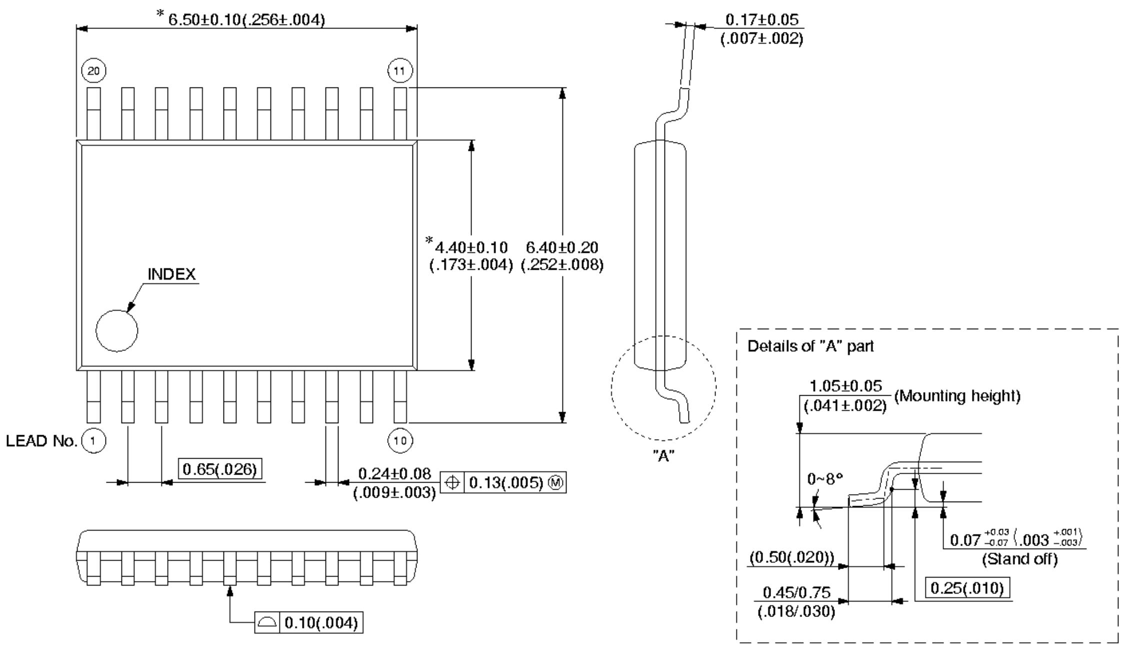
Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

Note :TSSOP-20

■ PACKAGE DIMENSION

20 pin, Plastic SSOP
(FPT-20P-M06)

* : These dimensions do not include resin protrusion.



(Continued)

(Continued)

20 pad, Plastic BCC
(LCC-20P-M05)