NIPPON PRECISION CIRCUITS INC.

SM5166AV

PLL Synthesizer IC

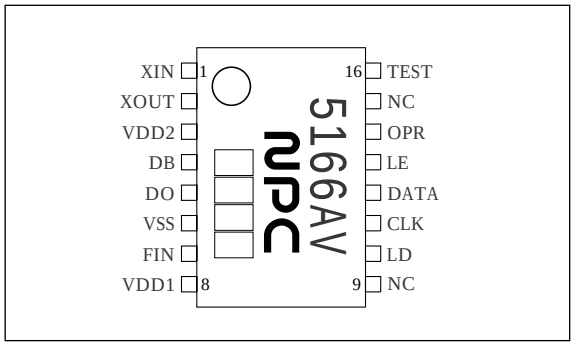
OVERVIEW

The SM5166AV is a PLL synthesizer IC developed for application in pagers and fabricated using NPC's Molybdenum-gate CMOS process. It incorporates independently-controlled reference frequency and operating frequency dividers, and operates from a low-voltage supply to realize low power dissipation. It features a charge pump that operates at 3 V, making possible a wide range of VCO designs.

FEATURES

- Operating frequency
  - f_{FIN} = 100 MHz (V_{DD1} = 1.00 V)
  - f_{FIN} = 90 MHz (V_{DD1} = 0.95 V)
- Reference frequency
  - f_{XIN} = 25 MHz
    (V_{DD1} = 0.95 V, External Input)
  - f_{XIN} = 16 MHz*
    (V_{DD1} = 0.95 V, Internal oscillaton)
    NOTE) * : NPC's recommended frequency.
    Confirm with crystal supplier.
- Unlock signal output pin
- Output circuit for passive filter connection
- −10 to 60 °C operating temperature range
- Standby function for low current consumption
- Boost-up signal output for fast locking
- Supply voltages
  - V_{DD1} = 0.95 to 1.5 V
    (prescaler, counters)
  - V_{DD2} = 2.0 to 3.3 V
    (charge pump)
- 40 to 65528 reference frequency divider ratio range (with 1/8 prescaler built-in) set by serial input data
- 1056 to 65535 operating frequency divider ratio range set by serial input data
- 16-pin VSOP
- Molybdenum-gate CMOS process

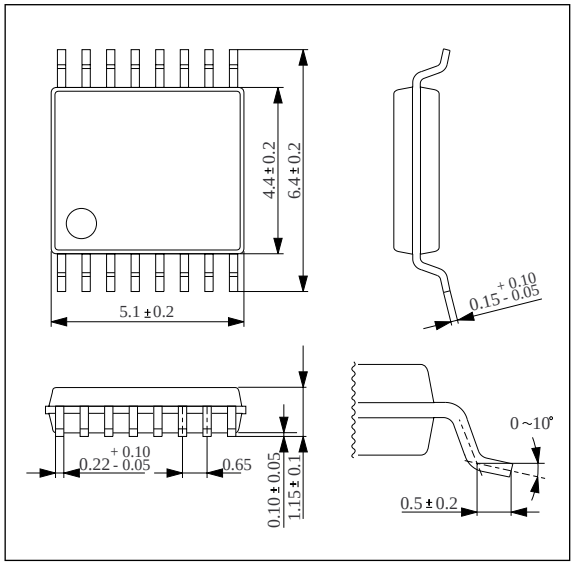
PINOUT(TOP VIEW)



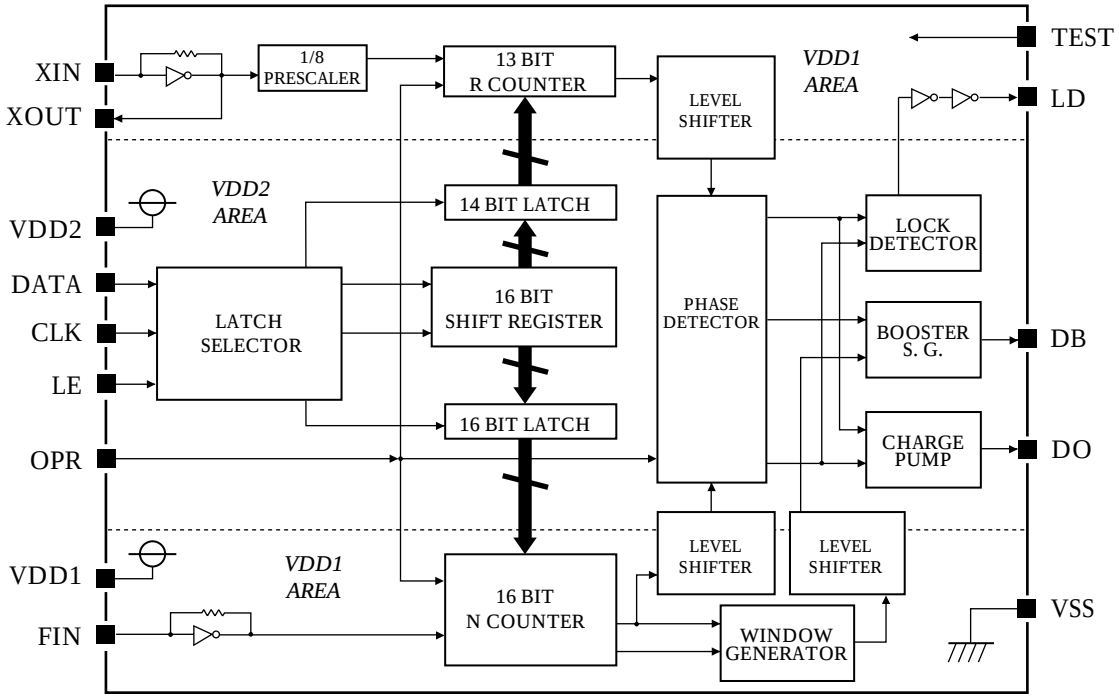
PACKAGE DIMENSIONS

Unit: mm

16-pin VSOP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	XIN	I	Reference frequency divider crystal (oscillator) connection pins. Alternatively, an external clock input can be connected to XIN. The clock is also output on XOUT. Feedback resistor built-in for AC-coupled inputs.
2	XOUT	O	
3	VDD2	–	Phase detector, charge pump and boost-up signal 3 V supply
4	DB	O	boost-up signal output for faster locking
5	DO	O	Phase detector output pin. Built-in charge pump and tristate output means that this output can be connected to a low-pass filter. The output polarity is preset for connection to a passive filter.
6	VSS	–	Ground pin
7	FIN	I	Operating frequency divider input pin. Feedback resistor built-in for AC-coupled inputs.
8	VDD1	–	Reference frequency and operating frequency prescaler and counter 1 V supply
9	NC	–	No connection
10	LD	O	Unlock signal output pin. (Unlocked when HIGH) The function of LD can be turned OFF using the LD input control bit (LD should be tied LOW when not used).
11	CLK	I	Control data clock input pin
12	DATA	I	Control data input pin
13	LE	I	Control data latch enable signal input pin
14	OPR	I	Power-save control pin. Start when HIGH, standby mode when LOW.
15	NC	–	No connection
16	TEST	I	Test pin. Pull-down resistor built-in. Leave open or connect to ground for normal operation.

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Pin name	Rating	Unit
Supply voltage	V_{DD1}	VDD1	–0.3 to 2.0	V
	V_{DD2}	VDD2	–0.3 to 7.0	V
Input voltage range	V_{IN1}	FIN, XIN, TEST	V_{SS} – 0.3 to V_{DD1} + 0.3	V
	V_{IN2}	OPR, CLK, DATA, LE	V_{SS} – 0.3 to V_{DD2} + 0.3	V
Storage temperature range	T_{stg}		–40 to 125	°C
Power dissipation	P_D		150	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD1}		0.95 to 1.5	V
	V_{DD2}		2.0 to 3.3	V
Operating temperature range	T_{opr}		–10 to 60	°C

Electrical Characteristics

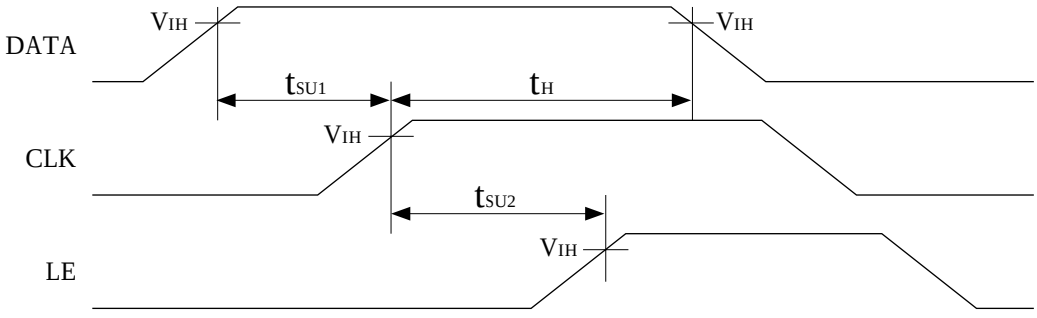
V_{SS} = 0 V, V_{DD1} = 0.95 to 1.5 V, V_{DD2} = 2.0 to 3.3 V, T_a = –10 to 60 °C

Parameter	Symbol	Condition		Rating			Unit
				min	typ	max	
VDD1 operating current consumption	I_{DD1}	Note 1.		–	0.70	1.10	mA
		Note 2.		–	0.75	1.20	
VDD2 standby current	I_{DD2}	Note 3.		–	0.01	10.0	µA
FIN maximum operating input frequency	f_{max1}	300 mVp-p sine wave	V_{DD1} = 0.95 to 1.50 V	90	–	–	MHz
			V_{DD1} = 1.00 to 1.50 V	100	–	–	
XIN maximum operating input frequency	f_{max2}	300 mVp-p sine wave (external input)		25	–	–	MHz
FIN minimum operating input frequency	f_{min1}	300 mVp-p sine wave		–	–	40	MHz
XIN minimum operating input frequency	f_{min2}	300 mVp-p sine wave (external input)		–	–	9	MHz
FIN input amplitude	V_{FIN}	V_{DD1} = 0.95 to 1.50 V, f_{FIN} = 90 MHz, AC coupling		0.3	–	–	Vp-p
		V_{DD1} = 1.00 to 1.50 V, f_{FIN} = 100 MHz, AC coupling		0.3	–	–	
XIN input amplitude	V_{XIN}	f_{XIN} = 25 MHz sine wave, AC coupling (external input)		0.3	–	–	Vp-p
OPR, CLK, DATA, LE LOW-level input voltage	V_{IL}			–	–	0.3	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
OPR, CLK, DATA, LE HIGH-level input voltage	V_{IH}		1.5	–	–	V
FIN LOW-level input current	I_{IL1}	V_{IL} = 0 V	–	–	60	µA
XIN LOW-level input current	I_{IL2}		–	–	10	µA
FIN HIGH-level input current	I_{IH1}	$V_{IH} = V_{DD1}$	–	–	60	µA
XIN HIGH-level input current	I_{IH2}		–	–	10	µA
DO, DB LOW-level output current	I_{OL}	Note 4.	1.0	–	–	mA
DO, DB HIGH-level output current	I_{OH}	Note 5.	1.0	–	–	mA
Tristate output high-impedance leakage current	I_{OZL}	V_{OL} = 0 V	–	–	100	nA
	I_{OZH}	$V_{OH} = V_{DD2}$	–	–	100	nA
DATA → CLK setup time	t_{SU1}	See the timing diagrams.	2	–	–	µs
CLK → LE setup time	t_{SU2}		2	–	–	µs
Hold time	t_H		2	–	–	µs

1. V_{DD1} = 0.95 to 1.05 V, V_{DD2} = 2.7 to 3.3 V, f_{FIN} = 90 MHz (300 mVp-p sine wave), f_{XIN} = 14.4 MHz (300 mVp-p sine wave), OPR = HIGH, no output load
2. V_{DD1} = 1.00 to 1.05 V, V_{DD2} = 2.7 to 3.3 V, f_{FIN} = 100 MHz (300 mVp-p sine wave), f_{XIN} = 14.4 MHz (300 mVp-p sine wave), OPR = HIGH, no output load
3. V_{DD1} = 0 V, V_{DD2} = 2.7 to 3.3 V, OPR = LOW, no input/output load (i.e. CLK = DATA = LE = 0 V)
4. DO and DB outputs are derived from the V_{DD2} supply. V_{DD2} = 2.7 to 3.3 V, V_{OL} = 0.4 V
5. DO and DB outputs are derived from the V_{DD2} supply. V_{DD2} = 2.7 to 3.3 V, $V_{OH} = V_{DD2} - 0.4V$

DATA, CLK, and LE timing



FUNCTIONAL DESCRIPTION

Operating Frequency Divider (N-counter) Structure

The operating frequency divider generates a comparator frequency signal (FV), which is input to the phase comparator, by dividing the VCO signal input on pin FIN.

The operating frequency divider is comprised by dual modulus prescalers, a 5-bit swallow counter and a 11-bit main counter.

The settings for the prescaler (P and P + 1), swallow counter (S) and main counter (M) are related to the comparator frequency divider ratio by:

$$N = (P + 1) \times S + P(M - S)$$
$$= PM + S$$

The counter value ranges are P = 32, P + 1 = 33, S = 0 to 31, and M = 32 to 2047. Therefore, the operating frequency divider ratio range N is 1056 to 65535.

Reference Frequency Divider (R-counter) Structure

The reference frequency divider generates a comparator frequency signal (FR), which is input to the phase comparator, by dividing the reference frequency input either from an external signal on XIN or from a crystal connected between XIN and XOUT.

The reference frequency divider is comprised by a fixed divide-by-8 prescaler and an 13-bit reference counter.

The settings for the prescaler (A = 8) and reference counter (R) are related to the reference frequency divider ratio by:

$$R = AB = 8B$$

The counter value ranges are A = 8 and B = 5 to 8191. Therefore, the reference frequency divider ratio range is R = 40 to 65528.

Input Data

The input data should be specified keeping in mind the V_{DD2} supply. The data is input using CLK, DATA and LE pins into the shift register and latch which operate from the V_{DD2} supply. However, the V_{DD1} supply level can vary.

The control data input uses a 3-line 17-bit serial interface comprising the clock (CLK), data input (DATA) and latch enable (LE). The data is input with the MSB first. The last (17th) bit is used as the latch select control bit. Data is written to the shift register on the rising edge of the clock signal. Accordingly, the data should change state on the falling edge of the clock signal. Data is transferred from the shift register to the latch when the latch enable (LE) signal goes HIGH. Accordingly, the latch enable signal should be held LOW while data is being written to the shift register.

The clock and data input signals are both ignored when the latch enable signal goes HIGH. Also, the CLK, DATA and LE inputs should be tied LOW when not setting data.

Input Data Format

Shift register timing

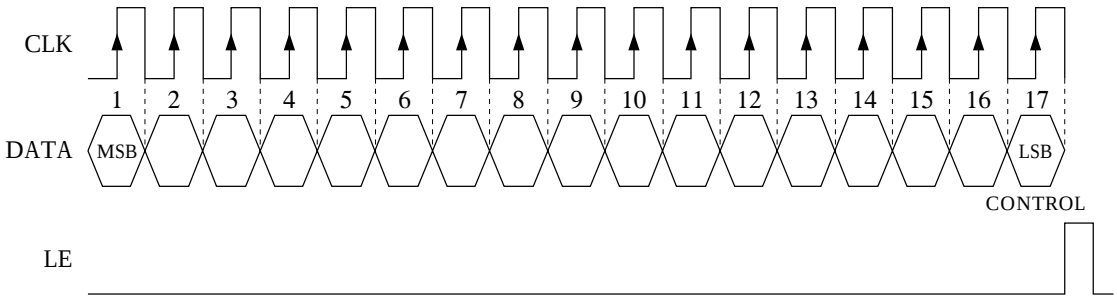


Figure 1. Comparator data format

Latch select

The last (17th) data bit determines the status of the shift register data latch.

Table 1. Latch select bit function

Bit 17	Latch
0	Swallow counter and main counter frequency divider ratio latch select
1	Reference frequency counter divider ratio data and LD output latch select

Swallow counter and main counter frequency divider

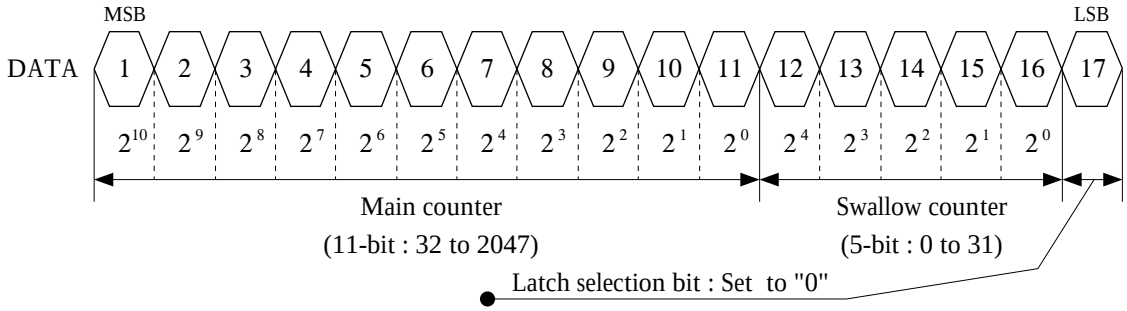


Figure 2. Swallow counter and main counter frequency divider data format

Input data example

If the VCO output (f_{VCO}) is trebled, the output frequency (f_{LO}) is 251.3 MHz, and the channel bandwidth (f_{CH}: operating frequency (f_R) × 3) is 25 kHz, then the comparator frequency divider ratio N is given by:

$$N = \frac{f_{LO}}{f_{CH}} = \frac{f_{VCO} \times 3}{f_R \times 3} = \frac{251.3/3}{0.025/3} = 10052 = 32 \times 314 + 4$$

Therefore, the swallow counter count is 4 $(00100)_2$ and the main frequency divider counter count is 314 $(0000100111010)_2$. The input data format is shown in figure 3.

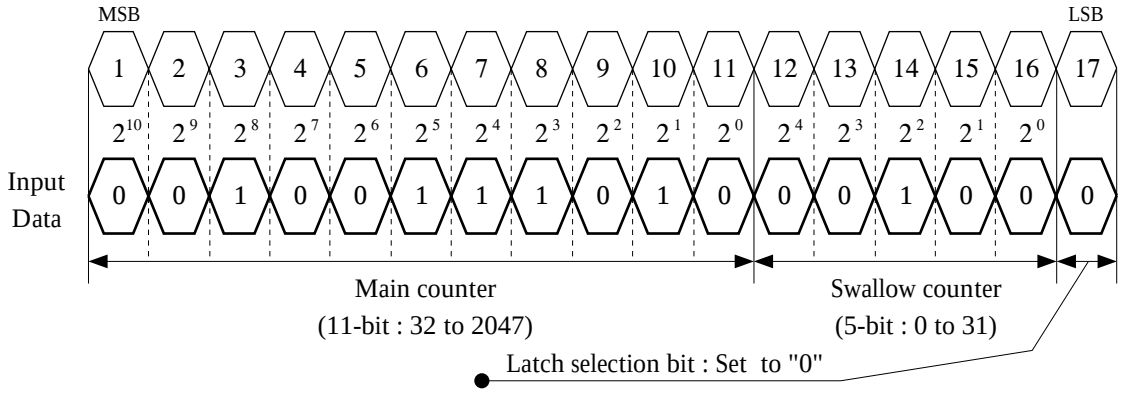


Figure 3. Swallow counter and main counter frequency divider data example

Reference counter frequency divider setting

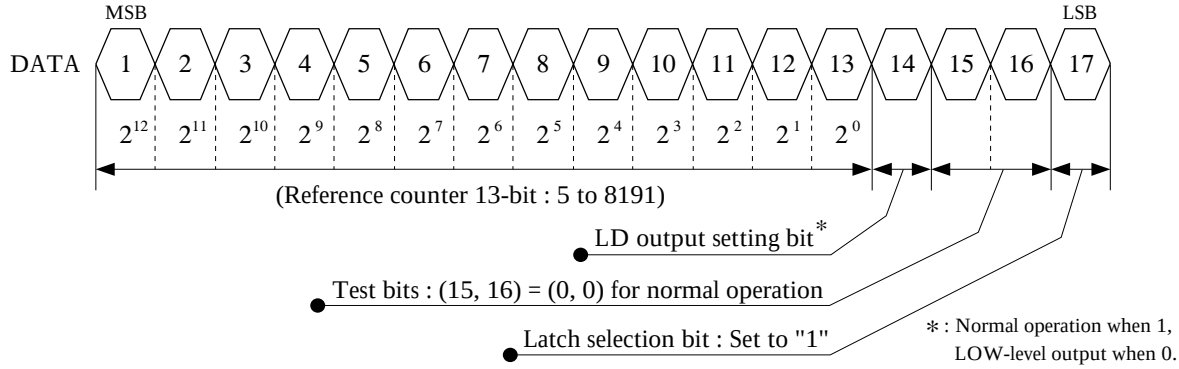


Figure 4. Reference counter data and LD output setting format

Input data example

If the VCO output (f_{VCO}) is trebled, the crystal frequency is 12.8 MHz and the channel bandwidth (f_{CH}: comparator frequency (f_R) × 3) is 25 kHz, then the reference frequency divider ratio R is given by:

$$NR = \frac{Xtal}{f_{CH}} = \frac{Xtal}{f_R \times 3} = \frac{12.8}{0.025/3} = 1536 = 8 \times 192$$

Therefore, the reference counter count is 192 $(00011000000)_2$. The input data format is shown in figure 5.

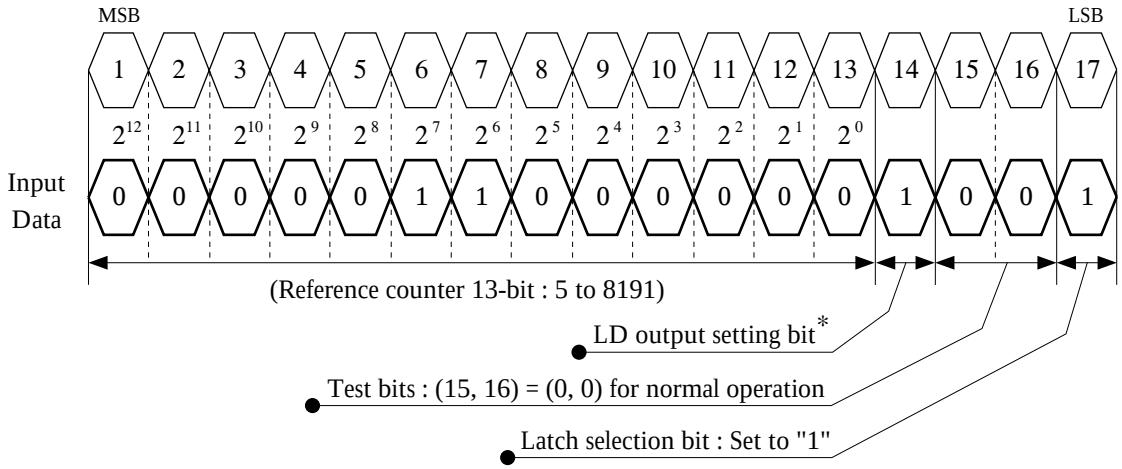


Figure 5. Reference counter data and LD output setting example

Boost-up Signal

If the PLL momentarily loses lock as a result of a phase error, a level signal is output on pin DB. When the PLL is operating in lock, output DB goes high impedance.

When the PLL starts up, the signal on DB charges the low-pass filter capacitor in anticipation of high-speed locking. After the boost-up signal is output and the PLL phase error comes within tolerance, the boost-up circuit stops and operation continues when the 2 supplies (V_{DD1}, V_{DD2}) are applied and OPR goes HIGH once only. After the boost-up circuit stops, new data is written and the boost-up signal is not output even if the VCO is not in lock.

Operating principles

When the PLL is operating with a phase error within fixed tolerance, an internal WINDOWN signal is generated, as shown in figure 6. This signal is in sync with the N counter output signal (FV) and is 64 cycles of the FIN input period in length centered about the falling edge of FV.

If the phase detector error correction signal occurs before the WINDOWN LOW-level pulsewidth, the HIGH-level output from DB continues. However, if the error correction signal occurs wholly within the WINDOWN LOW-level pulsewidth, DB goes high impedance and the boost-up circuit operation stops.

The above description applies when the error correction signal is revising up. When the error correction signal is revising down, DB goes LOW.

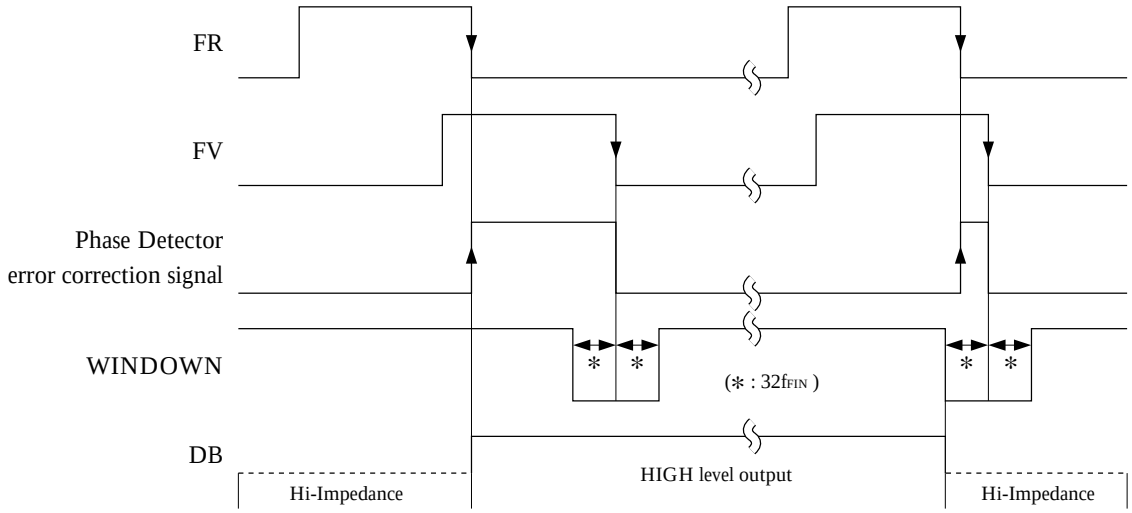


Figure 6. boost-up signal timing

Standby Mode

The SM5166AV enters standby mode when OPR goes LOW. In this mode, the states and functions shown in table 2 occur.

In standby mode, some current flows into VDD1 (FIN and XIN prescaler current). Therefore, it is necessary to reduce V_{DD1} to 0 V to fully reduce current consumption and reduce power dissipation.

Table 2. Standby mode block states

Block	State
DO and DB	Floating (high impedance)
LD	LOW-level output
Phase comparator	Reset
Input FIN	Feedback resistor is cutoff (HIGH level)
Input XIN	Feedback resistor is cutoff (HIGH level)
N counter	Reset
R counter	Reset
Latch data	Stored (while V_{DD2} is within rating)

Phase Comparator Timing Diagram

The DO output circuit polarity is configured for connection to an external passive filter.

The signals compared are FV and FR, which are the internal operating frequency divider output signal and reference frequency divider output signal, respectively.

The timing and passive filter basic structure are shown in figures 7 and 8, respectively.

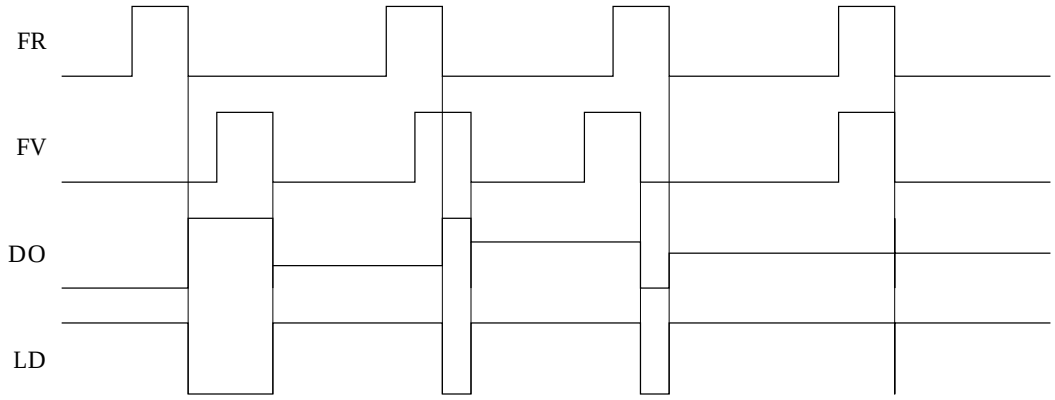


Figure 7. Phase detector timing

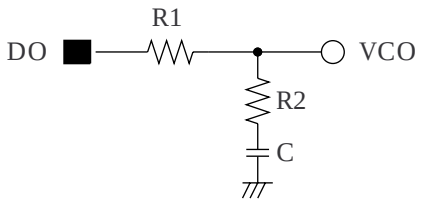


Figure 8. Passive filter

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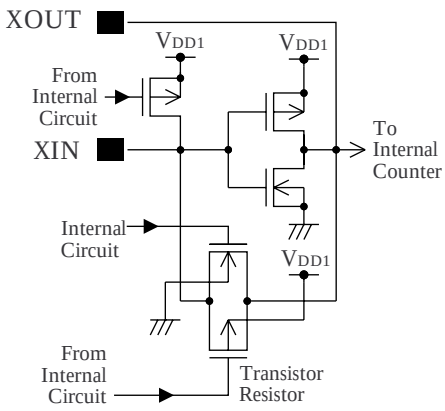
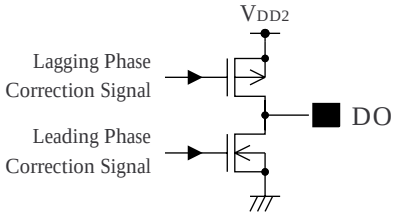
INPUT/OUTPUT EQUIVALENT CIRCUITS

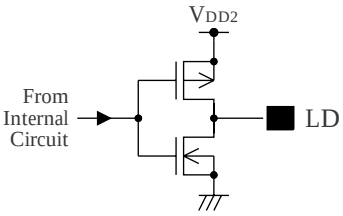
XIN, XOUT



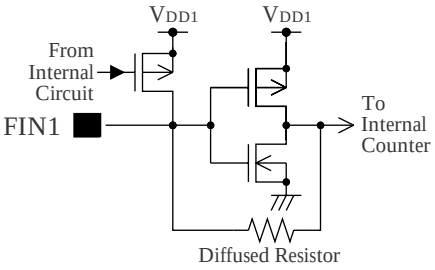
DO



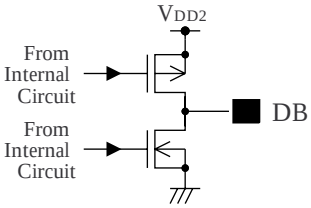
LD



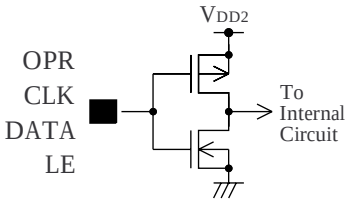
FIN



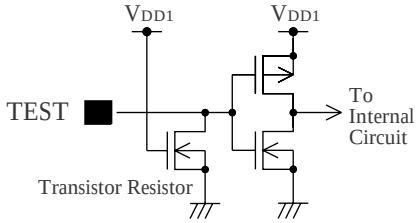
DB



OPR, CLK, DATA, LE



TEST



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