Fujitsu

MBF200
## Solid State Fingerprint Sensor

▶ Overview

The Fujitsu MBF200 Solid-State Fingerprint Sensor is a direct contact, fingerprint acquisition device. It is a high performance, low power, low cost, capacitive sensor composed of a two-dimensional array of metal electrodes in the sensing array. Each metal electrode acts as one plate of a capacitor and the contacting finger acts as the second plate. A passivation layer on the device surface forms the dielectric between these two plates. Ridges and valleys on the finger yield varying capacitor values across the array, and the resulting varying discharge voltages are read to form an image of the fingerprint.

The MBF200 is manufactured in standard CMOS technology. The 256 X 300 sensor array has a 50 µm pitch and yields a 500-dpi image. The sensor surface is protected by a patented, ultra-hard, abrasion and chemical resistant coating.

Packages

▶ Features

- Capacitive solid-state device
- 500-dpi resolution (50 µm pitch)
- 1.28 cm x 1.50 cm (0.5"x 0.6") sensor area
- 256 x 300 sensor array
- Smart Cards
- 3.3V to 5V operating range
- Exceptionally hard protective coating
- Integrated 8-bit analog to digital converter
- One of three bus interfaces:
  8-bit microprocessor bus interface
  Integrated USB Full-Speed Interface
  Integrated Serial Peripheral Interface
- Standard CMOS technology
- Low power, less than 70 mW operating at 5V
- Automatic finger detection
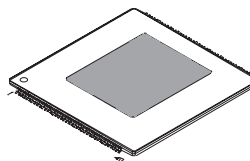
Applications

- Secure access for databases, networks, local storage
- Portable fingerprint acquisition
- Smart Cards
- Identity verification for ATM transactions
- Cellular phone-based security access
- Access control and monitoring (home, auto, office, etc.)

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Chip Operation

The sensor array includes 256 columns and 300 rows of sensor plates. Associated with each column are two sample-and-hold circuits. A fingerprint image is sensed or captured one row at a time. This "row capture" occurs in two phases. In the first phase, the sensor plates of the selected row are pre-charged to the VDD voltage. During this pre-charge period, an internal signal enables the first set of sample-and-hold circuits to store the pre-charged plate voltages of the row.

In the second phase, the row of sensor plates is discharged with a current source. The rate at which a cell is discharged is proportional to the "discharge current." After a period of time (referred to as the "discharge time"), an internal signal enables the second set of sample-and-hold circuits to store the final plate voltages. The difference between the precharged and discharged plate voltages is a measure of the capacitance of a sensor cell. After the row capture, the cells within the row are ready to be digitized.

The sensitivity of the chip is adjusted by changing the discharge current and discharge time. The nominal value of the current source is controlled by an external resistor connected between the ISET pin and ground. The current source is controlled from the Discharge Current Register (DCR). The discharge time is controlled by the Discharge Time Register (DTR).

Block Diagram
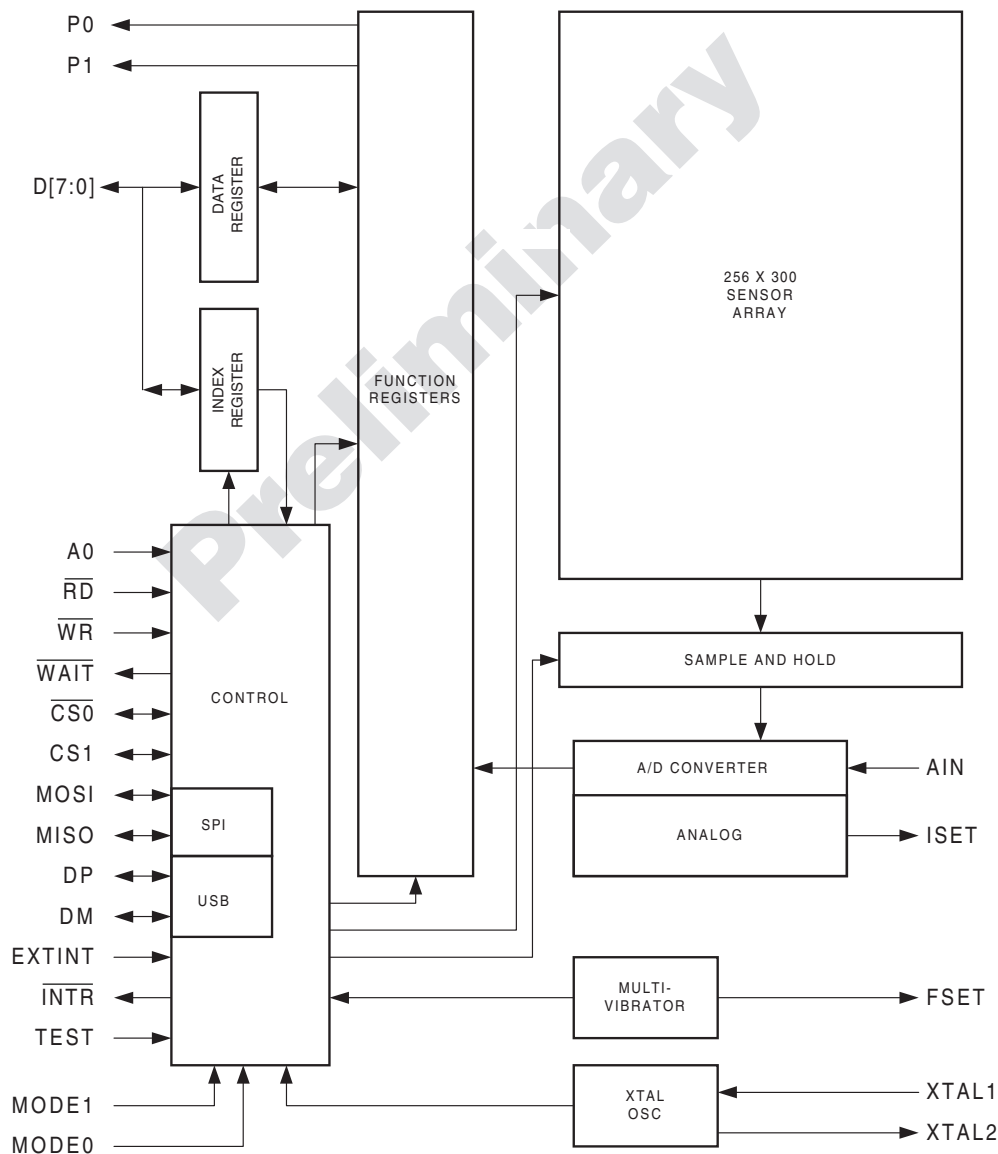
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Connection Diagram

Left Pin	No.		No.	Right Pin
VDDA1	1		80	N/C
VSSA1	2		79	N/C
ISET	3		78	N/C
AIN	4		77	N/C
FSET	5		76	N/C
VSSA2	6		75	N/C
VDDA2	7		74	N/C
TEST	8		73	N/C
P0	9		72	N/C
P1	10		71	N/C
D7	11		70	N/C
D6	12		69	N/C
D5	13		68	N/C
D4	14		67	N/C
VSS1	15		66	N/C
VDD1	16		65	N/C
D3	17		64	N/C
D2	18		63	N/C
D1	19		62	N/C
D0	20		61	N/C
A0	21		60	N/C
$\overline{RD}$	22	MBF200	59	N/C
$\overline{WR}$	23		58	N/C
VSS2	24		57	N/C
VDD2	25		56	N/C
XTAL2	26		55	N/C
XTAL1	27		54	N/C
$\overline{INTR}$	28		53	N/C
$\overline{WAIT}$	29		52	N/C
EXTINT	30		51	N/C
CS1/SCLK	31		50	N/C
$\overline{CS0/SCS}$	32		49	N/C
MOSI	33		48	N/C
MISO	34		47	N/C
MODE1	35		46	N/C
MODE0	36		45	N/C
DM	37		44	N/C
DP	38		43	N/C
VDD3	39		42	N/C
VSS3	40		41	N/C

Preliminary

Pin List

Pin Number	Name	Type	IOL (5.0 V)	IOH (5.0 V)	Description
1	VDDA1	PWR			Analog Power Supply
2	VSSA	GND			Analog Ground
3	ISET	O			Sets Reference Current
4	AIN	I			Analog Input
5	FSET	O			Sets Internal Multi-vibrator Frequency
6	VSSA2	GND			Analog Ground
7	VDDA2	PWR			Analog Power Supply
8	TEST	I			Test Mode Enable
9	P0	O	8mA	4mA	Output Port 0
10	P1	O	8mA	4mA	Output Port 1
11	D7	I/O	8mA	4mA	Data Bit 7
12	D6	I/O	8mA	4mA	Data Bit 6
13	D5	I/O	8mA	4mA	Data Bit 5
14	D4	I/O	8mA		Data Bit 4
15	VSS1	GND			Digital Ground
16	VDD1	PWR			Digital Power Supply
17	D3	I/O	8mA	4mA	Data Bit 3
18	D2	I/O	8mA	4mA	Data Bit 2
19	D1	I/O	8mA	4mA	Data Bit 1
20	D0	I/O	8mA	4mA	Data Bit 0
21	A0	I			Address Input
22	$\overline{RD}$	I	8mA	4mA	Read Enable, Active Low
23	$\overline{WR}$	I	8mA	4mA	Write Enable, Active Low
24	VSS2	GND			Digital Ground
25	VDD2	PWR			Digital Power Supply
26	XTAL2	O			Internal Oscillator Output
27	XTAL1	I			Internal Oscillator Input
28	$\overline{INTR}$	O	8mA		Interrupt Output, Active Low
29	$\overline{WAIT}$	O	8mA		Wait, Active Low
30	EXTINT	I			External Interrupt Input
31	CS1/SCLK	I/O			Chip Select, Active High
32	$\overline{CS0}/\overline{SCS}$	I/O			Chip Select, Active Low
33	MOSI	I/O	8mA	4mA	SPI Master Output / Slave Input
34	MISO	I/O	8mA	4mA	SPI Master Input / Slave Output
35	MODE1	I			Mode Select 1
36	MODE0	I			Mode Select 0
37	DM	I/O			USB D-
38	DP	I/O			USB D+
39	VDD3	PWR			Digital Power Supply
40	VSS3	GND			Digital Ground
[41:80]	N/C				No Connect

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Pin Descriptions

VDDA1, VDDA2 (Pins 1 and 7)

Power Supply to the analog section of the sensor. VDDA1 powers the array, row drivers, column receivers, A/D converter, and sample/hold amplifier. VDDA2 powers the multi-vibrator and bias circuits.

VSSA1, VSSA2 (Pins 2 and 6)

Ground for the analog section of the sensor. VSSA1 is the ground return for the array, row drivers, column receivers, A/D converter, and sample hold amplifier. VSSA2 is the ground return for the multi-vibrator and bias circuits.

VDD1, VDD2, VDD3 (Pins 25, 16, and 39)

Power supply to the digital logic and I/O drivers. VDD2 powers the core digital logic, oscillators, phase-locked loops, and digital inputs. VDD1 and VDD3 supply power to the digital output circuits and USB transceivers.

VSS1, VSS2, VSS3 (Pins 24, 15, and 40)

Ground for the digital logic and I/O drivers.

VSS2 is the ground connection for the core digital logic, oscillators, phase-locked loops, and digital inputs. VSS1 and VSS3 are the ground connections for the digital outputs and USB transceivers.

ISET (Pin 3)

Connect a 200k ohm resistor between ISET and analog ground VSSA1 to set the internal reference current. The discharge current is a scalar function of the internal reference current.

AIN (Pin 4)

Alternate analog input to the A/D converter. Set the AINSEL bit in register CTRLA to select AIN as the input to the A/D converter. Pull this pin to ground, preferably with a resistor.

FSET (Pin 5)

Connect a resistor between FSET and ground to set the internal multi-vibrator and automatic finger detection frequency. Use a 56k ohm resistor for standard 12 MHz (±20%) multi-vibrator operation and 120KHz (±20%) automatic finger detection sampling rate.

XTAL1 (Pin 27)

Input to the internal oscillator. To use the internal oscillator, connect a crystal circuit to this pin. If an external oscillator is used, connect its output to this pin.

XTAL2 (Pin 26)

Output from the internal oscillator. To use the internal oscillator, connect a crystal circuit to this pin. If an external oscillator is used, leave this pin unconnected.

D[7:0] (Pins 11-14, 17-20)

Bi-directional data bus. D[7:0] have weak latches that hold the bus's state when not being driven. These pins may be left unconnected in SPI or USB mode.

A0 (Pin 21)

Address input. Drive A0 low to select the address index register. Drive A0 high to select the data buffer. A0 has a weak latch that holds the pin state when not being driven. This pin may be left unconnected in SPI or USB mode.

$\overline{\text{RD}}$ (Pin 22)

Read enable, active low. To read from the chip, drive $\overline{\text{RD}}$ low while $\overline{\text{WR}}$ is high and the chip is selected. $\overline{\text{RD}}$ has an internal, weak pull-up resistor and may be left unconnected in SPI or USB mode.

$\overline{\text{WR}}$ (Pin 23)

Write enable, active low. To write to the chip, drive $\overline{\text{WR}}$ low while $\overline{\text{RD}}$ is high and the chip is selected. $\overline{\text{WR}}$ has an internal, weak pull-up resistor and may be left unconnected in SPI or USB mode.

$\overline{\text{CS0}}$ / $\overline{\text{SCS}}$ (Pin 32)

Chip select, active low. The $\overline{\text{CS0}}/\overline{\text{SCS}}$ pin has a weak latch that holds the pin's state when not being driven. $\overline{\text{CS0}}/\overline{\text{SCS}}$ may be left unconnected in USB mode if not using an external serial ROM. The function of the $\overline{\text{CS0}}/\overline{\text{SCS}}$ pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)
$\overline{\text{CS0}}/\overline{\text{SCS}}$ functions as an active-low chip select input. Drive $\overline{\text{CS0}}/\overline{\text{SCS}}$ low while CS1 is high to select the chip.

MODE[1:0] = 01b (SPI Slave Mode)
$\overline{\text{CS0}}/\overline{\text{SCS}}$ functions as an active-low slave chip select input. Connect a pull-up resistor between $\overline{\text{CS0}}/\overline{\text{SCS}}$ and VDD.

MODE[1:0] = 10b (USB Interface Mode, Using Internal ROM)
$\overline{\text{CS0}}/\overline{\text{SCS}}$ has no function.

MODE[1:0] = 11b (USB Interface Mode, Using External ROM)
$\overline{\text{CS0}}/\overline{\text{SCS}}$ functions as the master chip select output, active low to the slave serial ROM chip select. Connect a pullup resistor between $\overline{\text{CS0}}/\overline{\text{SCS}}$ and VDD.

CS1 / SCLK (Pin 31)

Chip select, active high. The CS1/SCLK pin has a weak latch that holds the pin's state when not being driven. CS1/SCLK may be left unconnected in USB mode if not using an external serial ROM. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)
CS1/SCLK functions as an active-high chip select input. Drive CS1/SCLK high while CS0-/CSC- is low to select the chip.

MODE[1:0] = 01b (SPI Slave Mode)
CS1/SCLK functions as the slave serial clock input.

MODE[1:0] = 10b (USB Interface Mode, Using Internal ROM)
CS1/SCLK has no function.

MODE[1:0] = 11b (USB Interface Mode, Using External ROM)
CS1/SCLK functions as the master serial clock output to the slave serial ROM clock input. Connect a pull-up resistor between CS1/SCLK and VDD.

EXTINT (Pin 30)

External Interrupt input. This pin can be programmed to be edge or level sensitive, active-high or active-low. EXTINT has a weak pull-up and may be left unconnected in MCU, SPI, or USB mode.

$\overline{\text{INTR}}$ (Pin 28)

Interrupt output, active low. $\overline{\text{INTR}}$ is high impedance when it is not active and is driven low when an enabled interrupt event occurs. $\overline{\text{INTR}}$ can be enabled if the sensor is in MCU or SPI mode. In USB mode leave this pin unconnected.

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$\overline{\text{WAIT}}$ (Pin 29)

Wait output, active low. $\overline{\text{WAIT}}$ is driven low when active and high-impedance when not active. $\overline{\text{WAIT}}$ goes low if the A/D converter is read while an A/D conversion is in progress. $\overline{\text{WAIT}}$ will remain low until the A/D conversion is completed.

MOSI (Pin 33)

SPI Master Output/Slave input. The MOSI pin has a weak latch that holds the pin's state when not being driven. MOSI may be left unconnected in MCU mode or USB mode if not using an external serial ROM. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)
MOSI has no function.

MODE[1:0] = 01b (SPI Slave Mode)
MOSI functions as the slave serial input.

MODE[1:0] = 10b (USB Interface Mode, Using Internal ROM)
MOSI has no function.

MODE[1:0] = 11b (USB Interface Mode, Using External ROM)
MOSI functions as the master serial data output to the slave serial ROM data input. Unlike standard SPI, MOSI is actively driven high and low when transmitting data and is high impedance when idle. Connect a pull-up resistor between MOSI and VDD to pull MOSI high when idle.

MISO (Pin 34)

SPI Master Input/Slave Output. The MISO pin has a weak latch that holds the pin's state when not being driven. MISO may be left unconnected in MCU mode or USB mode if not using an external serial ROM. The function of this pin depends on the MODE1 and MODE0 pins.

MODE[1:0] = 00b (Microprocessor Bus Interface Mode)
MISO has no function.

MODE[1:0] = 01b (SPI Slave Mode)
MISO functions as the slave serial data output. Unlike standard SPI, the MISO connection is actively driven high and low when transmitting data and is high impedance when idle. Connect a pull-up resistor between MISO and VDD to pull MISO high when idle.

MODE1/MODE0 = 10b (USB Interface Mode, Using Internal ROM)
MISO has no function.

MODE1/MODE0 = 11b (USB Interface Mode, Using External ROM)
MISO functions as the master serial data input from the slave serial ROM data output.

P0 (Pin 9)

Port Output 0. This output is controlled by bit 0 of the CTRLC register.

P1 (Pin 10)

Port Output 1. This output is controlled by bit 1 of the CTRLC register.

DP (Pin 38)

USB D+ data line. In USB mode, connect a 1.5k ohm resistor between DP and VDD3, which must be between 3.3V and 3.6V in this mode. Use a 43 ohm series resistor. In MCU or SPI mode, either pull-up this pin with a resistor or tie it to ground.

DM (Pin 37)

USB D- data line. Use 43 ohm series resistor. In MCU or SPI mode, either pull-up this pin with a resistor or tie it to ground.

MODE[1:0] (Pins 35 and 36)

Mode Select pins. MODE[1:0] select one of four operating modes.

MODE[1:0]	Description
00b	Microprocessor Bus Mode
01b	SPI Bus Mode
10b	USB Mode, Using Internal ROM
11b	USB Mode, Using External ROM

TEST (Pin 8)

Test Mode Enable. It is intended for factory use only. Connect this pin to VSS.

No Connect (Pins 41-80)

Unconnected pins.

Device Bus Operation

Microprocessor Bus Interface

The microprocessor bus interface mode uses the following pins: D[7:0], A0, $\overline{RD}$, $\overline{WR}$, $\overline{CS0}$, CS1, EXTINT, $\overline{INTR}$, and $\overline{WAIT}$. Either the internal multi-vibrator or the XTAL1/XTAL2 oscillator can be selected to provide the clock to the chip. The SPI and USB interfaces are disabled.

The fingerprint sensor chip uses an indexed addressing scheme to access its function registers. The chip has eight data lines (D[7:0]) and one address line (A0). The address line selects between the index register and the data register. Drive A0 low to select the index register. Drive A0 high to access the function register selected by the index register. The index register retains its value until it is rewritten or the chip is reset.

The chip has four control inputs: $\overline{CS0}$, CS1, $\overline{RD}$, and $\overline{WR}$. Drive $\overline{CS0}$ low and CS1 high to select the chip. Data is latched on the rising edge of WR-.

The chip has two status lines: $\overline{INTR}$ and $\overline{WAIT}$. The $\overline{INTR}$ signal is asserted when an interrupt event occurs. The $\overline{WAIT}$ signal goes low when the A/D converter is read while an A/D conversion is in progress. The $\overline{WAIT}$ signal will be high impedance when the A/D conversion is completed. Both the $\overline{WAIT}$ and $\overline{INTR}$ outputs are high impedance when they are not active. As a result, they can be active-low WIRE-ORed in conjunction with other interrupts or wait signals.

The SPI and USB interfaces are disabled when the microprocessor bus interface is selected. A truth table for the microprocessor bus interface is shown below:

Truth Table for the Microprocessor Bus Interface

$\overline{CS0}$	CS1	A0	$\overline{RD}$	$\overline{WR}$	Mode	Data Lines
H	X	X	X	X	De-selected	High Impedance
X	L	X	X	X	De-selected	High Impedance
L	H	X	H	H	Standby	High Impedance
L	H	L	L	H	Read Index Register	Output
L	H	L	H	L	Write Index Register	Input
L	H	H	L	H	Read Data Register	Output
L	H	H	H	L	Write Data Register	Input

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Serial Peripheral Bus Interface (SPI) Slave

SPI Bus Mode

SPI (Slave) bus mode uses the following pins: SCLK, $\overline{\text{SCS}}$, MOSI, MISO, and EXTINT. Either the internal multivibrator or the XTAL1/XTAL2 oscillator can be selected to provide the clock to the chip. The microprocessor bus and USB interface are disabled.

SPI Slave Mode

In SPI Slave Mode, the sensor can operate in either SPI mode (0, 0) where CPOL = 0 and CPHA = 0 or SPI mode (1, 1) where CPOL = 1 and CPHA = 1. The SPI Master may clock in commands and clock out data up to 12 Mbits per second. The SPI Master can write and read the registers of the sensor even when the internal 12 MHz multivibrator or XTAL1/XTAL2 oscillator is halted.

- MOSI bits are sampled on the rising edge of SCK

- MISO bits change on the falling edge of SCK

- SCK can be idle in either a high or low state

- The most significant bits are shifted out first

Register Read Command in SPI Slave Mode

The Register Read command includes a command byte and address byte. The command sequence begins when the SPI master drives $\overline{\text{SCS}}$ low and sends the Read Command byte (encoded as 0x03) on the MOSI pin. Following the command byte, the master sends the address byte, which is the index to the register to be read. After receiving the least significant bit (LSB) of the address byte, the SPI slave sensor sends the contents of the selected register on the MISO pin. Finally, the master drives $\overline{\text{SCS}}$ high after it has sampled the LSB of the data byte. When reading the A/D converter, the Master may keep $\overline{\text{SCS}}$ low to read consecutive pixels up to the end of the current row. A new Register Read command must be issued to read the next row. The SPI Master must drive $\overline{\text{SCS}}$ high before beginning another command.

Register Write Command for SPI Slave Mode

The Register Write command includes a command byte and address byte followed by the data to be written. The command sequence begins when the SPI Master drives $\overline{\text{SCS}}$ low and sends the Write Command byte (encoded as 0x02) on the MOSI pin. Then the master sends the address byte, which is the index to the register to be written. Finally, the master sends the data byte and thereafter drives $\overline{\text{SCS}}$ high.

USB Interface Mode, Using Internal ROM

This USB mode uses the following pins: DP, DM, EXTINT, XTAL1, and XTAL2. XTAL1 must be driven from a 12 MHz source or XTAL1 and XTAL2 must be connected to a 12 MHz crystal circuit. The internal 12 MHz multivibrator, the microprocessor bus, and SPI interface are disabled. The internal USB descriptor ROM will be accessed in response to a USB GET_DESCRIPTOR command.

The sensor's USB interface uses three endpoints:

Endpoint 0

Endpoint 0 is a control endpoint used for device enumeration and configuration. The sensor function registers are written and read using control transfers of vendor specific commands to endpoint 0.

Endpoint 1

Endpoint 1 is a bulk-in endpoint specifically for reading the CTRLA register, which is the output buffer of the A/D converter. Data is transmitted in 64-byte packets except for the last packet of a GETROW operation which may be 64-bytes or less, depending on the row length.

Endpoint 2

Endpoint 2 is an interrupt endpoint. In the event of an interrupt, the contents of the ISR (Interrupt Status Register) are transfered to endpoint 2.

USB Interface Mode, Using External ROM

This USB mode the uses following pins: DP, DM, SCLK, $\overline{\text{SCS}}$, MOSI, MISO, EXTINT, XTAL1, and XTAL2. XTAL1 must be driven from a 12 MHz source or a 12 MHz crystal circuit must be connected to XTAL1 and XTAL2. The internal 12 MHz multivibrator and the microprocessor bus are disabled.

The SPI interface is enabled as an SPI Master. The external SPI serial ROM will be accessed in response to a USB GET_DESCRIPTOR command. The internal USB descriptor ROM is disabled. This mode allows an external serial ROM to override the internal descriptor ROM.

Note: When the MBF200 is directly connected to USB in either of the modes above, the VDD and VDDA pins must be powered between 3.3V and 3.6V so that the MBF200 DP and DM pins do not drive the USB beyond 3.6V.

SPI Master Mode

In SPI Master Mode the sensor operates in SPI mode (1,1) where CPOL = 1, and CPHA = 1. SCK is limited to 1 MHz.

- MOSI bits change on the falling edge of SCK

- MISO bits are sampled on the rising edge of SCK

- SCK is idle in the high state

- The most significant bits are shifted out first

Function Register Descriptions

The function registers are accessed by indexed addressing. Write the index register to select a function register. Read or write the data register to access the contents of the function register. All registers can be read and written except as noted in the following descriptions.

Function Register Map

Index	Name	Description	Read/Write Access
0x00	RAH	Row Address, High	R/W
0x01	RAL	Row Address, Low	R/W
0x02	CAL	Column Address, Low	R/W
0x03	REH	Row Address End, High	R/W
0x04	REL	Row Address End, Low	R/W
0x05	CEL	Column Address End, Low	R/W
0x06	DTR	Discharge Time Register	R/W
0x07	DCR	Discharge Current Register	R/W
0x08	CTRLA	Control Register A	R/W
0x09	CTRLB	Control Register B	R/W
0x0A	CTRLC	Control Register C	R/W
0x0B	SRA	Status Register A	R
0x0C	PGC	Programmable Gain Control Register	R/W
0x0D	ICR	Interrupt Control Register	R/W
0x0E	ISR	Interrupt Status Register	R/W
0x0F	THR	Threshold Register	R/W
0x10	CIDH	Chip Identification, High	R
0x11	CIDL	Chip Identification, Low	R
0x12	TST	Test Mode Register	R/W

Note: In the following descriptions, "sub-image" means a rectangular region of the sensor array, up to and including the entire array.

RAH   0x00

Row Address Register High.
Reset State: 0x00

This register holds the high order bit of the address of the first row of a sub-image.

Bit Number	Bit Name	Function
[7:1]	-	Reserved. Write 0 to these bits.
0	RA[8]	Most Significant Bit of Row Address Register

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RAL   0x01

Row Address Register Low.
Reset State: 0x00

This register holds the low order byte of the address of the first row of a sub-image.

Bit Number	Bit Name	Function
[7:0]	RA[7:0]	Low eight bits of Row Address Register

CAL   0x02

Column Address Register.
Reset State: 0x00

This register holds the address of the first column of a sub-image.

Bit Number	Bit Name	Function
[7:0]	CA[7:0]	Column Address Register

REH   0x03

Row Address End Register High.
Reset State: 0x00

This register holds the most significant bit of the address of the last row of a sub-image.

Bit Number	Bit Name	Function
[7:1]	-	Reserved. Write 0 to these bits.
0	REND[8]	Most Significant Bit of Row Address Register

REL   0x04

Row Address End Register Low.
Reset State: 0x00

This register holds the least significant byte of the address of the last row of a sub-image.

Bit Number	Bit Name	Function
[7:0]	REND[7:0]	Low eight bits of Row Address Register

CEL   0x05

Column Address End Register.
Reset State: 0x00

This register holds the address of the last column of a sub-image.

Bit Number	Bit Name	Function
[7:0]	CEND[7:0]	Column Address Register

DTR   0x06

Discharge Time Register
Reset State: 0x00

Bit Number	Bit Name	Function
[7]	-	Reserved. Write 0 to these bits.
[6:0]	DT[6:0]	Sets the discharge time in oscillator clock periods.

DCR   0x07

Discharge Current Register
Reset State: 0x00

Bit Number	Bit Name	Function
[7:5]	-	Reserved. Write 0 to these bits.
[4:0]	DC[4:0]	Sets the discharge current rate.

CTRLA 0x08

Control Register A.
Reset State: 0x00

Write this register to initiate image conversion. Read this register to read the A/D converter.

Bit Number	Bit Name	Function
7	-	Reserved. Write 0 to this bit.
6	-	Reserved. Write 0 to this bit.
5	-	Reserved. Write 0 to this bit.
4	-	Reserved. Write 0 to this bit.
3	AINSEL	0=Select Array for Conversion 1=Select External Analog Input Pin and Start Conversion
2	GETSUB	Initiates Auto-increment for sub-image
1	GETIMG	Initiates Auto-increment for whole image
0	GETROW	Initiates Auto-increment for selected row

The GETSUB, GETIMG, and GETROW bits select an image access mode and initiate an A/D conversion sequence. The AINSEL bit selects the input source to the A/D converter.

Set the GETSUB bit to initiate the capture of a rectangular sub-image defined by the RAH, RAL, CAL, REH, REL, and CEL registers. In CPU or SPI mode, the sub-image can be an arbitrary rectangle ranging from a single pixel to the entire array. In USB mode, the number of columns in the sub-image must be an integral multiple of 64.

Set the GETIMG bit to initiate the capture of a whole image starting from row zero and column zero through row 299 and column 255, regardless of the RAH, RAL, CAL, REH, REL, and CEL registers.

Set the GETROW bit to initiate the capture of a row specified by the RAH and RAL registers.

Writing a 1 to any of GETSUB, GETIMG, or GETROW abandons the current image access operation and restarts at the beginning of the sub-image, image, or row. Set at most one of these three bits. If more than one these three bits are set, image conversion will not start.

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Setting the GETROW bit causes the following events to happen:

- Row address loaded with contents of RAH and RAL register.

- Column address resets to zero

- Row capture automatically starts

- Analog to digital conversion of first pixel automatically starts

Setting the GETIMG bit causes the following events to happen:

- Row address resets to zero

- Column address resets to zero

- Row capture automatically starts

- Analog to digital conversion of first pixel automatically starts

Setting the GETSUB bit causes the following events to happen:

- Row address loaded with contents of RAH and RAL register

- Column address loaded with contents of CAL

- Row capture automatically starts

- Analog to digital conversion of first pixel automatically starts

Set the AINSEL bit along with one of the other three bits to begin the analog to digital conversion of the voltage on the AIN pin instead of the sensor array.

Writing 0 to the CTRLA register has no effect other than clearing AINSEL; the current image access operation is not abandoned.

Read CTRLA for the result of the A/D conversion. The rising edge of $\overline{RD}$ causes the next A/D conversion to start.

Parameter Description	Max	Units
Rising Edge of $\overline{WR}$ to First Data Valid	28 + DT[6:0]	Clock Cycles
Rising Edge of $\overline{RD}$ to Next Data Valid	6	Clock Cycles

Note: DT[6:0] refers to the contents of the Discharge Time Register.

CRTLB 0x09
Control Register B.

Reset State: CTRLB[7:6] = state of MODE[1:0].

CTRLB[5] = 1.

CTRLB [4:0] = 0, Chip is disabled, oscillator is stopped.

Bit Number	Bit Name	Function
[7:6]	MODE[1:0]	Reflects the state of the MODE[1:0] pins. These bits are read-only. Writing to these bits has no effect. Write 0 to these bits.
5	RDY	This is a read-only bit that indicates the status of the A/D Converter. 0 = A/D Conversion is in progress. 1 = A/D Converter is idle. Writing this bit has no effect. Write 0 to this bit.
4	-	Reserved. Write 0 to this bit.
3	AFDEN	Set this bit to enable the automatic finger detection circuit. In USB mode, automatic finger detection will generate an interrupt on endpoint 2. In CPU or SPI mode, automatic finger detection will generate a finger detect interrupt on the $\overline{\text{INTR}}$ pin as controlled by the Interrupt Control Register (ICR). In any mode, the automatic finger detection can be combined with ENABLE=0 to save power.
2	AUTOINCEN	0 = Column and row addresses do not automatically increment after the A/D converter is read. 1 = Column addresses increment and another A/D conversion is initiated after the A/D converter is read. The row address increments at the end of each column.
1	XTALSEL	In USB mode this bit has no function. In CPU and SPI mode this bit selects the clock source for the digital logic. 0 = Selects the internal 12 MHz multi-vibrator. 1 = Selects the XTAL1 pin.
0	ENABLE	0 = Place the sensor array, digital, and analog block into low-power state (12 MHz clock is halted, A/D Converter is shut down). 1= Enable the sensor array, digital, and analog blocks (12 MHz clock and A/D Converter are enabled).

CTRLC 0x0A

Control Register C. This register controls the behavior of general output port pins P0 and P1.

Reset State: 0x00

Bit Number	Bit Name	Function
[7:5]	PT1[2:0]	Programs the toggle rate of the P1 pin. If PT1[2:0] = 000, then the P1 pin follows the state of the P1 bit. Otherwise PT1[2:0] selects the clock divisor to generate a square wave on the P1 pin. 000 = P1 pin follows state of bit P1. 001 = clock divided by 2^{24}. 010 = clock divided by 2^{23}. 011 = clock divided by 2^{22}. 100 = clock divided by 2^{21}. 101 = Reserved. 110 = Reserved. 111 = Reserved.
[4:2]	PT0[2:0]	Programs the toggle rate of the P0 pin. If PT0[2:0] = 000, then the P0 pin follows the state of the P0 bit. Otherwise PT0[2:0] selects the clock divisor to generate a square wave on the P0 pin. 000 = P0 pin follows state of bit P0. 001 = clock divided by 2^{24}. 010 = clock divided by 2^{23}. 011 = clock divided by 2^{22}. 100 = clock divided by 2^{21}. 101 = Reserved. 110 = Reserved. 111 = Reserved.
1	P1	General Purpose Output Port. When PT1[2:0] bits are 000, this bit controls the P1 pin. 0 = P1 pin low. 1 = P1 pin high.
0	P0	General Purpose Output Port. When PT0[2:0] bits are 000, this bit controls the P0 pin. 0 = P0 pin low. 1 = P0 pin high.

SRA   0x0B

Status Register A. Read Only. This register shadows the state of CTRLA.

Reset State: 0x00

Bit Number	Bit Name	Function
7	-	Reserved. Returns 0.
6	-	Reserved. Returns 0.
5	-	Reserved. Returns 0.
4	-	Reserved. Returns 0.
3	AINSEL	This bit is set or cleared when the AINSEL bit (CTRLA bit 3) is set or cleared by software.
2	GETSUB	This bit is set when the GETSUB bit (CTRLA bit 2) is set by software. This bit is cleared after the last byte is read.
1	GETIMG	This bit is set when the GETIMG bit (CTRLA bit 1) is set by software. This bit is cleared after the last byte is read.
0	GETROW	This bit is set when the GETROW bit (CTRLA bit 0) is set by software. This bit is cleared after the last byte is read.

PGC   0x0C

Programmable Gain Control Register.

Reset State: 0x00

Bit Number	Bit Name	Function
[7:4]	-	Reserved. Write 0 to these bits. Returns 0 when read.
[3:0]	PG[3:0]	Sets the gain of the amplifier. 0000 = 1.0 (default) 0001 = 0.25 0010 = 0.50 0011 = 0.75 0100 = 1.0 0101 = 1.25 0110 = 1.50 0111 = 1.75 1000 = 4.0 1001 = 1.0 1010 = 2.0 1011 = 3.0 1100 = 4.0 1101 = 5.0 1110 = 6.0 1111 = 7.0

ICR   0x0D

Interrupt Control Register.

Reset State 0x00.

This register controls the behavior of the two interrupt sources of the fingerprint sensor. Interrupt request 0 corresponds to the finger detect interrupt. Interrupt request 1 corresponds to the external interrupt pin EXTINT.

Set bits IE[1:0] to enable the corresponding interrupt. Disabling an interrupt prevents the interrupt event from causing the chip to assert INTR or to send a packet on USB endpoint 2. However, the interrupt event is not prevented from setting its corresponding bit in the ISR register.

Set bits IM[1:0] to prevent an interrupt event from setting the corresponding bit in the ISR. Setting or clearing IM[1:0] will not clear ISR bits IR[1:0].

Set bits IT[1:0] to program the interrupts as edge or level sensitive. If IT1 is programmed as edge triggered, then IR1 (interrupt request 1) will be set by the falling edge of EXTINT.

IP[1:0] select the polarity of the interrupt source. To detect finger down and finger up states with the internal finger detect circuit, set the IP0 bit to detect finger down (rising or high signal). After the finger down interrupt occurs, clear the IP0 bit to detect finger up (falling or low signal). Similarly, IP1 can be programmed to select the polarity of the EXTINT signal.

Bit Number	Bit Name	Function
7	IP1	0=EXTINT Interrupt Polarity is Falling Edge or Active Low 1=EXTINT Interrupt Polarity is Rising Edge or Active High
6	IP0	0=Finger Detect Interrupt Polarity is Falling Edge or Active Low 1=Finger Detect Interrupt Polarity is Rising Edge or Active High
5	IT1	0=EXTINT Interrupt is Edge Triggered 1=EXTINT Interrupt is Level Triggered
4	IT0	0=Finger Detect Interrupt is Edge Triggered 1=Finger Detect Interrupt is Level Triggered
3	IM1	0=EXTINT Interrupt Not Masked 1=EXTINT Interrupt Masked
2	IM0	0=Finger Detect Interrupt Not Masked 1=Finger Detect Interrupt Masked
1	IE1	0=EXTINT Interrupt Disabled 1=EXTINT Interrupt Enabled
0	IE0	0=Finger Detect Interrupt Disabled 1=Finger Detect Interrupt Enabled

ISR   0x0E

Interrupt Status Register.
Reset State   ISR[7:2] = 0.

ISR[1:0] = X. State is indeterminate after reset.

Read this register to determine source(s) of interrupt(s).
Write a 1 to IR[1:0] to acknowledge and clear the corresponding interrupt bit.

Bits IS[1:0] reflect the state of the finger detect sensor and the EXTINT pin, regardless of the bit settings in the ICR register. When the finger detect sensor is not triggered, the IS0 bit will be constantly low. However the IS0 bit may not be constantly high when a finger is present; the bit may be repeatedly changing from a low to high state.

Bit Number	Bit Name	Function
[7:4]	-	Reserved. Write 0 to these bits. Returns 0 when read.
3	IS1	Reflects the state of the EXTINT Pin. Write 0 to this bit.
2	IS0	Reflects the state of the Finger Detect Sensor. Write 0 to this bit.
1	IR1	EXTINT Interrupt Request Pending.
0	IR0	Finger Detect Interrupt Request Pending.

THR   0x0F

Threshold Register.
Reset State 0x00.

This register controls the threshold at which a finger is detected by the automatic finger detection circuit.

Bit Number	Bit Name	Function
7	-	Reserved. Write 0 to this bit.
[6:4]	THV[2:0]	Threshold voltage level.
[3:0]	THC[3:0]	Sharing capacitor size.

CIDH   0x10

Chip Identification Register High. This register holds the high order byte of the chip identification word.

Bit Number	Bit Name	Function
[7:0]	CIDH[7:0]	Returns 0x20 when read.

CIDL   0x11

Chip Identification Register Low. This register holds the low order byte of the chip identification word.

Bit Number	Bit Name	Function
[7:0]	CIDL[7:0]	The return value depends on the Revision of the chip.

TST   0x12

Test Mode Register. Reserved for factory use only.

Reset State 0x00.

Bit Number	Bit Name	Function
[7:0]	TST[7:0]	Reserved. Write only 0 to these bits.

Solid State Fingerprint Sensor

Sensor Initialization

The sensor should be enabled and its image parameters adjusted before beginning a GETIMG, GETROW, or GETSUB operation.

```
   ┌─────────────────┐
   │   Enable ADC    │
   └─────────────────┘
            │
   ┌─────────────────┐         ┌──────────────────────┐
   │ Write CTRLB with│─────────│ If using an external │
   │ bits 2 and 0 set.│        │ clock, then set bit  │
   └─────────────────┘         │ 1 also.              │
            │                  └──────────────────────┘
   ┌─────────────────┐         ┌──────────────────────┐
   │  Wait 30 µS.    │─────────│ Other registers (DTR │
   └─────────────────┘         │ and DCR for example) │
            │                  │ can be initialized   │
   ┌─────────────────┐         │ during this time.    │
   │ Sensor Enabled. │         └──────────────────────┘
   └─────────────────┘
```

```
   ┌─────────────────┐
   │ Adjust Parameters│
   └─────────────────┘
            │
   ┌─────────────────┐
   │   Write DTR.    │
   └─────────────────┘
            │
   ┌─────────────────┐
   │   Write DCR.    │
   └─────────────────┘
            │
   ┌─────────────────┐
   │   Write PGC.    │
   └─────────────────┘
            │
   ┌─────────────────┐
   │Parameters Adjusted.│
   └─────────────────┘
```
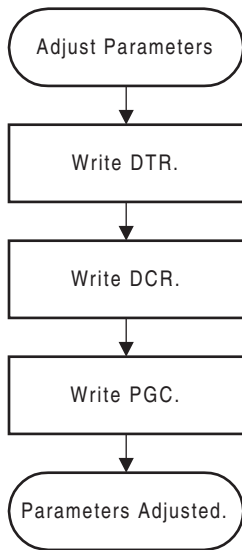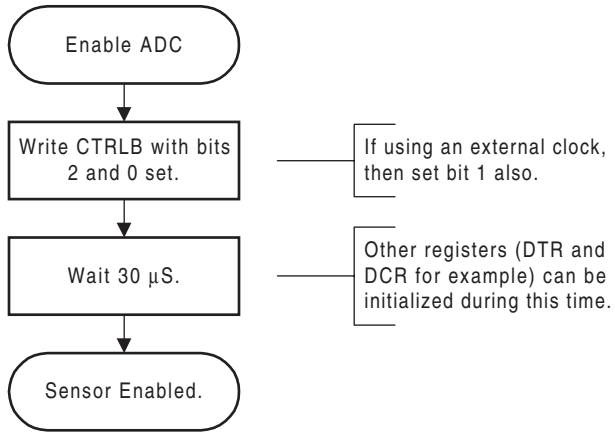
Image Retrieval

Microprocessor Interface
Get Row

First load the RAH and RAL registers with the address of the row to be fetched. Then write the CTRLA register to initiate a GETROW operation. Finally, read the CTRLA register 256 times to retrieve the row data.

```
   ┌─────────────────┐
   │ Setup Row Address│
   │   (MCU Mode)    │
   └─────────────────┘
            │
   ┌─────────────────┐         ┌──────────────────────┐
   │   Write RAH.    │─────────│ Set Row Address      │
   └─────────────────┘         │ High Order bit.      │
            │                  └──────────────────────┘
   ┌─────────────────┐         ┌──────────────────────┐
   │   Write RAL.    │─────────│ Set Row Address      │
   └─────────────────┘         │ Low Order byte.      │
            │                  └──────────────────────┘
   ┌─────────────────┐
   │  Row Selected.  │
   └─────────────────┘
```

```
   ┌─────────────────┐
   │     GetRow      │
   │   (MCU Mode)    │
   └─────────────────┘
            │
   ┌─────────────────┐
   │ Write CTRLA with│
   │     0x01.       │
   └─────────────────┘
            │
   ┌─────────────────┐
   │ Wait Row Capture│
   │     Time.       │
   └─────────────────┘
            │
   ┌─────────────────┐◄────┐
   │   Read CTRLA.   │     │
   └─────────────────┘     │
            │              │
   ┌─────────────────┐     │
   │   Wait A/D      │     │ No
   │ Conversion Time.│     │
   └─────────────────┘     │
            │              │
         ◇ Last Cell ◇─────┘
         ◇ of Row was ◇
         ◇  Read?    ◇
            │
           Yes
            │
   ┌─────────────────┐
   │  Row Captured.  │
   └─────────────────┘
```
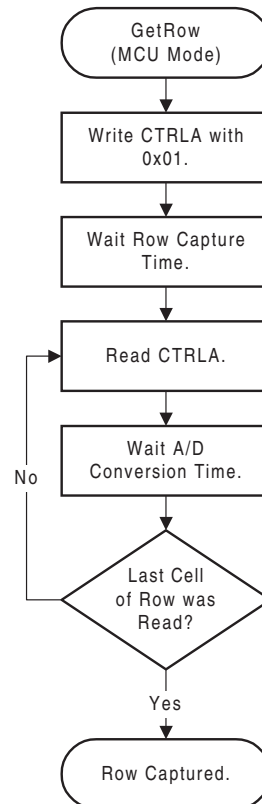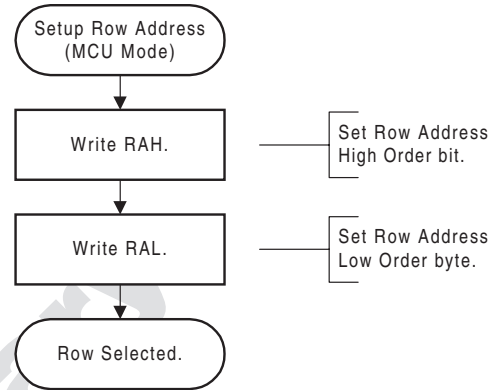
Get Whole Image

No row or column registers need to be loaded prior to starting a GETIMG operation. The sensor will automatically begin A/D conversion at row zero, column zero.

```
        Image Capture
         (MCU Mode)
              │
              ▼
      Write CTRLA with
          0x02.
              │
              ▼
      Wait Row Capture
          Time.
              │
              ▼
        Read CTRLA.
              │
              ▼
        Wait A/D
     Conversion Time.
              │
              ▼
        Last Cell
       of Row was    ── No
          Read?
              │ Yes
              ▼
        Last Cell
        of Image     ── No
       was Read?
              │ Yes
              ▼
       Image Captured.
```
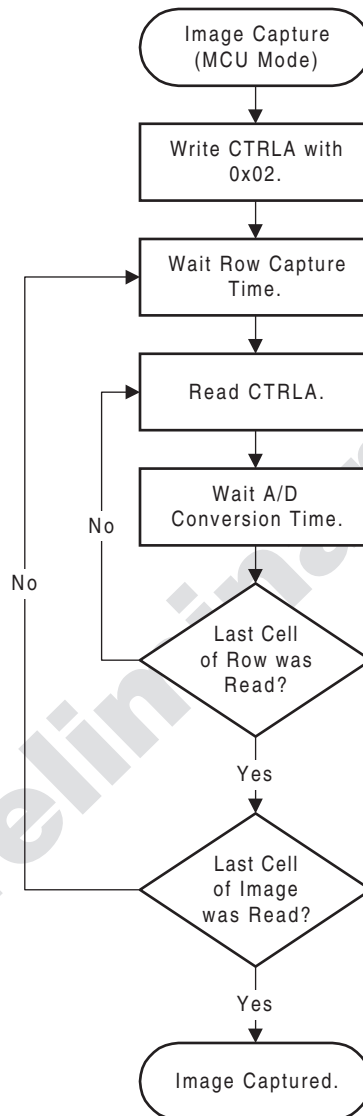
Solid State Fingerprint Sensor

Get Sub-Image

First, load the RAH, RAL, and CAL registers with the starting row and column address of the sensor sub-region. Then load registers REH, REL, and CEL with the ending row and column address of the sensor sub-region. Write the CTRLA register to initiate a GETSUB operation. Finally, read CTRLA register until the sub-image has been retrieved. The RAH, RAL, CAL, REH, REL, and CEL registers do not have to be loaded before each GETIMG operation unless a different sensor sub0region is to be captured.

Setup Sub Region (MCU Mode)

Write RAH. — Set Starting Row Address, High Order bit.

Write RAL. — Set Starting Row Address, Low Order byte.

Write CAL. — Set Starting Column Address.

Write REH. — Set Ending Row Address, High Order bit.

Write REL. — Set Ending Row Address, Low Order byte.

Write CEL. — Set Ending Column Address.

Sub Region Selected.

Get Sub Image (MCU Mode)

Write CTRLA with 0x04.

Wait Row Capture Time.

Read CTRLA.

Wait A/D Conversion Time.

Last Cell of Row was Read? — No / Yes

Last Cell of Image was Read? — No / Yes

Image Captured.

Serial Peripheral Interface

The "Get Image," "Get Sub-Image," and "Get Row" operations are initiated by writing the same registers as described in the microprocessor interface, except that the commands are written to the MOSI pin and the data is read back on the MISO pin. However, in SPI mode, an image or sub-image cannot be retrieved by issuing a single Register Read Command and shifting in the entire image; a separate Register Read Command must be issued prior to reading each row.

Get Image

```
        ┌─────────────────────┐
        │   Image Capture      │
        │    (SPI Mode)        │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │  Drive SCS- Low.     │
        │  Send Write Opcode.  │
        │  Send CTRLA Address. │
        │  Send Data 0x02.     │
        │  Drive SCS- High.    │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │  Wait Row Capture    │
        │       Time.          │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │  Drive SCS- Low.     │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │  Send Read Opcode.   │
        │  Send CTRLA Address. │
        └──────────┬──────────┘
                   │
        ┌──────────▼──────────┐
        │     Read Data.       │
        └──────────┬──────────┘
                   │
              ╱────▼────╲
   No   No   ╱ Converted ╲
  ◄────◄────◄  Last Cell  ►
             ╲  of Row?   ╱
              ╲────┬────╱
                   │ Yes
        ┌──────────▼──────────┐
        │  Drive SCS- High.    │
        └──────────┬──────────┘
                   │
              ╱────▼────╲
             ╱ Converted ╲
  ◄─────────◄  Last Cell  ►
             ╲ of Image?  ╱
              ╲────┬────╱
                   │ Yes
        ┌──────────▼──────────┐
        │   Image Captured.    │
        └─────────────────────┘
```
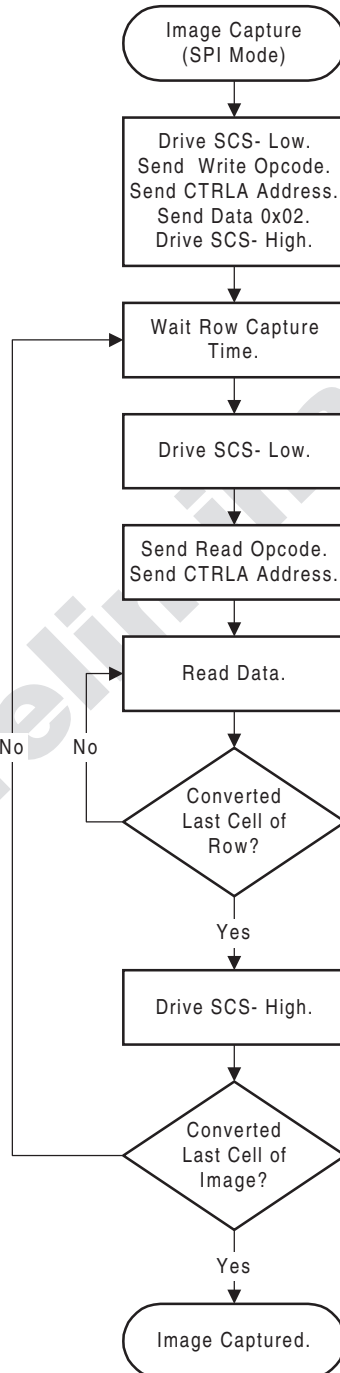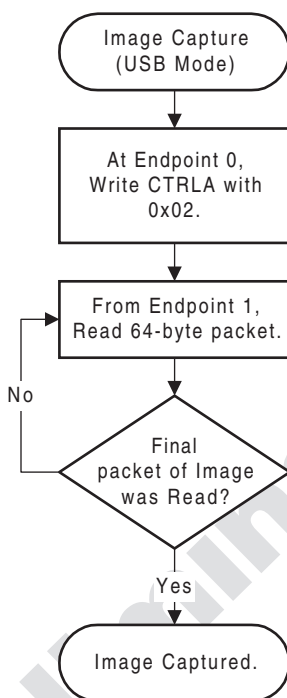
Solid State Fingerprint Sensor

USB Interface

The "Get Image," "Get Sub-Image," and "Get Row" operations are initiated by writing the same registers as described in the microprocessor interface, except that the registers are written and read on endpoint 0 and the image data is read from endpoint 1.

Get Image

```
        ┌─────────────────────┐
        │   Image Capture     │
        │    (USB Mode)       │
        └─────────────────────┘
                  │
                  ▼
        ┌─────────────────────┐
        │   At Endpoint 0,    │
        │  Write CTRLA with   │
        │       0x02.         │
        └─────────────────────┘
                  │
                  ▼
        ┌─────────────────────┐
        │  From Endpoint 1,   │◄────┐
        │ Read 64-byte packet.│     │
        └─────────────────────┘     │ No
                  │                 │
                  ▼                 │
              ╱───────╲             │
             ╱  Final  ╲            │
            ╱ packet of ╲───────────┘
            ╲ Image was ╱
             ╲  Read?  ╱
              ╲───────╱
                  │ Yes
                  ▼
        ┌─────────────────────┐
        │   Image Captured.   │
        └─────────────────────┘
```

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V$_{DD}$	Power Supply Voltage	+7.0	V
V$_{IN}$, V$_{OUT}$	Voltage on Any Pin Relative to VSS	-0.5V to +7.0V	V
I$_{OUT}$	Output Current per I/O	8.0	mA
T$_{STG}$	Storage Temperature	-65°C to +150°C	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

Operating Range

Symbol	Description		Min	Max	Unit
V$_{DD}$	Supply Voltage		3.3	5.5	V
		USB Mode	3.3	3.6	V
T$_A$	Ambient Temperature		0°C	60°C	°C

DC Characteristics

(VDD=5.0V)

Symbol	Description	Test Conditions	Min	Max	Units
V$_{IL}$	Input LOW Voltage	VDO = 4.5V	-0.5	0.8	V
V$_{IH}$	Input HIGH Voltage	–	2.0	VDD	V
V$_{OL}$	Output LOW Voltage	VDD = MIN, IOL = 8 mA	-	0.4	V
V$_{OH}$	Output HIGH Voltage	VDD = MIN, IOH = -4 mA	2.4	-	V
I$_{LI}$	Input Leakage Current	VDD = MAX, VIN = VSS to VDD	-5.0	5.0	µA
I$_{LO}$	Output Leakage Current	VDD = MAX, VOUT = VSS to VDD, CE0- = VIH or CE1 = VIL	-5.0	5.0	µA

(VDD=3.3V)

Symbol	Description	Test Conditions	Min	Max	Units
V$_{IL}$	Input LOW Voltage	VDD = 3.0V	-0.5	0.6	V
V$_{IH}$	Input HIGH Voltage		2.0	VDD	V
V$_{OL}$	Output LOW Voltage	VDD = 3.6V, IOL = 4 mA	-	0.4	V
V$_{OH}$	Output HIGH Voltage	VDD = 3.0V, IOH = -2 mA	2.4	-	V
I$_{LI}$	Input Leakage Current	VDD = 3.6V VIN = VSS to VDD	-5.0	5.0	µA
I$_{LO}$	Output Leakage Current	VDD = 3.6V, VOUT = VSS to VDD, CE0- = VIH or CE1 = VIL	-5.0	5.0	µA

Solid State Fingerprint Sensor

Power Supply Consumption

Symbol	Description	Test Conditions	Typ	Max	Units
(Microprocessor Mode, VDD=5.0V f_{OSC} = 20MHz)					
I_{DD}	Digital Current, Dynamic		TBD	5	mA
I_{DDSB}	Digital Current, Standby		TBD	1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	10	µA
I_{DDPD}	Digital Current, Power Down		TBD	10	µA
I_{DDA}	Analog Current, Dynamic		TBD	20	mA
I_{DDASB}	Analog Current, Standby		TBD	12	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	200	µA
I_{DDAPD}	Analog Current, Power Down		TBD	10	µA
(SPI Slave Mode, VDD=5.0V)					
I_{DD}	Digital Current, Dynamic		TBD	5	mA
I_{DDSB}	Digital Current, Standby		TBD	1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	10	µA
I_{DDPD}	Digital Current, Power Down		TBD	10	µA
I_{DDA}	Analog Current, Dynamic		TBD	20	mA
I_{DDASB}	Analog Current, Standby		TBD	12	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	200	µA
I_{DDAPD}	Analog Current, Power Down		TBD	10	µA
(Microprocessor Mode, VDD=3.3V)					
I_{DD}	Digital Current, Dynamic		TBD	5	mA
I_{DDSB}	Digital Current, Standby		TBD	1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	10	µA
I_{DDPD}	Digital Current, Power Down		TBD	10	µA
I_{DDA}	Analog Current, Dynamic		TBD	15	mA
I_{DDASB}	Analog Current, Standby		TBD	8	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	200	µA
I_{DDAPD}	Analog Current, Power Down		TBD	10	µA
(SPI Slave Mode, VDD=3.3V)					
I_{DD}	Digital Current, Dynamic		TBD	5	mA
I_{DDSB}	Digital Current, Standby		TBD	1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	10	µA
I_{DDPD}	Digital Current, Power Down		TBD	10	µA
I_{DDA}	Analog Current, Dynamic		TBD	15	mA
I_{DDASB}	Analog Current, Standby		TBD	8	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	200	µA
I_{DDAPD}	Analog Current, Power Down		TBD	10	µA

Power Supply Consumption (continued)

Symbol	Description	Test Conditions	Typ	Max	Units
(USB Mode, VDD=3.3V)					
I_{DD}	Digital Current, Dynamic		TBD	5	mA
I_{DDSB}	Digital Current, Standby		TBD	1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		TBD	10	µA
I_{DDPD}	Digital Current, Power Down		TBD	10	µA
I_{DDSPF}	Digital Current, USB Suspend with Auto Finger Detection Enabled		TBD	10	µA
I_{DDSP}	Digital Current, USB Suspend		TBD	10	µA
I_{DDA}	Analog Current, Dynamic		TBD	30	mA
I_{DDASB}	Analog Current, Standby		TBD	20	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		TBD	200	µA
I_{DDAPD}	Analog Current, Power Down		TBD	10	µA

AC Characteristics

Microprocessor Bus Mode
Read Cycle

Symbol	Description	Min	Max	Units
t_{ACC}	Address to Output Delay	5	35	ns
t_{CE}	Chip Select to Output Delay	5	35	ns
t_{OE}	Read Enable to Output Delay	5	35	ns
t_{OH}	Output Hold Time from Address, $\overline{CS0}$, CS1, or $\overline{RD}$, which ever occurs first	5	-	ns
t_{DF}	$\overline{RD}$ high to Output High Z	-	10	ns
t_{DF}	$\overline{CS0}$ high or CS1 low to Output High Z	-	10	ns

Write Cycle

Symbol	Description	Min	Max	Units
t_{AS}	Address Setup to $\overline{WR}$ low	0	-	ns
t_{CS}	$\overline{CS0}$ Setup to $\overline{WR}$ low	0	-	ns
t_{CS}	CS1 Setup to $\overline{WR}$ low	0	-	ns
t_{AH}	Address Hold Time from $\overline{WR}$ high	5	-	ns
t_{CH}	$\overline{CS0}$ Hold Time from $\overline{WR}$ high	0	-	ns
t_{CH}	CS1 Hold Time from $\overline{WR}$ high	0	-	ns
t_{WP}	$\overline{WR}$ Pulse Width Low	10	-	ns
t_{WPH}	$\overline{WR}$ Pulse Width High	10	-	ns
t_{DS}	Data Setup Time to $\overline{WR}$ low	8	-	ns
t_{DH}	Data Hold Time to $\overline{WR}$ high	0	-	ns

Solid State Fingerprint Sensor

SPI Slave Mode

Symbol	Description	Min	Max	Units
f_{SCK}	SCLK Clock Frequency	-	12	MHz
t_{CSS}	$\overline{SCS}$ Setup Time	40	-	ns
t_{CSH}	$\overline{SCS}$ Hold Time	40	-	ns
t_{WL}	SCLK Low	40	-	ns
t_{WH}	SCLK High	40	-	ns
t_{CS}	$\overline{SCS}$ High Time	40	-	ns
t_{SU}	Data-In Setup Time	20	-	ns
t_{H}	Data-In Hold Time	20	-	ns
t_{V}	Data-Out Valid Time	20	30	ns
t_{HD}	Data-Out Hold Time	0	-	ns
t_{DIS}	Data-Out Disable Time	-	100	ns

SPI Master

Symbol	Description	Min	Max	Units
f_{SCKM}	SCLK Clock Frequency	-	2	MHz
t_{CSSM}	$\overline{SCS}$ Setup Time	250	-	ns
t_{CSHM}	$\overline{SCS}$ Hold Time	-	250	ns
t_{WLM}	SCLK Low	-	250	ns
t_{WHM}	SCLK High	-	250	ns
t_{CSM}	$\overline{SCS}$ High Time	-	250	ns
t_{SUM}	Data-In Setup Time	-	100	ns
t_{HM}	Data-In Hold Time	-	250	ns
t_{VM}	Data-Out Valid Time	-	200	ns
t_{HDM}	Data-Out Hold Time	-	200	ns
t_{DISM}	Data-Out Disable Time	-	300	ns

Timing Diagrams
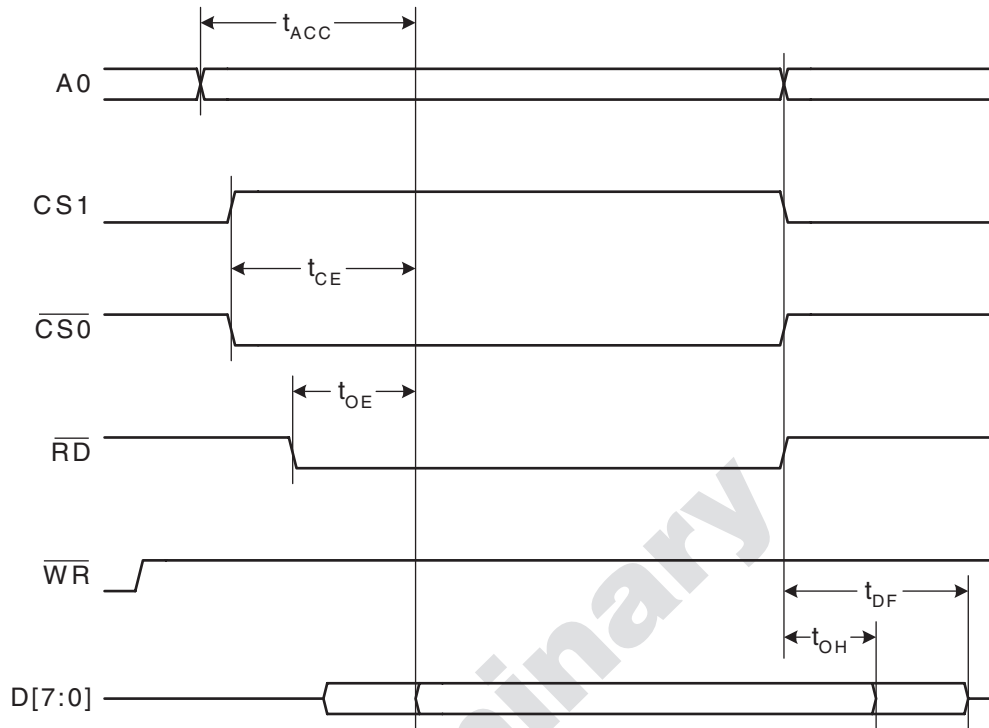
Figure 1.   Microprocessor Mode Read Cycle
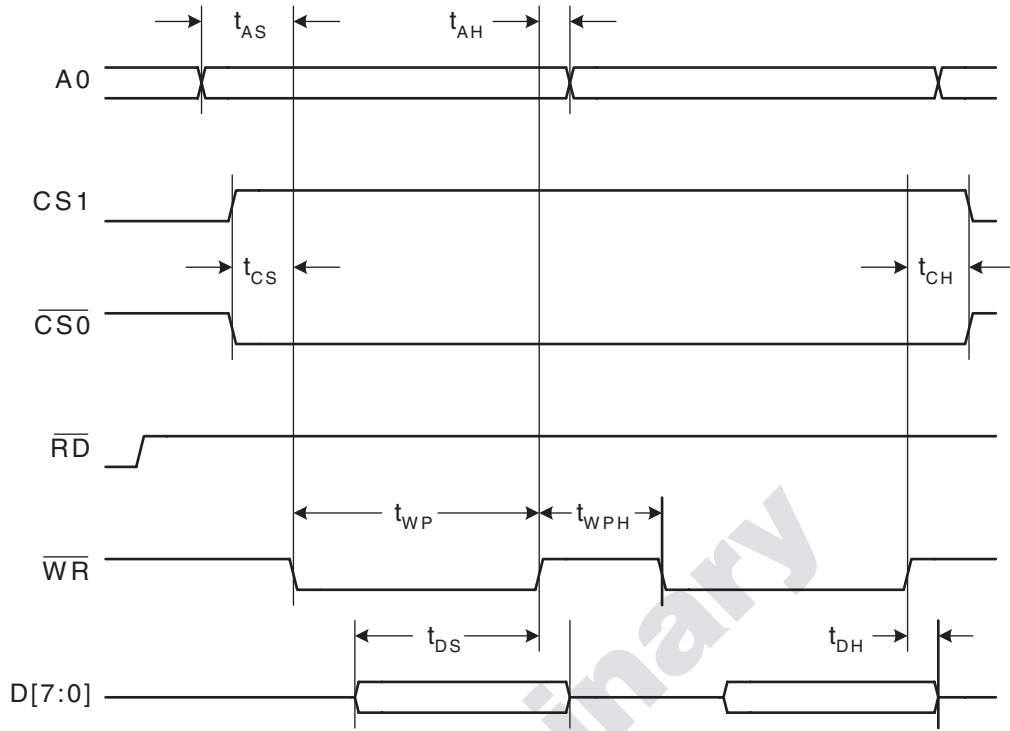
Solid State Fingerprint Sensor
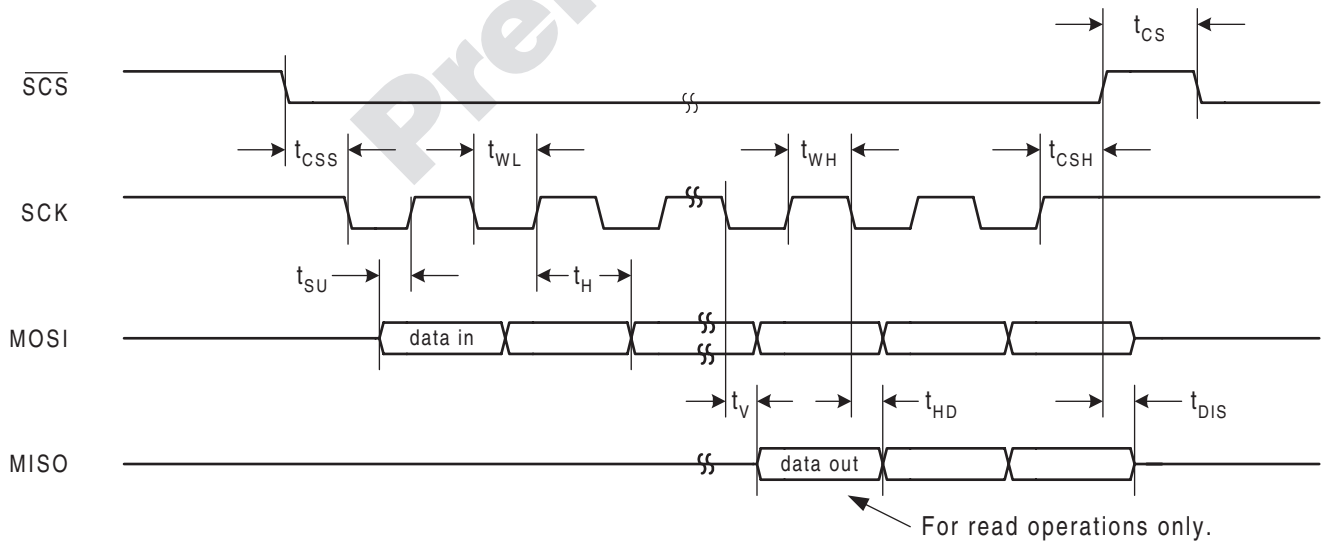

Figure 2. Microprocessor Mode Write Cycle

For read operations only.

Figure 3. SPI Slave Mode Timing

Figure 4.   SPI Slave Mode Read Operation

Figure 5.   SPI Slave Mode Write Operation

Figure 6.   SPI Master Timing

Solid State Fingerprint Sensor
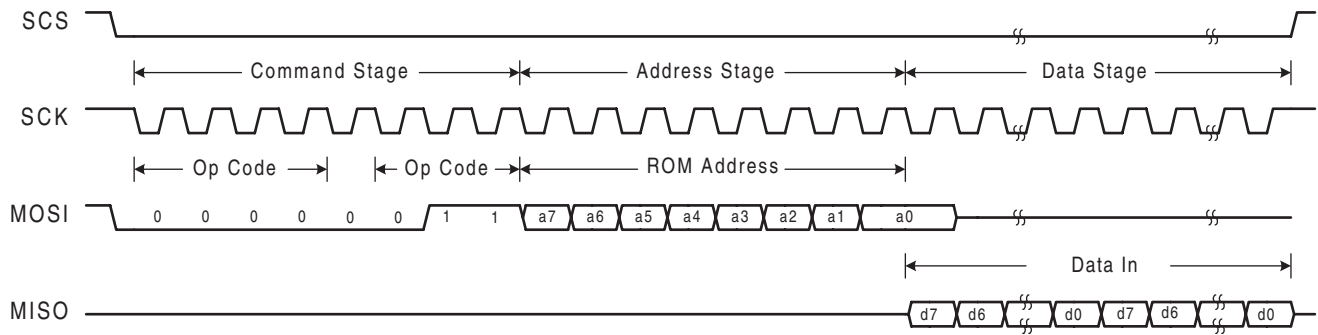
Figure 7. SPI Master Read Operation

Physical Dimensions

MBF200

TSOP(LQFP)-80 pin Package
MBF200 : TSOP 80 pin Assembly Diagram
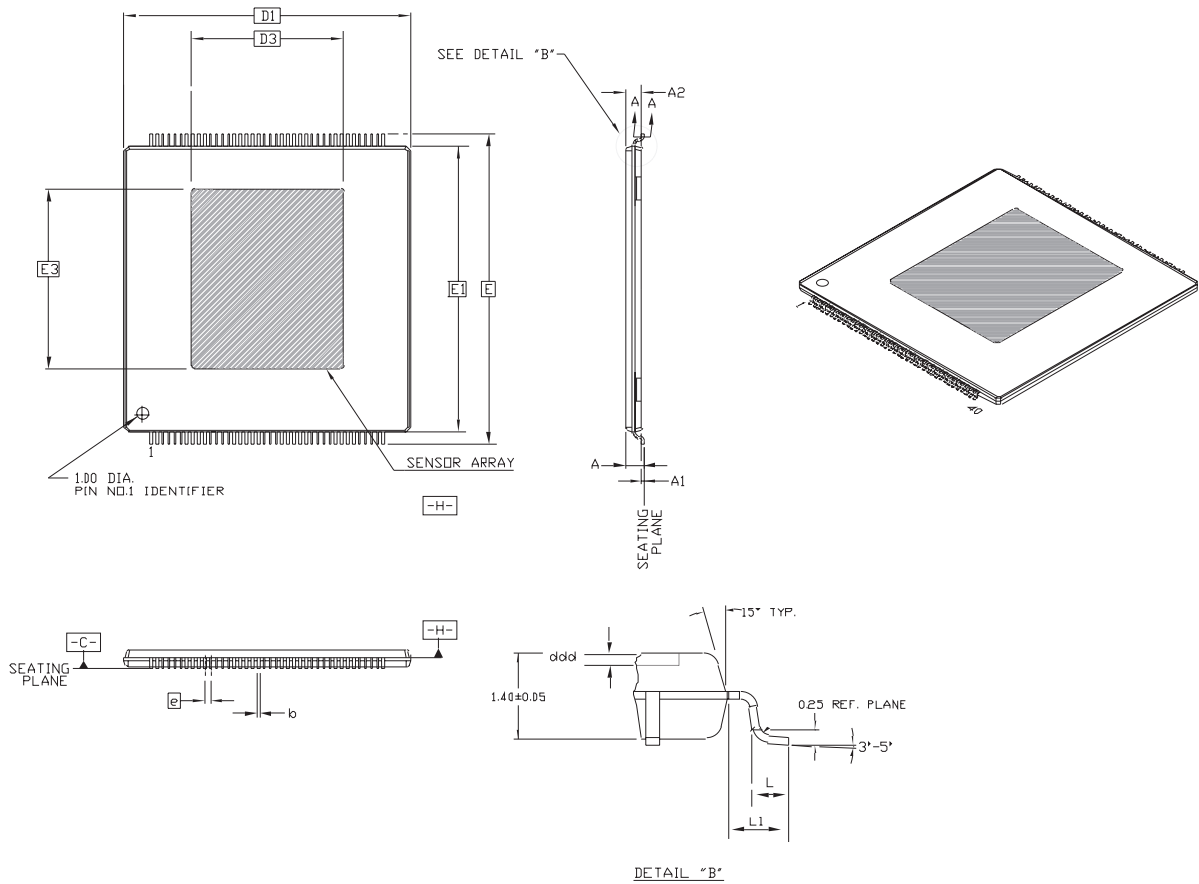
	MBF200	DIMENSIONS					
SYMBOL	Description	MILLIMETERS			INCHES		
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	Overall Height	1.45	1.55	1.70	.057	.061	.067
A1	Stand Off	0.10	0.15	0.20	.004	.006	.010
A2	Package Thickness	1.35	1.40	1.45	.053	.055	.057
b	Lead Width	0.16	0.25	0.30	.006	.010	.012
D1	Pacakge Body Width		24.00 BSC.			.945 BSC.	
D3	Sensor Array Width	12.74	12.79	12.84	.502	.504	.506
ddd	Sensor Array Depth		0.30	0.35		.012	.014
E	Tip to Tip Dimension	0.25	26.00 BSC.			1.024 BSC.	
E1	Package Body Height		24.00 BSC.			.945 BSC.	
E3	Sensor Array Height	14.95	15.00	15.05	.588	.590	.592
e	Lead Pitch		0.50 TYP.			.0197 TYP.	
L	Lead Length	0.50	0.60	0.70	.020	.024	.028
L1	Foot Length		1.00 REF.			.039 REF.	

Solid State Fingerprint Sensor

Recommended Land Pattern
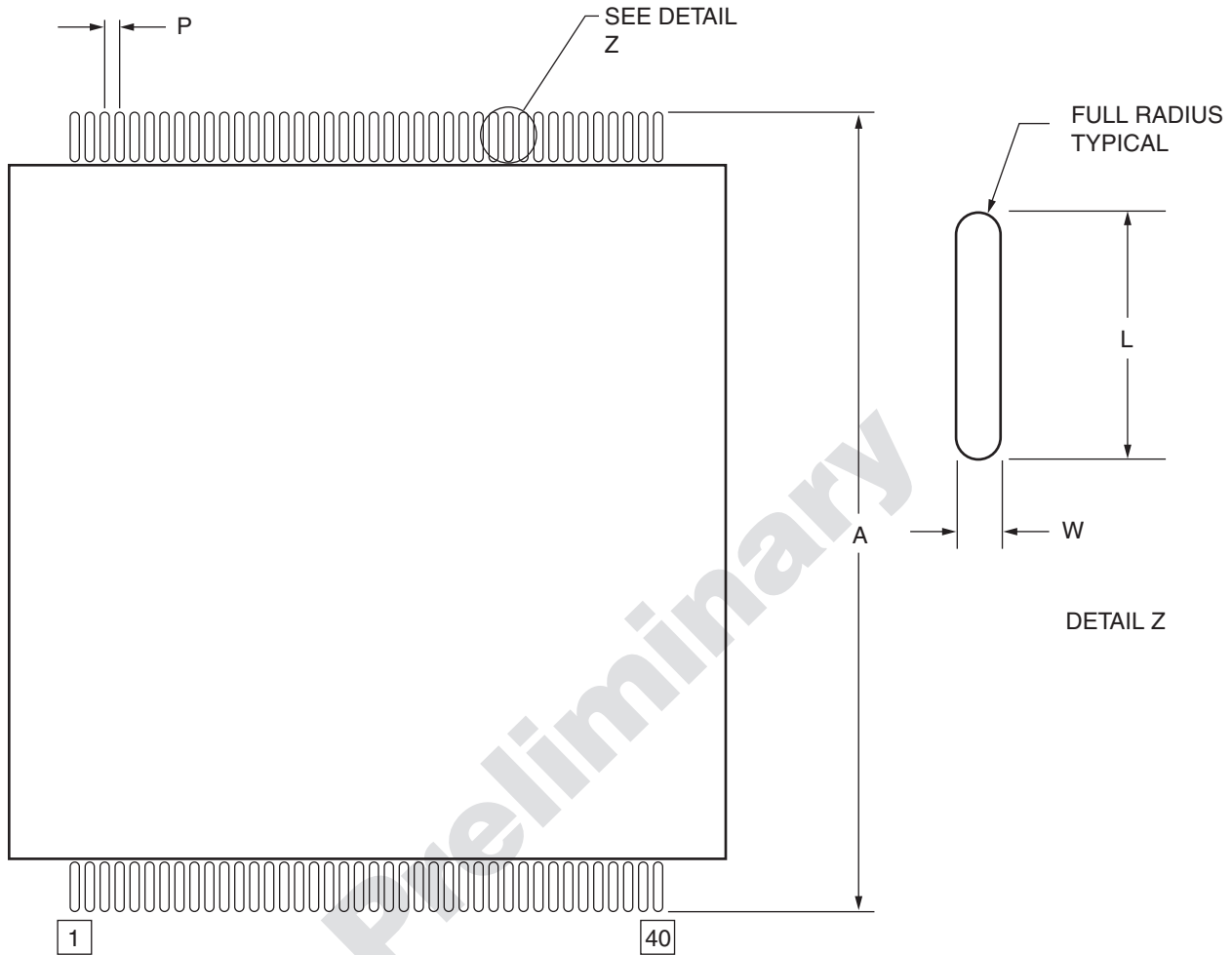
Symbol	Description	Dimension
N	Pin Count	80
A	Tip to Tip Dimension	1.074 (27.30)
P	Pitch	.0197 (.50)
L	Pad Length	.065 (1.65)
W	Pad Width	.012 (.30)

Note: Dimensions are in inches (mm)

Array Orientation

(0, 0)   (255, 0)

MBF200

(0, 299)   (255, 299)
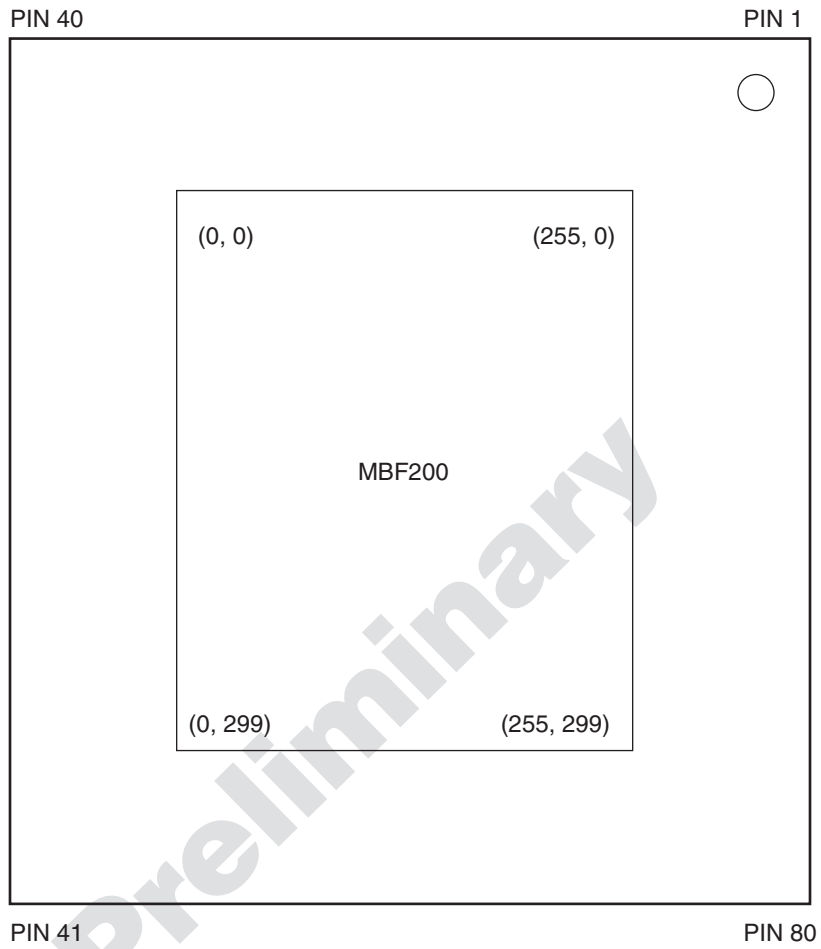
Solid State Fingerprint Sensor

Appendix A

Recommended Power and Ground Connections

The following describes the recommended method for reducing image noise to get the best image from the sensor.

VDDA1 (Pin 1) and VDDA2 (Pin 7) are the analog power supply pins. VSSA1 (Pin 2) and VSSA2 (Pin 6) are the ground returns. Connect one bulk capacitor (4.7µF to 10µF) and two 0.1µF capacitors in parallel between analog power and ground to provide filtering of low and high frequency noise. Place the bulk capacitor near VDDA1. Separate VDDA1 and VDDA2 from the digital power pins through a 10 ohm resistor.

VDD1 (Pin 16), VDD2 (Pin 25), and VDD3 (Pin 39) are the digital power supply pins. VSS1 (Pin 15), VSS2 (Pin 24), and VSS3 (Pin 40) are the ground returns. Place 0.1µF capacitors between digital power and ground, as close to the pins as possible.

Input signals that are to be tied high should not be shorted directly to VDD, but connected through a 1K to 10K ohm resistor in order to maximize ESD immunity of the sensor. A single resistor may be used for all inputs that are tied high.
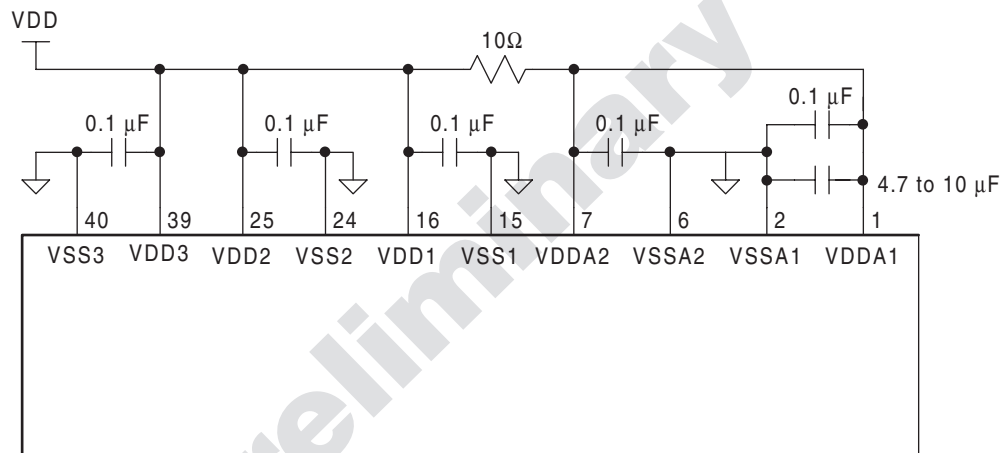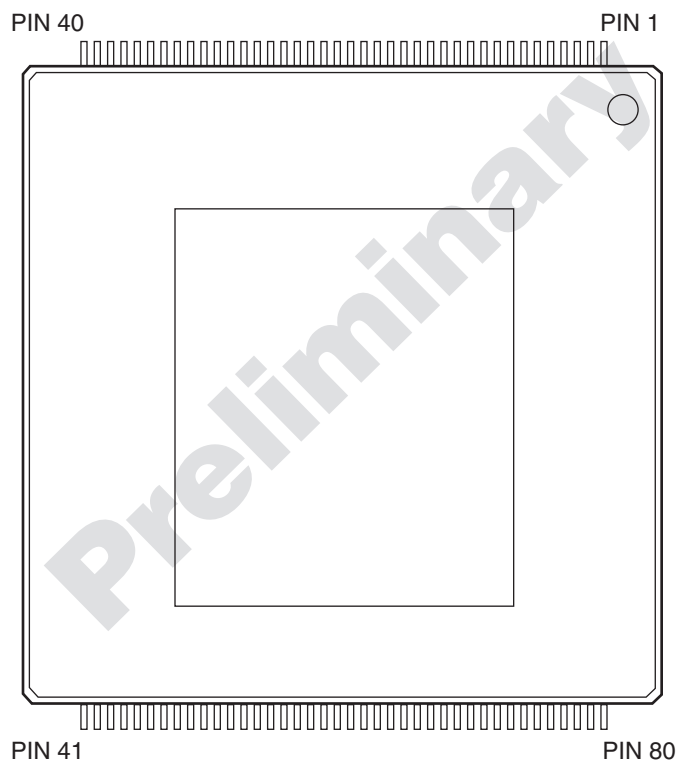
MBF200

APPENDIX B

Recommended MBF200 Sensor Orientation

Mount the MBF200 such that pins 1 through 40 point away the user and pins 41 through 80 point toward from the user. When a finger is placed on the sensor, the tip of the finger should be near pins 1 through 40, the cuticle should be centered over the sensor, and the knuckle should be near pins 41 through 80. This orientation ensures that fingerprint images will be captured right-side up, not sideways nor upside down, using Fujitsu's standard software.

The sensor should be mounted flush with the surrounding surface to allow the finger to rest flat on the sensor surface and increase the contact area between the finger and the sensor. If the sensor is recessed too deeply, only the tip of the finger will be imaged.

It is also recommended that there be a groove or channel to guide the finger into the proper position so that images are captured with a uniform orientation.

PIN 40   PIN 1

PIN 41   PIN 80

35