4Stacked MCP (Multi-Chip Package) FLASH & FLASH & FCRAM & SRAM

CMOS

128M (×16) Page Mode FLASH MEMORY & 64M (×16) FLASH MEMORY & 64M (×16) Mobile FCRAM™ & 8M (×16) STATIC RAM

MB84VZ128B-70

■ FEATURES

- **Power Supply Voltage of 2.7 to 3.1V**
- **High Performance**
  25 ns maximum Page read access time, 70 ns maximum random access time (Flash_1)
  70 ns maximum access time (Flash_2)
  65 ns maximum access time (FCRAM)
  70 ns maximum access time (SRAM)
- **Operating Temperature**
  –30 °C to +85 °C
- **Package 115-ball BGA**

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■ PRODUCT LINEUP

	Flash_1	Flash_2	FCRAM	SRAM
Supply Voltage (V)	V_{ccf}_1* = 3.0 V $^{+0.1V}_{-0.3\ V}$	V_{ccf}_2* = 3.0 V $^{+0.1V}_{-0.3\ V}$	V_{ccr}* = 3.0 V $^{+0.1V}_{-0.3\ V}$	V_{ccs}* = 3.0 V $^{+0.1V}_{-0.3\ V}$
Max. Random Address Access Time (ns)	70	70	65	70
Max. Page Address Access Time (ns)	25	-	-	-
Max. $\overline{CE}$ Access Time (ns)	70	70	65	70
Max. $\overline{OE}$ Access Time (ns)	25	30	40	35

Note:*1,All of V_{ccf}_1, V_{ccf}_2, V_{ccr} and V_{ccs} must be the same level when either part is being accessed.

■ PACKAGE

115-pin plastic FBGA T.B.D. BGA-115P-Mxx

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— FLASH MEMORY_1

- **0.13 μm Process Technology**
- **Dual CE function**
- **Single 3.0 V read, program and erase**
  Minimized system level power requirements
- **Simultaneous Read/Write operations (Dual Bank)**
- **FlexBank™**
  Bank A: 16 Mbit (4 KW ×8 and 32 KW ×31)
  Bank B: 48 Mbit (32 KW ×96)
  Bank C: 48 Mbit (32 KW ×96)
  Bank D: 16 Mbit (4 KW ×8 and 32 KW ×31)
- **High Performance Page Mode**
  20 ns maximum page access time (55ns random access time)
- **8 words Page (x16)**
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Minimum 100,000 program/erase cycles**
- **Sector erase architecture**
  Eight 4 Kwords, two hundred fifty-four 32 Kwords, eight 8 Kwords sectors.
  Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Dual Boot Block**
  16 4Kwords bootblock sectors, 8 at the top of the address range and 8 at the bottom of the address range
- **$\overline{\text{WP}}$/ACC input pin**
  At V_{IL}, allows protection of “outermost” 2×4 K words on both ends of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Embedded Erase™ Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$_1)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Hardware Reset Pin ($\overline{\text{RESET}}$_1)**
  Hardware method to reset the device for reading array dataNew Sector Protection
  Persistent Sector Protection
  Password Sector Protection
- **Please refer to “MBM29QM12DH“ Datasheet in deteiled function**

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— FLASH MEMORY_2

- **Simultaneous Read/Write Operations** (**Dual Bank**)
- **FlexBank™**
  Bank A : 8 Mbit (8 KB × 8 and 64 KB × 15)
  Bank B : 24 Mbit (64 KB × 48)
  Bank C : 24 Mbit (64 KB × 48)
  Bank D : 8 Mbit (8 KB × 8 and 64 KB × 15)
  Two virtual Banks are chosen from the combination of four physical banks.
  Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.
  Read-while-erase
  Read-while-program
- **Minimum 100,000 Program/Erase Cycles**
- **Sector Erase Architecture**
  Sixteen 4 Kword and one hundred twenty-six 32 Kword sectors in word.
  Any combination of sectors can be concurrently erased. It also supports full chip erase.
- **Hidden ROM** (**Hi-ROM**) **Region**
  256 byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC Input Pin**
  At V_{IL}, allows protection of “outermost” 2 × 8 Kbytes on both ends of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Embedded Erase™ Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready/Busy Output (RY/$\overline{\text{BY}}$_2)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V_{CC}f write Inhibit ≤ 2.5 V**
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Please Refer to “MBM29DL64DF” Datasheet in Detailed Function.**

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— FCRAM

- **Power Dissipation**
  Operating : 25 mA max.
  Standby : 200 μA max.
- **Power Down Mode**
  Sleep : 10 μA max.
  NAP : 65 μA max.
  16M Partial : 85 μA max.
- **Power Down Control by CE2r**
- **Byte Write Control: $\overline{LB}$(DQ_7-DQ_0), $\overline{UB}$(DQ_{15}-DQ_8)**
- **8 words Address Access Capability**

— SRAM

- **Power Dissipation**
  Operating : 50 mA Max.
  Standby : 15 μA Max.
- **Power Down Features using $\overline{CE1}$s and CE2s**
- **Data Retention Supply Voltage: 1.5 V to 3.1 V**
- **$\overline{CE1}$s and CE2s Chip Select**
- **Byte Data Control: $\overline{LB}$ (DQ_7-DQ_0), $\overline{UB}$ (DQ_{15}-DQ_8)**

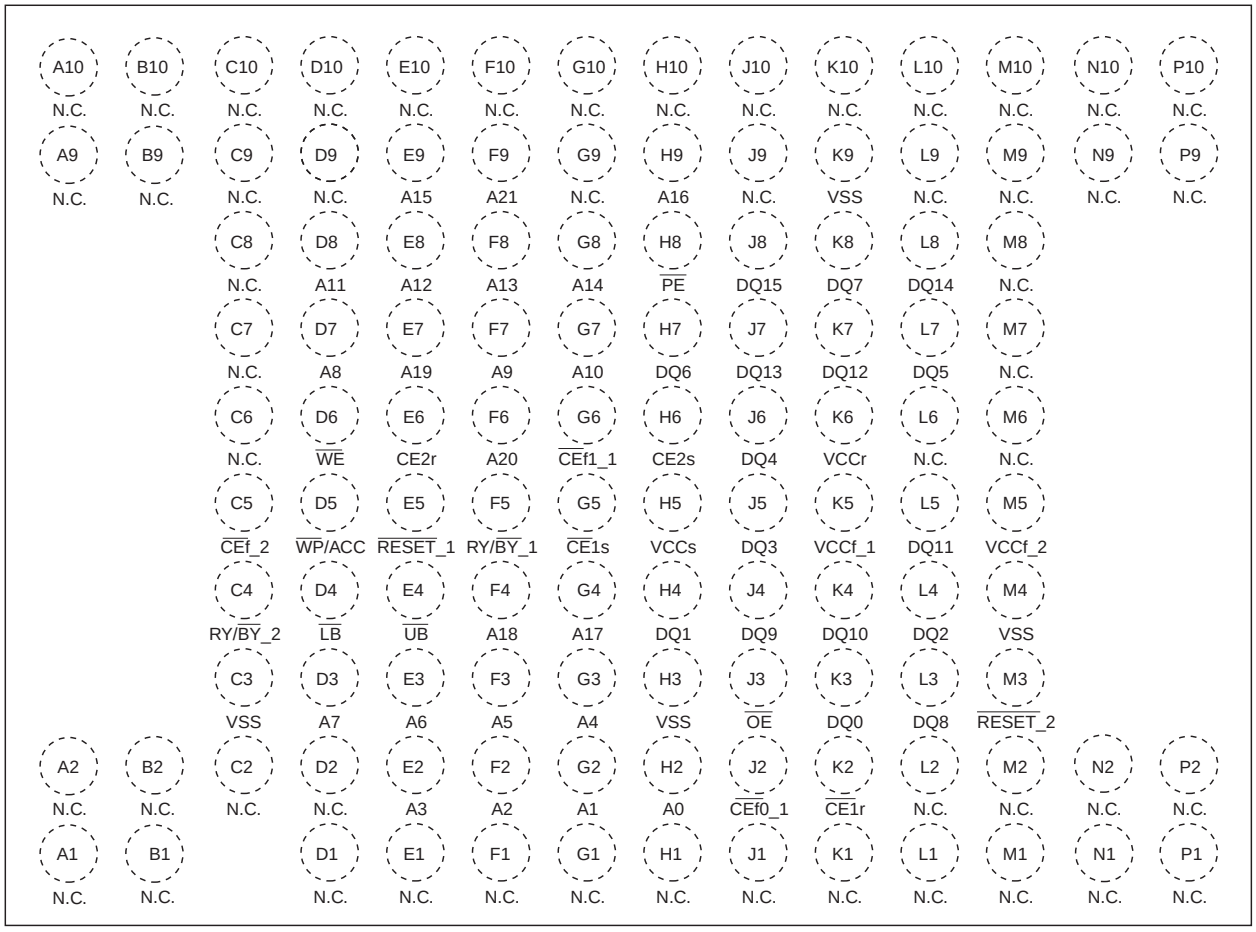
*: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

*: Mobile FCRAM™ is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

(Top View)
Marking Side

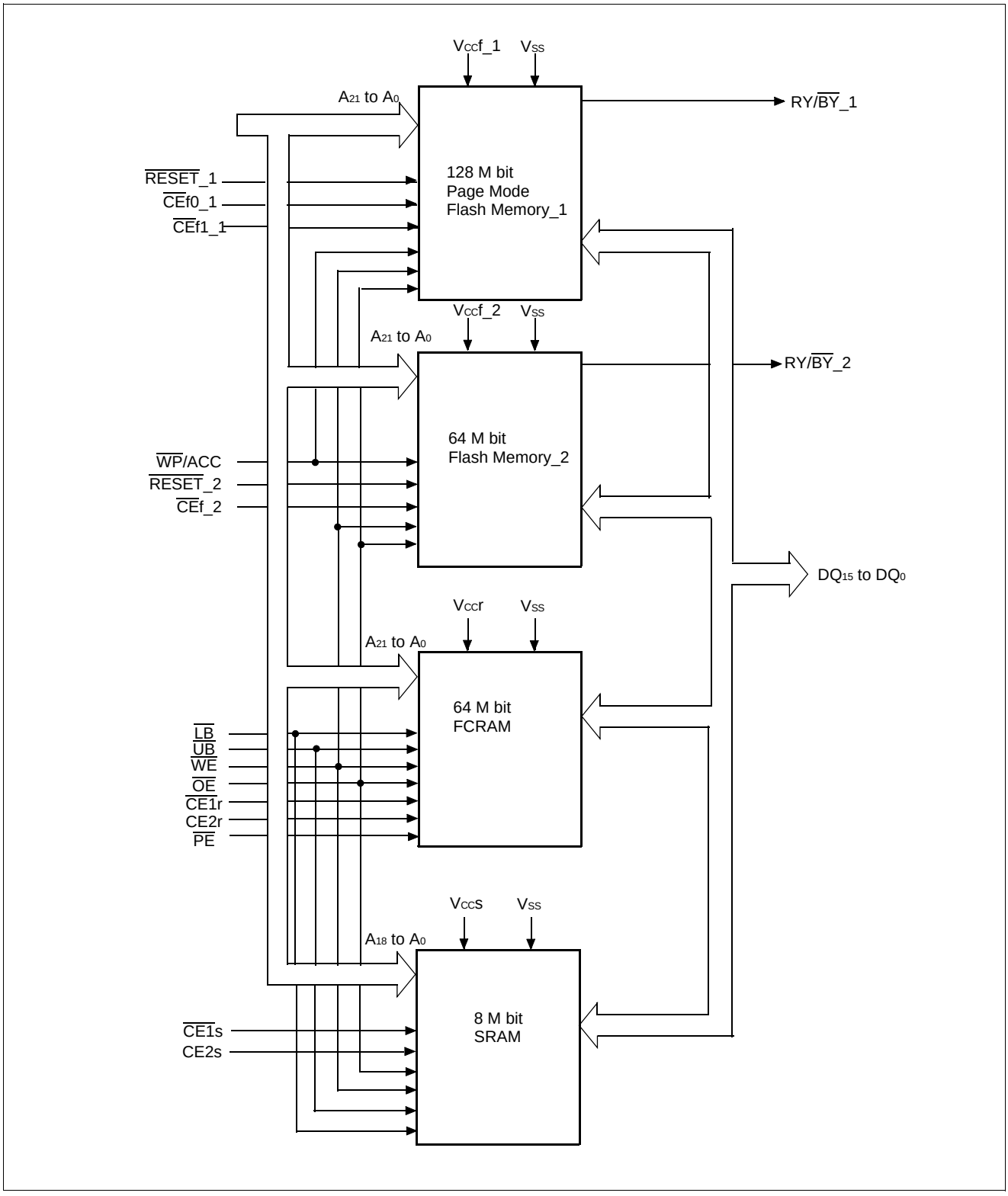


(BGA-115P-Mxx)

■ PIN DESCRIPTION

Pin name	Input/ Output	Description
A_{18} to A_0	I	Address Inputs (Common)
A_{21} to A_{19}	I	Address Inputs (FCRAM & Flash_1& Flash_2)
DQ_{15} to DQ_0	I/O	Data Inputs/Outputs (Common)
$\overline{CE}$f0_1	I	Chip Enable (Flash_1)
$\overline{CE}$f1_1	I	Chip Enable (Flash_1)
$\overline{CE}$f_2	I	Chip Enable (Flash_2)
$\overline{CE1}$r	I	Chip Enable (FCRAM)
$\overline{CE1}$s	I	Chip Enable (SRAM)
CE2r	I	Chip Enable (FCRAM)
CE2s	I	Chip Enable (SRAM)
$\overline{OE}$	I	Output Enable (Common)
$\overline{WE}$	I	Write Enable (Common)
RY/$\overline{BY}$_1	O	Ready/Busy Output (Flash_1) Open Drain Output
RY/$\overline{BY}$_2	O	Ready/Busy Output (Flash_2) Open Drain Output
$\overline{UB}$	I	Upper Byte Control (FCRAM & SRAM)
$\overline{LB}$	I	Lower Byte Control (FCRAM & SRAM)
$\overline{RESET}$_1	I	Hardware Reset Pin/Sector Protection Unlock (Flash_1)
$\overline{RESET}$_2	I	Hardware Reset Pin/Sector Protection Unlock (Flash_2)
$\overline{WP}$/ACC	I	Write Protect / Acceleration (Flash_1& Flash_2)
$\overline{PE}$	I	Partial Enable (FCRAM)
N.C.	—	No Internal Connection
V_{SS}	Power	Device Ground (Common)
V_{CC}f_1	Power	Device Power Supply (Flash_1)
V_{CC}f_2	Power	Device Power Supply (Flash_2)
V_{CC}r	Power	Device Power Supply (FCRAM)
V_{CC}s	Power	Device Power Supply (SRAM)

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

Operation (1), (2)	$\overline{CEf0\_1}$	$\overline{CEf1\_1}$	$\overline{CEf\_2}$	$\overline{CE1r}$	CE2r	$\overline{CE1s}$	CE2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$\overline{PE}$	A_{21} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET\_1}$	$\overline{RESET\_2}$	$\overline{WP/ACC(12)}$
Full Standby	H	H	H	H	H	H	X	X	X	X	X	H	X	High-Z	High-Z	H	H	X
						X	L											
Output Disable(3)	H	H	H	L	H	H	X	H	H	X	X	H	X (10)	High-Z	High-Z	H	H	X
						X	L											
	H	H	H	H	H	L	H	H	H	X	X		X					
								X	X	H	H							
	L	H	H	H		H	X	H	H	X	X							
						X	L											
	H	L	H	H		H	X											
						X	L											
	H	H	L	H		H	X											
						X	L											
Read from Flash_1 (4)	L	H	H	H	H	H	X	L	H	X	X	H	Valid	D_{OUT}	D_{OUT}	H	H	X
						X	L											
	H	L	H	H	H	H	X	L	H	X	X	H	Valid	D_{OUT}	D_{OUT}	H	H	X
						X	L											
Read from Flash_2 (4)	H	H	L	H	H	H	X	L	H	X	X	H	Valid	D_{OUT}	D_{OUT}	H	H	X
						X	L											
Write to Flash _1	L	H	H	H	H	H	X	H	L	X	X	H	Valid	D_{IN}	D_{IN}	H	H	X
						X	L											
	H	L	H	H	H	H	X	H	L	X	X	H	Valid	D_{IN}	D_{IN}	H	H	X
						X	L											
Write to Flash_2	H	H	L	H	H	H	X	H	L	X	X	H	Valid	D_{IN}	D_{IN}	H	H	X
						X	L											
Read from FCRAM(5)	H	H	H	L	H	H	X	L	H	L (9)	L (9)	H	Valid	D_{OUT}	D_{OUT}	H	H	X
						X	L											
Write to FCRAM	H	H	H	L	H	H	X	H	L	L	L	H	Valid	D_{IN}	D_{IN}	H	H	X
										H	L			High-Z	D_{IN}			
										L	H			D_{IN}	High-Z			
						X	L			L	L	H	Valid	D_{IN}	D_{IN}			
										H	L			High-Z	D_{IN}			
										L	H			D_{IN}	High-Z			
Read from SRAM	H	H	H	H	H	L	H	L	H	L	L	H	Valid	D_{OUT}	D_{OUT}	H	H	X
										H	L			High-Z	D_{OUT}			
										L	H			D_{OUT}	High-Z			
Write to SRAM	H	H	H	H	H	L	H	H	L	L	L	H	Valid	D_{IN}	D_{IN}	H	H	X
										H	L			High-Z	D_{IN}			
										L	H			D_{IN}	High-Z			

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Operation (1), (2)	$\overline{CE}$0f_1	$\overline{CE}$1f_1	$\overline{CE}$f_2	$\overline{CE}$1r	CE2r	$\overline{CE}$1s	CE2s	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$\overline{PE}$	A_{21} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$_1	$\overline{RESET}$_2	$\overline{WP}$/ ACC(12)
Flash_1 Temporary Sector Group Unprotection(6)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X	X
Flash_ 2 Temporary Sector Group Unprotection(6)	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash_1 Hardware Reset	X	X	X	H	H	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X	X
						X	L											
Flash_2 Hardware Reset	X	X	X	H	H	H	X	X	X	X	X	X	X	High-Z	High-Z	X	L	X
						X	L											
Flash_1 or 2 Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
FCRAM Power Down Program	H	H	H	H	H	H	X	X	X	X	X	L	KEY (11)	High-Z	High-Z	H	H	X
						X	L											
FCRAM NO READ (7)	H	H	H	L	H	H	X	L	H	H	H	H	Valid	High-Z	High-Z	H	H	X
						X	L											
FCRAM Power Down (8)	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes:
1. Other operations except for indicated this column are inhibited.
2. Do not apply for a following state two or more on the same time;
   1) $\overline{CE}$f0_1 = V_{IL}, 2) $\overline{CE}$f1_1 = V_{IL}, 3)$\overline{CE}$f_2 = V_{IL}, 4) $\overline{CE}$1r = V_{IL} and CE2r = V_{IH},
   5) $\overline{CE}$1s = V_{IL} and CE2s = V_{IH}
3. FCRAM Output Disable condition should not be kept longer than 1µs.
4. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
5. FCRAM $\overline{LB}$, $\overline{UB}$ control at Read operation is not supported.
6. It is also used for the extended sector group protections.
7. The FCRAM Power Down Program can be performed one time after compliance of Power-UP timings and it should not be re-programmed after regular Read or Write.
8. FCRAM Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. I_{PD}r current and data retention depends on the selection of Power Down Program.
9. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low for FCRAM Read Operation.
10. Can be either V_{IL} or V_{IH} but must be valid before Read or Write.
11. See " FCRAM Power Down Program Key Table " in FCRAM Part.
12. Protect " outer most " 2x8K bytes (4 words) on both ends of the boot block sectors.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–30	+85	°C
Voltage with Respect to Ground All pins except $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2,$\overline{\text{WP}}$/ACC *1	V_{IN}, V_{OUT}	–0.3	V_{CC}f_1 +0.3	V
			V_{CC}f_2 +0.3	V
			V_{CC}r +0.3	V
			V_{CC}s +0.3	V
V_{CC}f_1/V_{CC}f_2/V_{CC}r/V_{CC}s Supply *1	V_{CC}f_1,V_{CC}f_2, V_{CC}r, V_{CC}s	–0.3	+3.3	V
$\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 *2	V_{IN}	–0.5	+ 13.0	V
$\overline{\text{WP}}$/ACC *3	V_{IN}	–0.5	+10.5	V

*1 Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC}f_1 + 0.3 V or V_{CC}f_2 + 0.3 V or V_{CC}r + 0.3 V or V_{CC}s + 0.3 V. During voltage transitions, input or I/O pins may overshoot to V_{CC}f_1 + 2.0 V or V_{CC}f_2 + 2.0 V or V_{CC}r + 1.0 V or V_{CC}s + 2.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 pin is –0.5 V. During voltage transitions $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns.
Voltage difference between input and supply voltage (VIN-V_{CC}f_1 or V_{CC}f_2) does not exceed +9.0 V.
Maximum DC input voltage on $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3: Minimum DC input voltage on $\overline{\text{WP}}$/ACC pin is –0.5 V. During voltage transitions, $\overline{\text{WP}}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP}}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when V_{CC}f_1 or V_{CC}f_2 is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T_A	–25	+85	°C
V_{CC}f_1/V_{CC}f_2/V_{CC}r/V_{CC}s Supply Voltages	V_{CC}f_1,V_{CC}f_2,V_{CC}r,V_{CC}s	+2.7	+3.1	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

■ ELECTRICAL CHARACTERISTICS (DC Characteristics)

Parameter	Sym-bol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{CCf}_1,V_{CCr},V_{CCs}		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to V_{CCf}_1,V_{CCr},V_{CCs}		–1.0	—	+1.0	µA
$\overline{RESET}$ Inputs Leakage Current (Flash_1 & Flash_2)	I_{LIT}	V_{CCf} = V_{CCf} Max., $\overline{RESET}$ = 12.5 V		—	—	35	µA
$\overline{WP}$/ACC Acceleration Program Current (Flash_1 & Flash_2)	I_{ACC}	V_{CCf} = V_{CCf} Max., $\overline{WP}$/ACC = V_{ACC} Max.		—	—	20	mA
Flash_1 V_{CC} Active Current (Read) *1	$I_{CC1}f_1$	$\overline{CE}$ ($\overline{CE0f}$ or $\overline{CE1f}$) = V_{IL}, $\overline{OE}$f= V_{IH}	f = 10 MHz	—	—	45	mA
		$\overline{CE}$ ($\overline{CE0f}$ or $\overline{CE1f}$) = V_{IL}, $\overline{OE}$f= V_{IH}	f = 5 MHz	—	—	20	mA
Flash_1 V_{CC} Active Current *2	$I_{CC2}f_1$	$\overline{CE}$ ($\overline{CE0f}$ or $\overline{CE1f}$) = V_{IL}, $\overline{OE}$f= V_{IH}		—	—	25	mA
Flash_1 V_{CC} Current (Standby)	$I_{SB1}f_1$	V_{CCf} = V_{CCf} Max., $\overline{CE0f}$, $\overline{CE1f}$ = V_{CCf} ±0.3 V, $\overline{RESET}$= V_{CCf} ±0.3 V, $\overline{WP}$/ACC = V_{CCf} ±0.3 V		—	1	5	µA
Flash_1 V_{CC} Current (Standby,Reset)	$I_{SB2}f_1$	V_{CCf} = V_{CCf} Max., $\overline{RESET}$= V_{SS} ±0.3 V,		—	1	5	µA
Flash_1 V_{CC} Current (Automatic Sleep Mode)*3	$I_{SB3}f_1$	V_{CCf} = V_{CCf} Max., $\overline{CE0f}$, $\overline{CE1f}$= V_{SS} ±0.3 V, $\overline{RESET}$= V_{CCf} ±0.3 V, V_{IN} = V_{CCf} ±0.3 V or V_{SSf}±0.3 V		—	1	5	µA
Flash_1 V_{CC} Active Current (Read-while-Program)*5	$I_{CC3}f_1$	$\overline{CE}$ ($\overline{CE0f}$ or $\overline{CE1f}$) = V_{IL}, $\overline{OE}$f= V_{IH}		—	—	45	mA
Flash_1 V_{CC} Active Current (Read-while-Erase)	$I_{CC4}f_1$	$\overline{CE}$ ($\overline{CE0f}$ or $\overline{CE1f}$) = V_{IL}, $\overline{OE}$f= V_{IH}		—	—	45	mA
Flash_1 V_{CC} Active Current (Erase-while-Program)*5	$I_{CC5}f_1$	$\overline{CE}$ ($\overline{CE0f}$ or $\overline{CE1f}$) = V_{IL}, $\overline{OE}$f= V_{IH}		—	—	25	mA
Flash_2 V_{CC} Active Current (Read) *1	$I_{CC1}f_2$	$\overline{CE}$f = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} =5 MHz	—	—	18	mA
			t_{CYCLE} =1 MHz	—	—	4	mA
Flash_2 V_{CC} Active Current (Program/Erase) *2	$I_{CC2}f_2$	$\overline{CE}$f = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	35	mA
Flash_2 V_{CC} Active Current (Read-While-Program) *5	$I_{CC3}f_2$	$\overline{CE}$f = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	53	mA
Flash_2 V_{CC} Active Current (Read-While-Erase) *5	$I_{CC4}f_2$	$\overline{CE}$f = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	53	mA
Flash_2 V_{CC} Active Current (Erase-Suspend-Program)	$I_{CC5}f_2$	$\overline{CE}$f = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	40	mA
Flash_2 V_{CC} Standby Current	$I_{SB1}f$	V_{CCf} = V_{CCf} Max., $\overline{CE}$f = V_{CCf} ± 0.3 V, $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V		—	1 *7	5 *7	µA
Flash_2 V_{CC} Standby Current ($\overline{RESET}$)	$I_{SB2}f$	V_{CCf} = V_{CCf} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V		—	1 *7	5 *7	µA
Flash_2 V_{CC} Current (Automatic Sleep Mode) *3	$I_{SB3}f$	V_{CCf} = V_{CCf} Max., $\overline{CE}$f = V_{SS} ± 0.3 V, $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V, V_{IN} = V_{CCf}± 0.3 V or V_{SS} ± 0.3 V		—	1 *7	5 *7	µA
FCRAM V_{CC} Active Current	$I_{CC1}r$	V_{CCr} = V_{CCr} Max., $\overline{CE1r}$ = V_{IL}, CE2r = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	t_{RC} / t_{WC} =min.	—	—	25	mA
			t_{RC} / t_{WC} =1µs	—	—	3	
SRAM V_{CC} Active Current	$I_{CC1}s$	V_{CCs} = V_{CCs} Max., $\overline{CE1s}$ = V_{IL}, CE2s = V_{IH}	t_{CYCLE} =10 MHz	—	—	50	mA
SRAM V_{CC} Active Current	$I_{CC2}s$	$\overline{CE1s}$ = 0.2 V, CE2s = V_{CCs} – 0.2 V	t_{CYCLE} =10 MHz	—	—	50	mA
			t_{CYCLE} =1 MHz	—	—	10	mA

(Continued)

(Continued)

Parameter	Sym-bol	Conditions		Value			Unit
				Min.	Typ.	Max.	
FCRAM V_{CC} Standby Current	$I_{SB1}r$	$V_{CC}r$ = $V_{CC}r$ Max., $\overline{CE1}r \geq V_{CC}r - 0.2V$, $CE2r \geq V_{CC}r - 0.2V$, $V_{IN} \leq 0.2$ V or $V_{CC}r - 0.2$ V		—	—	150	µA
FCRAM V_{CC} Power Down Current	$I_{PDS}r$	$V_{CC}r$ = $V_{CC}r$ Max., $\overline{CE1}r \geq V_{CC}r - 0.2V$, $CE2r \leq 0.2V$, V_{IN} Cycle time = t_{RC} min.	Sleep	—	—	10	µA
	$I_{PDN}r$		NAP	—	—	65	µA
	$I_{PD8}r$		16M Partial	—	—	85	µA
SRAM V_{CC} Standby Current	$I_{SB1}s$	$\overline{CE1}s \geq V_{CC}s - 0.2$ V, $CE2s \geq V_{CC}s - 0.2$ V		—	—	15	µA
SRAM V_{CC} Standby Current	$I_{SB2}s$	$CE2s \leq 0.2V$		—	—	15	µA
Input Low Level	V_{IL}	—		–0.3	—	0.5	V
Input High Level	V_{IH}	—		2.2	—	V_{CC}+ 0.3 *6	V
Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$) *4	V_{ID}	—		11.5	—	12.5	V
Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration *4	V_{ACC}	—		8.5	9.0	9.5	V
Output Low Voltage Level	$V_{OL}f$	$V_{CC}f$ = $V_{CC}f$ Min., I_{OL}=4.0 mA	Flash_1& Flash_2	—	—	0.45	V
	$V_{OL}r$	$V_{CC}r$ = $V_{CC}r$ Min., I_{OL} =1.0mA	FCRAM	—	—	0.4	V
	$V_{OL}s$	$V_{CC}s$ = $V_{CC}s$ Min., I_{OL}=1.0 mA	SRAM	—	—	0.4	V
Output High Voltage Level	$V_{OH}f$	$V_{CC}f$ = $V_{CC}f$ Min., I_{OH}=–0.1 mA	Flash_1& Flash_2	$V_{CC}f$– 0.4	—	—	V
	$V_{OH}r$	$V_{CC}r$ = $V_{CC}r$ Min., I_{OH} =–0.5mA	FCRAM	2.2	—	—	V
	$V_{OH}s$	$V_{CC}s$ = $V_{CC}s$ Min., I_{OH}=–0.5 mA	SRAM	2.2	—	—	V
Flash Low $V_{CC}f$ Lock-Out Voltage	V_{LKO}	—		2.3	2.4	2.5	V

Legend: Flash means Flash_1 or Flash_2, $V_{CC}f$ means $V_{CC}f\_1$ or $V_{CC}f\_2$, $V_{SS}f$ means $V_{SS}f\_1$ or $V_{SS}f\_2$, $\overline{CE}f$ means $\overline{CE}f\_1$ or $\overline{CE}f\_2$, $\overline{RESET}$ means $\overline{RESET}\_1$ or $\overline{RESET}\_2$

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: Applicable for only $V_{CC}f$ applying.

*5: Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

*6: V_{CC} indicates lower of $V_{CC}f\_1$ or $V_{CC}f\_2$ or $V_{CC}s$ or $V_{CC}r$.

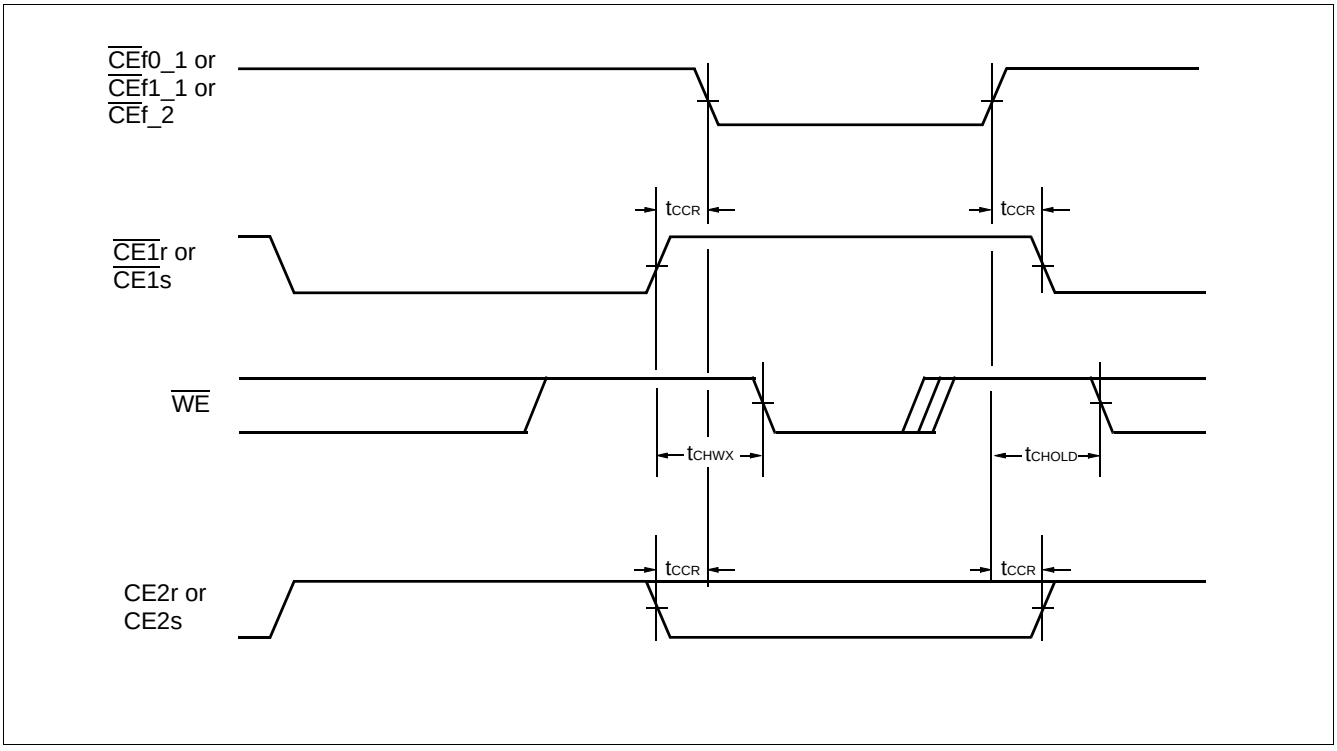
*7: Actual Standby Current is twice of what is indicated in the table, due to two Flash memory chips embedment withn one device.

■ ELECTRICAL CHARACTERISTICS (AC Characteristics)

- **$\overline{CE}$ Timing**

Parameter	Symbol		Condition	Value		Unit
	JEDEC	Standard		Min.	Max.	
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	—	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	—	ns
$\overline{CE1}$r, $\overline{CE1}$s High to $\overline{WE}$ Invalid time for Standby Entry	—	t_{CHWX}	—	10	—	ns

- **Timing Diagram for alternating RAM to Flash_1 or Flash_2**



- **Flash_1 Characteristics**
  Please refer to “128M Page Flash Memory for MCP“ part. In this part, Flash means Flash_1, V_{CC}f means V_{CC}f_1, V_{SS}f means V_{SS}f_1, $\overline{CE}$f0 means $\overline{CE}$f0_1, $\overline{CE}$f0 means $\overline{CE}$f1_1, $\overline{RESET}$ means $\overline{RESET}$_1

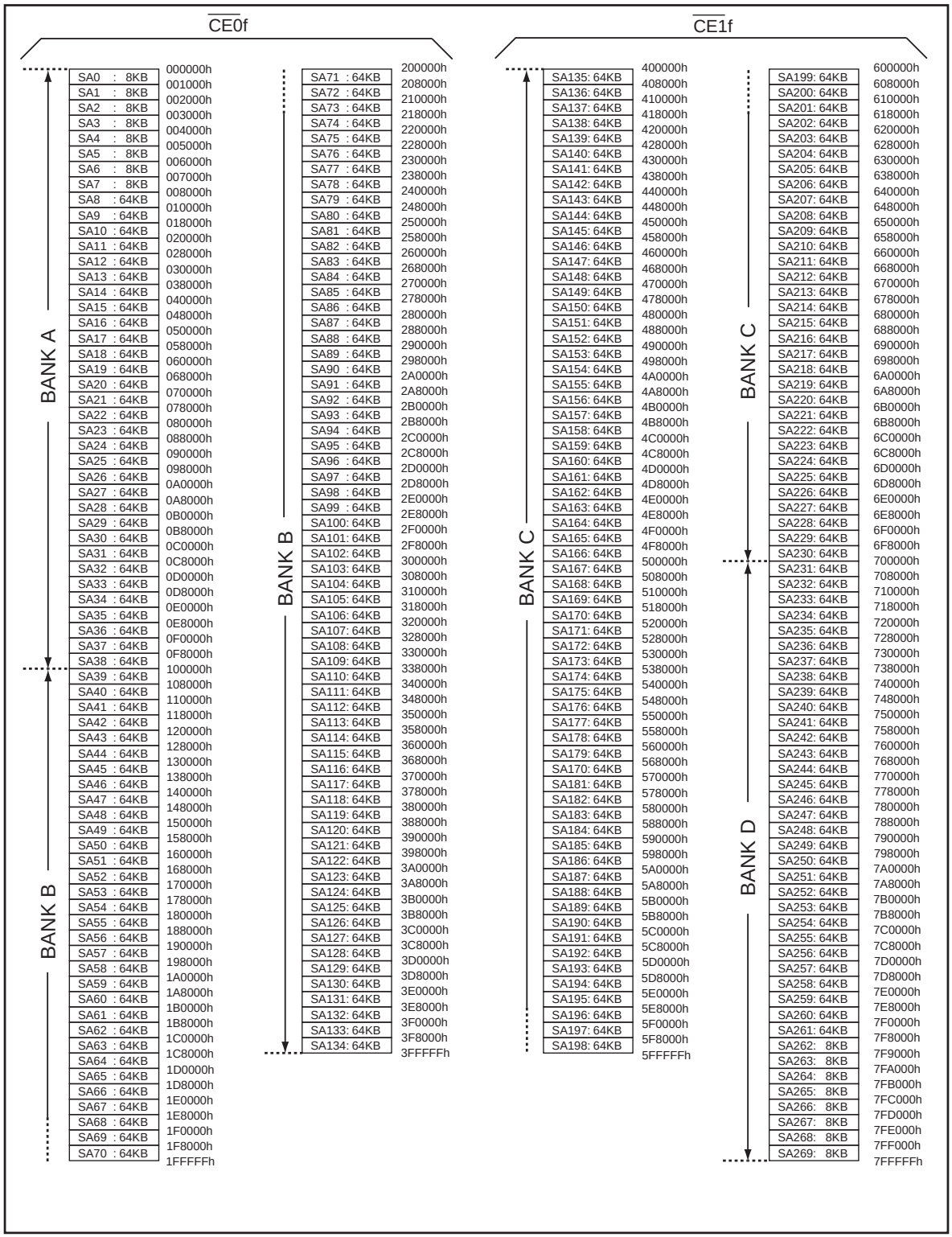
- **Flash_2 Characteristics**
  Please refer to “64M Flash Memory for MCP“ part. In this part, Flash means Flash_2, V_{CC}f means V_{CC}f_2, V_{SS}f means V_{SS}f_2, $\overline{CE}$f means $\overline{CE}$f _2, $\overline{RESET}$ means $\overline{RESET}$_2

- **FCRAM Characteristics**
  Please refer to “64M FCRAM for MCP“ part.

- **SRAM Characteristics,**
  Please refer to “8M SRAM for MCP“ part.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Sixteen 4K words, and two hundred fifty-four 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



128M Page Flash for MCP

•FlexBank™ Architecture

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	16 Mbit	Bank A	112 Mbit	Remainder (Bank B, C, D)
2	48 Mbit	Bank B	80 Mbit	Remainder (Bank A, C, D)
3	48 Mbit	Bank C	80 Mbit	Remainder (Bank A, B, D)
4	16 Mbit	Bank D	112 Mbit	Remainder (Bank A, B, C)

•Example of Virtual Banks Combination

Bank Splits	Bank 1			Bank 2		
	Volume	Combination	Sector Size	Volume	Combination	Sector Size
1	16 Mbit	Bank A	8 × 4 Kword + 31 x 32 Kword	112 Mbit	Bank B + Bank C + Bank D	8 x 4 Kword + 223 x 32 Kword
2	32 Mbit	Bank A + Bank D	16 x 4 Kword + 62 x 32 Kword	96 Mbit	Bank B + Bank C	192 x 32 Kword
3	48 Mbit	Bank B	96 x 32 Kword	80 Mbit	Bank A + Bank C + Bank D	16 x 4 Kword + 158 x 32 Kword
4	64 Mbit	Bank A + Bank B	8 x 4 Kword + 127 x 32 Kword	64 Mbit	Bank C + Bank D	8 x 4 Kword + 127 x 32 Kword

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

•Simultaneous Operation(Dual $\overline{CE}$)

The device features functions that enable reading of data from one memory bank while a program or erase operation is in progress in the other memory bank (simultaneous operation) , in addition to conventional features (read, program, erase, erase-suspend read, and erase-suspend program) . The bank can be selected by bank address (A_{21}, A_{20}) with zero latency. The device consists of the following four banks :
$\overline{CE0}$ controll: Bank A : 8 x 4 KW and 31 x 32 KW; Bank B : 96 x 32 KW
$\overline{CE1}$ controll: Bank C : 96 x 32 KW; Bank D : 8 x 4 KW and 31 x 32 KW.
Table 12 shows the possible combinations for simultaneous operation. ((Refer to Figure 11 Bank-to-Bank Read/ Write Timing Diagram.)

•Simultaneous Operation for Dual CE

Case	Bank 1 ($\overline{CE0}$) Status 16 Mbit	Bank 2 ($\overline{CE0}$) Status 48 Mbit	Bank 1 ($\overline{CE1}$) Status 48 Mbit	Bank 2 ($\overline{CE1}$) Status 16 Mbit
1	Read mode	Read mode	Read mode	Read mode
2	Autoselect mode	Read mode	Read mode	Read mode
3	Read mode	Autoselect mode	Read mode	Read mode
4	Read mode	Read mode	Autoselect mode	Read mode
5	Read mode	Read mode	Read mode	Autoselect mode
6	Program mode	Read mode	Read mode	Read mode
7	Read mode	Program mode	Read mode	Read mode
8	Read mode	Read mode	Program mode	Read mode
9	Read mode	Read mode	Read mode	Program mode
10	Erase Mode	Read mode	Read mode	Read mode
11	Read mode	Erase Mode	Read mode	Read mode
12	Read mode	Read mode	Erase Mode	Read mode
13	Read mode	Read mode	Read mode	Erase Mode
14*1	Multiple Erase Mode	Multiple Erase Mode	Read mode	Read mode
15*1	Multiple Erase Mode	Read mode	Multiple Erase Mode	Read mode
16*1	Multiple Erase Mode	Read mode	Read mode	Multiple Erase Mode
17*1	Read mode	Multiple Erase Mode	Multiple Erase Mode	Read mode
18*1	Read mode	Multiple Erase Mode	Read mode	Multiple Erase Mode
19*1	Read mode	Read mode	Multiple Erase Mode	Multiple Erase Mode
20*1	Multiple Erase Mode	Multiple Erase Mode	Multiple Erase Mode	Read mode
21*1	Multiple Erase Mode	Multiple Erase Mode	Read mode	Multiple Erase Mode
22*1	Multiple Erase Mode	Read mode	Multiple Erase Mode	Multiple Erase Mode
23*1	Read mode	Multiple Erase Mode	Multiple Erase Mode	Multiple Erase Mode

*1: Multiple Erase Mode requires muliple sector erase sequence which is followed by writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than "t_{TOW}". (Refer to Sector Erase section.)

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

•Sector Address Tables (Bank A)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kwords)	(×16) Address Range
				Bank Address											
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank A	SA0	0	1	0	0	0	0	0	0	0	0	0	0	4	000000h to 000FFFh
	SA1	0	1	0	0	0	0	0	0	0	0	0	1	4	001000h to 001FFFh
	SA2	0	1	0	0	0	0	0	0	0	0	1	0	4	002000h to 002FFFh
	SA3	0	1	0	0	0	0	0	0	0	0	1	1	4	003000h to 003FFFh
	SA4	0	1	0	0	0	0	0	0	0	1	0	0	4	004000h to 004FFFh
	SA5	0	1	0	0	0	0	0	0	0	1	0	1	4	005000h to 005FFFh
	SA6	0	1	0	0	0	0	0	0	0	1	1	0	4	006000h to 006FFFh
	SA7	0	1	0	0	0	0	0	0	0	1	1	1	4	007000h to 007FFFh
	SA8	0	1	0	0	0	0	0	0	1	X	X	X	32	008000h to 00FFFFh
	SA9	0	1	0	0	0	0	0	1	0	X	X	X	32	010000h to 017FFFh
	SA10	0	1	0	0	0	0	0	1	1	X	X	X	32	018000h to 01FFFFh
	SA11	0	1	0	0	0	0	1	0	0	X	X	X	32	020000h to 027FFFh
	SA12	0	1	0	0	0	0	1	0	1	X	X	X	32	028000h to 02FFFFh
	SA13	0	1	0	0	0	0	1	1	0	X	X	X	32	030000h to 037FFFh
	SA14	0	1	0	0	0	0	1	1	1	X	X	X	32	038000h to 03FFFFh
	SA15	0	1	0	0	0	1	0	0	0	X	X	X	32	040000h to 047FFFh
	SA16	0	1	0	0	0	1	0	0	1	X	X	X	32	048000h to 04FFFFh
	SA17	0	1	0	0	0	1	0	1	0	X	X	X	32	050000h to 057FFFh
	SA18	0	1	0	0	0	1	0	1	1	X	X	X	32	058000h to 05FFFFh
	SA19	0	1	0	0	0	1	1	0	0	X	X	X	32	060000h to 06FFFFh
	SA20	0	1	0	0	0	1	1	0	1	X	X	X	32	068000h to 06FFFFh
	SA21	0	1	0	0	0	1	1	1	0	X	X	X	32	070000h to 077FFFh
	SA22	0	1	0	0	0	1	1	1	1	X	X	X	32	078000h to 07FFFFh
	SA23	0	1	0	0	1	0	0	0	0	X	X	X	32	080000h to 087FFFh
	SA24	0	1	0	0	1	0	0	0	1	X	X	X	32	088000h to 08FFFFh
	SA25	0	1	0	0	1	0	0	1	0	X	X	X	32	090000h to 097FFFh
	SA26	0	1	0	0	1	0	0	1	1	X	X	X	32	098000h to 09FFFFh
	SA27	0	1	0	0	1	0	1	0	0	X	X	X	32	0A0000h to 0A7FFFh
	SA28	0	1	0	0	1	0	1	0	1	X	X	X	32	0A8000h to 0AFFFFh
	SA29	0	1	0	0	1	0	1	1	0	X	X	X	32	0B0000h to 0B7FFFh
	SA30	0	1	0	0	1	0	1	1	1	X	X	X	32	0B8000h to 0BFFFFh
	SA31	0	1	0	0	1	1	0	0	0	X	X	X	32	0C0000h to 0C7FFFh
	SA32	0	1	0	0	1	1	0	0	1	X	X	X	32	0C8000h to 0CFFFFh
	SA33	0	1	0	0	1	1	0	1	0	X	X	X	32	0D0000h to 0D7FFFh
	SA34	0	1	0	0	1	1	0	1	1	X	X	X	32	0D8000h to 0DFFFFh
	SA35	0	1	0	0	1	1	1	0	0	X	X	X	32	0E0000h to 0E7FFFh
	SA36	0	1	0	0	1	1	1	0	1	X	X	X	32	0E8000h to 0EFFFFh
	SA37	0	1	0	0	1	1	1	1	0	X	X	X	32	0F0000h to 0F7FFFh
	SA38	0	1	0	0	1	1	1	1	1	X	X	X	32	0F8000h to 0FFFFFh

•Sector Address Tables (Bank B)

Bank	Sector	Chip Enable		Sector Address									Sector Size (Kwords)	(×16) Address Range
				Bank Address										
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank B	SA39	0	1	0	1	0	0	0	0	0	X	X	X	32	100000h to 107FFFh
	SA40	0	1	0	1	0	0	0	0	1	X	X	X	32	108000h to 10FFFFh
	SA41	0	1	0	1	0	0	0	1	0	X	X	X	32	110000h to 117FFFh
	SA42	0	1	0	1	0	0	0	1	1	X	X	X	32	118000h to 11FFFFh
	SA43	0	1	0	1	0	0	1	0	0	X	X	X	32	120000h to 127FFFh
	SA44	0	1	0	1	0	0	1	0	1	X	X	X	32	128000h to 12FFFFh
	SA45	0	1	0	1	0	0	1	1	0	X	X	X	32	130000h to 137FFFh
	SA46	0	1	0	1	0	0	1	1	1	X	X	X	32	138000h to 13FFFFh
	SA47	0	1	0	1	0	1	0	0	0	X	X	X	32	140000h to 147FFFh
	SA48	0	1	0	1	0	1	0	0	1	X	X	X	32	148000h to 14FFFFh
	SA49	0	1	0	1	0	1	0	1	0	X	X	X	32	150000h to 157FFFh
	SA50	0	1	0	1	0	1	0	1	1	X	X	X	32	158000h to 15FFFFh
	SA51	0	1	0	1	0	1	1	0	0	X	X	X	32	160000h to 167FFFh
	SA52	0	1	0	1	0	1	1	0	1	X	X	X	32	168000h to 16FFFFh
	SA53	0	1	0	1	0	1	1	1	0	X	X	X	32	170000h to 177FFFh
	SA54	0	1	0	1	0	1	1	1	1	X	X	X	32	178000h to 17FFFFh
	SA55	0	1	0	1	1	0	0	0	0	X	X	X	32	180000h to 187FFFh
	SA56	0	1	0	1	1	0	0	0	1	X	X	X	32	188000h to 18FFFFh
	SA57	0	1	0	1	1	0	0	1	0	X	X	X	32	190000h to 197FFFh
	SA58	0	1	0	1	1	0	0	1	1	X	X	X	32	198000h to 19FFFFh
	SA59	0	1	0	1	1	0	1	0	0	X	X	X	32	1A0000h to 1A7FFFh
	SA60	0	1	0	1	1	0	1	0	1	X	X	X	32	1A8000h to 1AFFFFh
	SA61	0	1	0	1	1	0	1	1	0	X	X	X	32	1B0000h to 1B7FFFh
	SA62	0	1	0	1	1	0	1	1	1	X	X	X	32	1B8000h to 1BFFFFh
	SA63	0	1	0	1	1	1	0	0	0	X	X	X	32	1C0000h to 1C7FFFh
	SA64	0	1	0	1	1	1	0	0	1	X	X	X	32	1C8000h to 1CFFFFh
	SA65	0	1	0	1	1	1	0	1	0	X	X	X	32	1D0000h to 1D7FFFh
	SA66	0	1	0	1	1	1	0	1	1	X	X	X	32	1D8000h to 1DFFFFh
	SA67	0	1	0	1	1	1	1	0	0	X	X	X	32	1E0000h to 1E7FFFh
	SA68	0	1	0	1	1	1	1	0	1	X	X	X	32	1E8000h to 1EFFFFh
	SA69	0	1	0	1	1	1	1	1	0	X	X	X	32	1F0000h to 1F7FFFh
	SA70	0	1	0	1	1	1	1	1	1	X	X	X	32	1F8000h to 1FFFFFh
	SA71	0	1	1	0	0	0	0	0	0	X	X	X	32	200000h to 207FFFh
	SA72	0	1	1	0	0	0	0	0	1	X	X	X	32	208000h to 20FFFFh
	SA73	0	1	1	0	0	0	0	1	0	X	X	X	32	210000h to 217FFFh
	SA74	0	1	1	0	0	0	0	1	1	X	X	X	32	218000h to 21FFFFh
	SA75	0	1	1	0	0	0	1	0	0	X	X	X	32	220000h to 227FFFh
	SA76	0	1	1	0	0	0	1	0	1	X	X	X	32	228000h to 22FFFFh
	SA77	0	1	1	0	0	0	1	1	0	X	X	X	32	230000h to 237FFFh

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kwords)	(× 16) Address Range
				Bank Address											
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank B	SA78	0	1	1	0	0	0	1	1	1	X	X	X	32	238000h to 23FFFFh
	SA79	0	1	1	0	0	1	0	0	0	X	X	X	32	240000h to 247FFFh
	SA80	0	1	1	0	0	1	0	0	1	X	X	X	32	248000h to 24FFFFh
	SA81	0	1	1	0	0	1	0	1	0	X	X	X	32	250000h to 257FFFh
	SA82	0	1	1	0	0	1	0	1	1	X	X	X	32	258000h to 25FFFFh
	SA83	0	1	1	0	0	1	1	0	0	X	X	X	32	260000h to 267FFFh
	SA84	0	1	1	0	0	1	1	0	1	X	X	X	32	268000h to 26FFFFh
	SA85	0	1	1	0	0	1	1	1	0	X	X	X	32	270000h to 277FFFh
	SA86	0	1	1	0	0	1	1	1	1	X	X	X	32	278000h to 27FFFFh
	SA87	0	1	1	0	1	0	0	0	0	X	X	X	32	280000h to 287FFFh
	SA88	0	1	1	0	1	0	0	0	1	X	X	X	32	288000h to 28FFFFh
	SA89	0	1	1	0	1	0	0	1	0	X	X	X	32	290000h to 297FFFh
	SA90	0	1	1	0	1	0	0	1	1	X	X	X	32	298000h to 29FFFFh
	SA91	0	1	1	0	1	0	1	0	0	X	X	X	32	2A0000h to 2A7FFFh
	SA92	0	1	1	0	1	0	1	0	1	X	X	X	32	2A8000h to 2AFFFFh
	SA93	0	1	1	0	1	0	1	1	0	X	X	X	32	2B0000h to 2B7FFFh
	SA94	0	1	1	0	1	0	1	1	1	X	X	X	32	2B8000h to 2BFFFFh
	SA95	0	1	1	0	1	1	0	0	0	X	X	X	32	2C0000h to 2C7FFFh
	SA96	0	1	1	0	1	1	0	0	1	X	X	X	32	2C8000h to 2CFFFFh
	SA97	0	1	1	0	1	1	0	1	0	X	X	X	32	2D0000h to 2D7FFFh
	SA98	0	1	1	0	1	1	0	1	1	X	X	X	32	2D8000h to 2DFFFFh
	SA99	0	1	1	0	1	1	1	0	0	X	X	X	32	2E0000h to 2E7FFFh
	SA100	0	1	1	0	1	1	1	0	1	X	X	X	32	2E8000h to 2EFFFFh
	SA101	0	1	1	0	1	1	1	1	0	X	X	X	32	2F0000h to 2F7FFFh
	SA102	0	1	1	0	1	1	1	1	1	X	X	X	32	2F8000h to 2FFFFFh
	SA103	0	1	1	1	0	0	0	0	0	X	X	X	32	300000h to 307FFFh
	SA104	0	1	1	1	0	0	0	0	1	X	X	X	32	308000h to 30FFFFh
	SA105	0	1	1	1	0	0	0	1	0	X	X	X	32	310000h to 317FFFh
	SA106	0	1	1	1	0	0	0	1	1	X	X	X	32	318000h to 31FFFFh
	SA107	0	1	1	1	0	0	1	0	0	X	X	X	32	320000h to 327FFFh
	SA108	0	1	1	1	0	0	1	0	1	X	X	X	32	328000h to 32FFFFh
	SA109	0	1	1	1	0	0	1	1	0	X	X	X	32	330000h to 337FFFh
	SA110	0	1	1	1	0	0	1	1	1	X	X	X	32	338000h to 33FFFFh
	SA111	0	1	1	1	0	1	0	0	0	X	X	X	32	340000h to 347FFFh
	SA112	0	1	1	1	0	1	0	0	1	X	X	X	32	348000h to 34FFFFh
	SA113	0	1	1	1	0	1	0	1	0	X	X	X	32	350000h to 357FFFh
	SA114	0	1	1	1	0	1	0	1	1	X	X	X	32	358000h to 35FFFFh
	SA115	0	1	1	1	0	1	1	0	0	X	X	X	32	360000h to 367FFFh
	SA116	0	1	1	1	0	1	1	0	1	X	X	X	32	368000h to 36FFFFh

(Continued)

(Continued)

Bank	Sector	Chip Enable		Sector Address									Sector Size (Kwords)	(×16) Address Range
				Bank Address										
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank B	SA117	0	1	1	1	0	1	1	1	0	X	X	X	32	370000h to 377FFFh
	SA118	0	1	1	1	0	1	1	1	1	X	X	X	32	378000h to 37FFFFh
	SA119	0	1	1	1	1	0	0	0	0	X	X	X	32	380000h to 387FFFh
	SA120	0	1	1	1	1	0	0	0	1	X	X	X	32	388000h to 38FFFFh
	SA121	0	1	1	1	1	0	0	1	0	X	X	X	32	390000h to 397FFFh
	SA122	0	1	1	1	1	0	0	1	1	X	X	X	32	398000h to 39FFFFh
	SA123	0	1	1	1	1	0	1	0	0	X	X	X	32	3A0000h to 3A7FFFh
	SA124	0	1	1	1	1	0	1	0	1	X	X	X	32	3A8000h to 3AFFFFh
	SA125	0	1	1	1	1	0	1	1	0	X	X	X	32	3B0000h to 3B7FFFh
	SA126	0	1	1	1	1	0	1	1	1	X	X	X	32	3B8000h to 3BFFFFh
	SA127	0	1	1	1	1	1	0	0	0	X	X	X	32	3C0000h to 3C7FFFh
	SA128	0	1	1	1	1	1	0	0	1	X	X	X	32	3C8000h to 3CFFFFh
	SA129	0	1	1	1	1	1	0	1	0	X	X	X	32	3D0000h to 3D7FFFh
	SA130	0	1	1	1	1	1	0	1	1	X	X	X	32	3D8000h to 3DFFFFh
	SA131	0	1	1	1	1	1	1	0	0	X	X	X	32	3E0000h to 3E7FFFh
	SA132	0	1	1	1	1	1	1	0	1	X	X	X	32	3E8000h to 3EFFFFh
	SA133	0	1	1	1	1	1	1	1	0	X	X	X	32	3F0000h to 3F7FFFh
	SA134	0	1	1	1	1	1	1	1	1	X	X	X	32	3F8000h to 3FFFFFh

•Table 5.3 Sector Address Tables (Bank C)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kwords)	(× 16) Address Range
				Bank Address											
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA135	1	0	0	0	0	0	0	0	0	X	X	X	32	400000h to 407FFFh
	SA136	1	0	0	0	0	0	0	0	1	X	X	X	32	408000h to 40FFFFh
	SA137	1	0	0	0	0	0	0	1	0	X	X	X	32	410000h to 417FFFh
	SA138	1	0	0	0	0	0	0	1	1	X	X	X	32	418000h to 41FFFFh
	SA139	1	0	0	0	0	0	1	0	0	X	X	X	32	420000h to 427FFFh
	SA140	1	0	0	0	0	0	1	0	1	X	X	X	32	428000h to 42FFFFh
	SA141	1	0	0	0	0	0	1	1	0	X	X	X	32	430000h to 437FFFh
	SA142	1	0	0	0	0	0	1	1	1	X	X	X	32	438000h to 43FFFFh
	SA143	1	0	0	0	0	1	0	0	0	X	X	X	32	440000h to 447FFFh
	SA144	1	0	0	0	0	1	0	0	1	X	X	X	32	448000h to 44FFFFh
	SA145	1	0	0	0	0	1	0	1	0	X	X	X	32	450000h to 457FFFh
	SA146	1	0	0	0	0	1	0	1	1	X	X	X	32	458000h to 45FFFFh
	SA147	1	0	0	0	0	1	1	0	0	X	X	X	32	460000h to 467FFFh
	SA148	1	0	0	0	0	1	1	0	1	X	X	X	32	468000h to 46FFFFh
	SA149	1	0	0	0	0	1	1	1	0	X	X	X	32	470000h to 477FFFh
	SA150	1	0	0	0	0	1	1	1	1	X	X	X	32	478000h to 47FFFFh
	SA151	1	0	0	0	1	0	0	0	0	X	X	X	32	480000h to 487FFFh
	SA152	1	0	0	0	1	0	0	0	1	X	X	X	32	488000h to 48FFFFh
	SA153	1	0	0	0	1	0	0	1	0	X	X	X	32	490000h to 497FFFh
	SA154	1	0	0	0	1	0	0	1	1	X	X	X	32	498000h to 49FFFFh
	SA155	1	0	0	0	1	0	1	0	0	X	X	X	32	4A0000h to 4A7FFFh
	SA156	1	0	0	0	1	0	1	0	1	X	X	X	32	4A8000h to 4AFFFFh
	SA157	1	0	0	0	1	0	1	1	0	X	X	X	32	4B0000h to 4B7FFFh
	SA158	1	0	0	0	1	0	1	1	1	X	X	X	32	4B8000h to 4BFFFFh
	SA159	1	0	0	0	1	1	0	0	0	X	X	X	32	4C0000h to 4C7FFFh
	SA160	1	0	0	0	1	1	0	0	1	X	X	X	32	4C8000h to 4CFFFFh
	SA161	1	0	0	0	1	1	0	1	0	X	X	X	32	4D0000h to 4D7FFFh
	SA162	1	0	0	0	1	1	0	1	1	X	X	X	32	4D8000h to 4DFFFFh
	SA163	1	0	0	0	1	1	1	0	0	X	X	X	32	4E0000h to 4E7FFFh
	SA164	1	0	0	0	1	1	1	0	1	X	X	X	32	4E8000h to 4EFFFFh
	SA165	1	0	0	0	1	1	1	1	0	X	X	X	32	4F0000h to 4F7FFFh
	SA166	1	0	0	0	1	1	1	1	1	X	X	X	32	4F8000h to 4FFFFFh
	SA167	1	0	0	1	0	0	0	0	0	X	X	X	32	500000h to 507FFFh
	SA168	1	0	0	1	0	0	0	0	1	X	X	X	32	508000h to 50FFFFh
	SA169	1	0	0	1	0	0	0	1	0	X	X	X	32	510000h to 517FFFh
	SA170	1	0	0	1	0	0	0	1	1	X	X	X	32	518000h to 51FFFFh
	SA171	1	0	0	1	0	0	1	0	0	X	X	X	32	520000h to 527FFFh
	SA172	1	0	0	1	0	0	1	0	1	X	X	X	32	528000h to 52FFFFh
	SA173	1	0	0	1	0	0	1	1	0	X	X	X	32	530000h to 537FFFh

(Continued)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kwords)	(× 16) Address Range
				Bank Address											
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA174	1	0	0	1	0	0	1	1	1	X	X	X	32	538000h to 53FFFFh
	SA175	1	0	0	1	0	1	0	0	0	X	X	X	32	540000h to 547FFFh
	SA176	1	0	0	1	0	1	0	0	1	X	X	X	32	548000h to 54FFFFh
	SA177	1	0	0	1	0	1	0	1	0	X	X	X	32	550000h to 557FFFh
	SA178	1	0	0	1	0	1	0	1	1	X	X	X	32	558000h to 55FFFFh
	SA179	1	0	0	1	0	1	1	0	0	X	X	X	32	560000h to 567FFFh
	SA180	1	0	0	1	0	1	1	0	1	X	X	X	32	568000h to 56FFFFh
	SA181	1	0	0	1	0	1	1	1	0	X	X	X	32	570000h to 577FFFh
	SA182	1	0	0	1	0	1	1	1	1	X	X	X	32	578000h to 57FFFFh
	SA183	1	0	0	1	1	0	0	0	0	X	X	X	32	580000h to 587FFFh
	SA184	1	0	0	1	1	0	0	0	1	X	X	X	32	588000h to 58FFFFh
	SA185	1	0	0	1	1	0	0	1	0	X	X	X	32	590000h to 597FFFh
	SA186	1	0	0	1	1	0	0	1	1	X	X	X	32	598000h to 59FFFFh
	SA187	1	0	0	1	1	0	1	0	0	X	X	X	32	5A0000h to 5A7FFFh
	SA188	1	0	0	1	1	0	1	0	1	X	X	X	32	5A8000h to 5AFFFFh
	SA189	1	0	0	1	1	0	1	1	0	X	X	X	32	5B0000h to 5B7FFFh
	SA190	1	0	0	1	1	0	1	1	1	X	X	X	32	5B8000h to 5BFFFFh
	SA191	1	0	0	1	1	1	0	0	0	X	X	X	32	5C0000h to 5C7FFFh
	SA192	1	0	0	1	1	1	0	0	1	X	X	X	32	5C8000h to 5CFFFFh
	SA193	1	0	0	1	1	1	0	1	0	X	X	X	32	6D0000h to 5D7FFFh
	SA194	1	0	0	1	1	1	0	1	1	X	X	X	32	6D8000h to 5DFFFFh
	SA195	1	0	0	1	1	1	1	0	0	X	X	X	32	5E0000h to 5E7FFFh
	SA196	1	0	0	1	1	1	1	0	1	X	X	X	32	5E8000h to 5EFFFFh
	SA197	1	0	0	1	1	1	1	1	0	X	X	X	32	5F0000h to 5F7FFFh
	SA198	1	0	0	1	1	1	1	1	1	X	X	X	32	5F8000h to 5FFFFFh
	SA199	1	0	1	0	0	0	0	0	0	X	X	X	32	600000h to 607FFFh
	SA200	1	0	1	0	0	0	0	0	1	X	X	X	32	608000h to 60FFFFh
	SA201	1	0	1	0	0	0	0	1	0	X	X	X	32	610000h to 617FFFh
	SA202	1	0	1	0	0	0	0	1	1	X	X	X	32	618000h to 61FFFFh
	SA203	1	0	1	0	0	0	1	0	0	X	X	X	32	620000h to 627FFFh
	SA204	1	0	1	0	0	0	1	0	1	X	X	X	32	628000h to 62FFFFh
	SA205	1	0	1	0	0	0	1	1	0	X	X	X	32	630000h to 637FFFh
	SA206	1	0	1	0	0	0	1	1	1	X	X	X	32	638000h to 63FFFFh
	SA207	1	0	1	0	0	1	0	0	0	X	X	X	32	640000h to 647FFFh
	SA208	1	0	1	0	0	1	0	0	1	X	X	X	32	648000h to 64FFFFh
	SA209	1	0	1	0	0	1	0	1	0	X	X	X	32	650000h to 657FFFh
	SA210	1	0	1	0	0	1	0	1	1	X	X	X	32	658000h to 65FFFFh
	SA211	1	0	1	0	0	1	1	0	0	X	X	X	32	660000h to 667FFFh
	SA212	1	0	1	0	0	1	1	0	1	X	X	X	32	668000h to 66FFFFh

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(Continued)

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kwords)	(× 16) Address Range
				Bank Address											
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank C	SA213	1	0	1	0	0	1	1	1	0	X	X	X	32	670000h to 677FFFh
	SA214	1	0	1	0	0	1	1	1	1	X	X	X	32	678000h to 67FFFFh
	SA215	1	0	1	0	1	0	0	0	0	X	X	X	32	680000h to 687FFFh
	SA216	1	0	1	0	1	0	0	0	1	X	X	X	32	688000h to 68FFFFh
	SA217	1	0	1	0	1	0	0	1	0	X	X	X	32	690000h to 697FFFh
	SA218	1	0	1	0	1	0	0	1	1	X	X	X	32	698000h to 69FFFFh
	SA219	1	0	1	0	1	0	1	0	0	X	X	X	32	6A0000h to 6A7FFFh
	SA220	1	0	1	0	1	0	1	0	1	X	X	X	32	6A8000h to 6AFFFFh
	SA221	1	0	1	0	1	0	1	1	0	X	X	X	32	6B0000h to 6B7FFFh
	SA222	1	0	1	0	1	0	1	1	1	X	X	X	32	8B8000h to 6BFFFFh
	SA223	1	0	1	0	1	1	0	0	0	X	X	X	32	6C0000h to 6C7FFFh
	SA224	1	0	1	0	1	1	0	0	1	X	X	X	32	6C8000h to 6CFFFFh
	SA225	1	0	1	0	1	1	0	1	0	X	X	X	32	6D0000h to 6D7FFFh
	SA226	1	0	1	0	1	1	0	1	1	X	X	X	32	6D8000h to 6DFFFFh
	SA227	1	0	1	0	1	1	1	0	0	X	X	X	32	6E0000h to 6E7FFFh
	SA228	1	0	1	0	1	1	1	0	1	X	X	X	32	6E8000h to 6EFFFFh
	SA229	1	0	1	0	1	1	1	1	0	X	X	X	32	6F0000h to 6F7FFFh
	SA230	1	0	1	0	1	1	1	1	1	X	X	X	32	6F8000h to 6FFFFFh

(Continued)

• **Sector Address Tables (Bank D)**

Bank	Sector	Chip Enable		Sector Address										Sector Size (Kwords)	(× 16) Address Range
				Bank Address											
		$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank D	SA231	1	0	1	1	0	0	0	0	0	X	X	X	32	700000h to 707FFFh
	SA232	1	0	1	1	0	0	0	0	1	X	X	X	32	708000h to 70FFFFh
	SA233	1	0	1	1	0	0	0	1	0	X	X	X	32	710000h to 717FFFh
	SA234	1	0	1	1	0	0	0	1	1	X	X	X	32	718000h to 71FFFFh
	SA235	1	0	1	1	0	0	1	0	0	X	X	X	32	720000h to 727FFFh
	SA236	1	0	1	1	0	0	1	0	1	X	X	X	32	728000h to 72FFFFh
	SA237	1	0	1	1	0	0	1	1	0	X	X	X	32	730000h to 737FFFh
	SA238	1	0	1	1	0	0	1	1	1	X	X	X	32	738000h to 73FFFFh
	SA239	1	0	1	1	0	1	0	0	0	X	X	X	32	740000h to 747FFFh
	SA240	1	0	1	1	0	1	0	0	1	X	X	X	32	748000h to 74FFFFh
	SA241	1	0	1	1	0	1	0	1	0	X	X	X	32	750000h to 757FFFh
	SA242	1	0	1	1	0	1	0	1	1	X	X	X	32	758000h to 75FFFFh
	SA243	1	0	1	1	0	1	1	0	0	X	X	X	32	760000h to 767FFFh
	SA244	1	0	1	1	0	1	1	0	1	X	X	X	32	768000h to 76FFFFh
	SA245	1	0	1	1	0	1	1	1	0	X	X	X	32	770000h to 777FFFh
	SA246	1	0	1	1	0	1	1	1	1	X	X	X	32	778000h to 77FFFFh
	SA247	1	0	1	1	1	0	0	0	0	X	X	X	32	780000h to 787FFFh
	SA248	1	0	1	1	1	0	0	0	1	X	X	X	32	788000h to 78FFFFh
	SA249	1	0	1	1	1	0	0	1	0	X	X	X	32	790000h to 797FFFh
	SA250	1	0	1	1	1	0	0	1	1	X	X	X	32	798000h to 79FFFFh
	SA251	1	0	1	1	1	0	1	0	0	X	X	X	32	7A0000h to 7A7FFFh
	SA252	1	0	1	1	1	0	1	0	1	X	X	X	32	7A8000h to 7AFFFFh
	SA253	1	0	1	1	1	0	1	1	0	X	X	X	32	7B0000h to 7B7FFFh
	SA254	1	0	1	1	1	0	1	1	1	X	X	X	32	7B8000h to 7BFFFFh
	SA255	1	0	1	1	1	1	0	0	0	X	X	X	32	7C0000h to 7C7FFFh
	SA256	1	0	1	1	1	1	0	0	1	X	X	X	32	7C8000h to 7CFFFFh
	SA257	1	0	1	1	1	1	0	1	0	X	X	X	32	7D0000h to 7D7FFFh
	SA258	1	0	1	1	1	1	0	1	1	X	X	X	32	7D8000h to 7DFFFFh
	SA259	1	0	1	1	1	1	1	0	0	X	X	X	32	7E0000h to 7E7FFFh
	SA260	1	0	1	1	1	1	1	0	1	X	X	X	32	7E8000h to 7EFFFFh
	SA261	1	0	1	1	1	1	1	1	0	X	X	X	32	7F0000h to 7F7FFFh
	SA262	1	0	1	1	1	1	1	1	1	0	0	0	4	7F8000h to 7F8FFFh
	SA263	1	0	1	1	1	1	1	1	1	0	0	1	4	7F9000h to 7F9FFFh
	SA264	1	0	1	1	1	1	1	1	1	0	1	0	4	7FA000h to 7FAFFFh
	SA265	1	0	1	1	1	1	1	1	1	0	1	1	4	7FB000h to 7FBFFFh
	SA266	1	0	1	1	1	1	1	1	1	1	0	0	4	7FC000h to 7FCFFFh
	SA267	1	0	1	1	1	1	1	1	1	1	0	1	4	7FD000h to 7FDFFFh
	SA268	1	0	1	1	1	1	1	1	1	1	1	0	4	7FE000h to 7FEFFFh
	SA269	1	0	1	1	1	1	1	1	1	1	1	1	4	7FF000h to 7FFFFFh

•Sector Group Address Table

Sector Group	$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	1	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	1	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	1	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	1	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	1	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	1	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	1	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	1	0	0	0	0	0	0	1	X	X	X	SA8
SGA9	0	1	0	0	0	0	0	1	0	X	X	X	SA9
SGA10	0	1	0	0	0	0	0	1	1	X	X	X	SA10
SGA11	0	1	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA12	0	1	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA13	0	1	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA14	0	1	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA15	0	1	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA16	0	1	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA17	0	1	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA18	0	1	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA19	0	1	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA20	0	1	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA21	0	1	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA22	0	1	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA23	0	1	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA24	0	1	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA25	0	1	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA26	0	1	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA27	0	1	1	0	0	0	1	X	X	X	X	X	SA75 to SA78

(Continued)

(Continued)

Sector Group	$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA28	0	1	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA29	0	1	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA30	0	1	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA31	0	1	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA32	0	1	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA33	0	1	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA34	0	1	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA35	0	1	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA36	0	1	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA37	0	1	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA38	0	1	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA39	0	1	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA40	0	1	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA41	0	1	1	1	1	1	1	X	X	X	X	X	SA131 to SA134
SGA42	1	0	0	0	0	0	0	X	X	X	X	X	SA135 to SA138
SGA43	1	0	0	0	0	0	1	X	X	X	X	X	SA139 to SA142
SGA44	1	0	0	0	0	1	0	X	X	X	X	X	SA143 to SA146
SGA45	1	0	0	0	0	1	1	X	X	X	X	X	SA147 to SA150
SGA46	1	0	0	0	1	0	0	X	X	X	X	X	SA151 to SA154
SGA47	1	0	0	0	1	0	1	X	X	X	X	X	SA155 to SA158
SGA48	1	0	0	0	1	1	0	X	X	X	X	X	SA159 to SA162
SGA49	1	0	0	0	1	1	1	X	X	X	X	X	SA163 to SA166
SGA50	1	0	0	1	0	0	0	X	X	X	X	X	SA167 to SA170
SGA51	1	0	0	1	0	0	1	X	X	X	X	X	SA171 to SA174

(Continued)

(Continued)

Sector Group	$\overline{CE0}$	$\overline{CE1}$	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA52	1	0	0	1	0	1	0	X	X	X	X	X	SA175 to SA178
SGA53	1	0	0	1	0	1	1	X	X	X	X	X	SA179 to SA182
SGA54	1	0	0	1	1	0	0	X	X	X	X	X	SA183 to SA186
SGA55	1	0	0	1	1	0	1	X	X	X	X	X	SA187 to SA190
SGA56	1	0	0	1	1	1	0	X	X	X	X	X	SA191 to SA194
SGA57	1	0	0	1	1	1	1	X	X	X	X	X	SA195 to SA198
SGA58	1	0	1	0	0	0	0	X	X	X	X	X	SA199 to SA202
SGA59	1	0	1	0	0	0	1	X	X	X	X	X	SA203 to SA206
SGA60	1	0	1	0	0	1	0	X	X	X	X	X	SA207 to SA210
SGA61	1	0	1	0	0	1	1	X	X	X	X	X	SA211 to SA214
SGA62	1	0	1	0	1	0	0	X	X	X	X	X	SA215 to SA218
SGA63	1	0	1	0	1	0	1	X	X	X	X	X	SA219 to SA222
SGA64	1	0	1	0	1	1	0	X	X	X	X	X	SA223 to SA226
SGA65	1	0	1	0	1	1	1	X	X	X	X	X	SA227 to SA230
SGA66	1	0	1	1	0	0	0	X	X	X	X	X	SA231 to SA234
SGA67	1	0	1	1	0	0	1	X	X	X	X	X	SA235 to SA238
SGA68	1	0	1	1	0	1	0	X	X	X	X	X	SA239 to SA242
SGA69	1	0	1	1	0	1	1	X	X	X	X	X	SA243 to SA246
SGA70	1	0	1	1	1	0	0	X	X	X	X	X	SA247 to SA250
SGA71	1	0	1	1	1	0	1	X	X	X	X	X	SA251 to SA254
SGA72	1	0	1	1	1	1	0	X	X	X	X	X	SA255 to SA258
SGA73	1	0	1	1	1	1	1	0	0	X	X	X	SA259
SGA74	1	0	1	1	1	1	1	0	1	X	X	X	SA260
SGA75	1	0	1	1	1	1	1	1	0	X	X	X	SA261
SGA76	1	0	1	1	1	1	1	1	1	0	0	0	SA262
SGA77	1	0	1	1	1	1	1	1	1	0	0	1	SA263
SGA78	1	0	1	1	1	1	1	1	1	0	1	0	SA264
SGA79	1	0	1	1	1	1	1	1	1	0	1	1	SA265
SGA80	1	0	1	1	1	1	1	1	1	1	0	0	SA266
SGA81	1	0	1	1	1	1	1	1	1	1	0	1	SA267
SGA82	1	0	1	1	1	1	1	1	1	1	1	0	SA268
SGA83	1	0	1	1	1	1	1	1	1	1	1	1	SA269

•Sector Group Protection Verify Autoselect Codes

Type	A_{22} to A_{12}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA	L	L	X	X	L	L	L	L	04h
Device Code	BA	L	L	X	X	L	L	L	H	227Eh
Extended Device Code*2	BA	L	L	X	X	H	H	H	L	2221h
		L	L	X	X	H	H	H	H	2200h
Sector Group Protection	Sector Group Addresses	L	L	L	L	L	L	H	L	01h*1

Legand: L = V_{IL}, H = V_{IH}, X= V_{IL} or V_{IH} .

*1 : Sector Group can be protected by "Sector Group Protection", "Extended Sector Group Protection", and "New Sector Protection(PPB Protection). Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh is output, it indicates that two additional codes, called Extended Device Codes, will be required. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

- **Command Definitions**

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle		Seventh Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h	RA	RD	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	—	—
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h	—	—
Program/Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—	—	—
Program/Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—	—	—
Fast Program	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	4	XXXh	60h	SGA+ WPH	60h	SGA+ WPH	40h	SGA+W PH	SD	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—	—	—
Password Program	4	555h	AAh	2AAh	55h	555h	38h	XX0h	PD0	—	—	—	—	—	—
		555h	AAh	2AAh	55h	555h	38h	XX1h	PD1						
		555h	AAh	2AAh	55h	555h	38h	XX2h	PD2						
		555h	AAh	2AAh	55h	555h	38h	XX3h	PD3						
Password Unlock	7	555h	AAh	2AAh	55h	555h	28h	XX0h	PD0	XX1h	PD1	XX2h	PD2	XX3h	PD3
Password Verify	4	555h	AAh	2AAh	55h	555h	C8h	PWA	PWD	—	—	—	—	—	—
Password Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	PL	68h	PL	48h	XXXh	RD(0)	—	—
Persistent Protection Mode Locking Bit Program	6	555h	AAh	2AAh	55h	555h	60h	SPML	68h	SPML	48h	XXXh	RD(0)	—	—
PPB Program	6	555h	AAh	2AAh	55h	555h	60h	SGA+WP	68h	SGA+WP	48h	XXXh	RD(0)	—	—
PPB Verify	4	555h	AAh	2AAh	55h	(BA) 555h	90h	SGA+WP	RD(0)	—	—	—	—	—	—
All PPB Erase	4	555h	AAh	2AAh	55h	555h	60h	WP	60h	SGA+WP	40h	XXXh	RD(0)	—	—
PPB Lock Bit Set	3	555h	AAh	2AAh	55h	555h	78h	—	—	—	—	—	—	—	—
PPB Lock Bit Verify	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD(1)	—	—	—	—	—	—
DPB Write	4	555h	AAh	2AAh	55h	555h	48h	SA	X1h	—	—	—	—	—	—
DPB Erase	4	555h	AAh	2AAh	55h	555h	48h	SA	X0h	—	—	—	—	—	—
DPB Verify	4	555h	AAh	2AAh	55h	(BA) 555h	58h	SA	RD(0)	—	—	—	—	—	—

Legend:

RA = Address of the memory location to be read

PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{22}, A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12} will uniquely select any sector.

BA = Bank Address. Address setted by A_{22}, A_{21}, A_{20}, A_{19} will select Bank A, Bank B, Bank C and Bank D.

RD = Data read from location RA during read operation.

PD = Data to be programmed at location PA. Data is latched on the rising edge of write pulse.

SGA = Sector group address to be protected.

WPH = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 0, 0, 0, 1, 0)

SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

HRA = Address of the Hi-ROM area Word Mode : 000000h to 00007Fh

HRBA = Bank Address of the Hi-ROM area (A_{22} = A_{21} = A_{20} = V_{IL})

RD (0) = Read Data bit. If programmed, DQ_0 = 1, if erase, DQ_0 = 0

RD (1) = Read Data bit. If programmed, DQ_1 = 1, if erase, DQ_1 = 0

OPBP = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 1, 1, 0, 1, 0)

PWA/PWD = Password Address/Password Data

PL =(A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 0, 1, 0, 1, 0)

SPML = (A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 1, 0, 0, 1, 0)

WP =(A_7, A_6, A_5, A_4, A_3, A_2, A_1, A_0) is (0, 0, 0, 0, 0, 0, 1, 0)

*1: This command is valid during Fast Mode.

*2: This command is valid while $\overline{\text{RESET}}$ = V_{ID}.

*3: This command is valid during Hi-ROM mode.

*4: The data “00h” is also acceptable.

Notes : 1. Address bits A_{22} to A_{11} = X = “H” or “L” for all address commands except for PA, SA, BA, SGA, OPBP, PWA, PL, SPML, WP, WPH.
2. Bus operations are defined in this document.
3. The system should generate the following address patterns:
Word Mode : 555h or 2AAh to addresses A_{10} to A_0
4. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

■ ELECTRICAL CHARACTERISTICS (AC Characteristics)

- **Read Only Operations Characteristics (Flash)**

Parameter Symbols		Description	Test Setup		Value (Note1)	Unit
JEDEC	Standard					
t_{AVAV}	t_{RC}	Read Cycle Time	—	Min.	70	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	70	ns
—	t_{PRC}	Page Read Cycle Time	—	Min.	25	ns
—	t_{PACC}	Page Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	Max.	25	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max.	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	Max.	25	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output HIGH-Z	—	Max.	25	ns
t_{GHQZ}	t_{DF}	Output Enable to Output HIGH-Z	—	Max.	25	ns
t_{AXQX}	t_{OH}	Output Hold Time From Address, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	—	Min.	5	ns

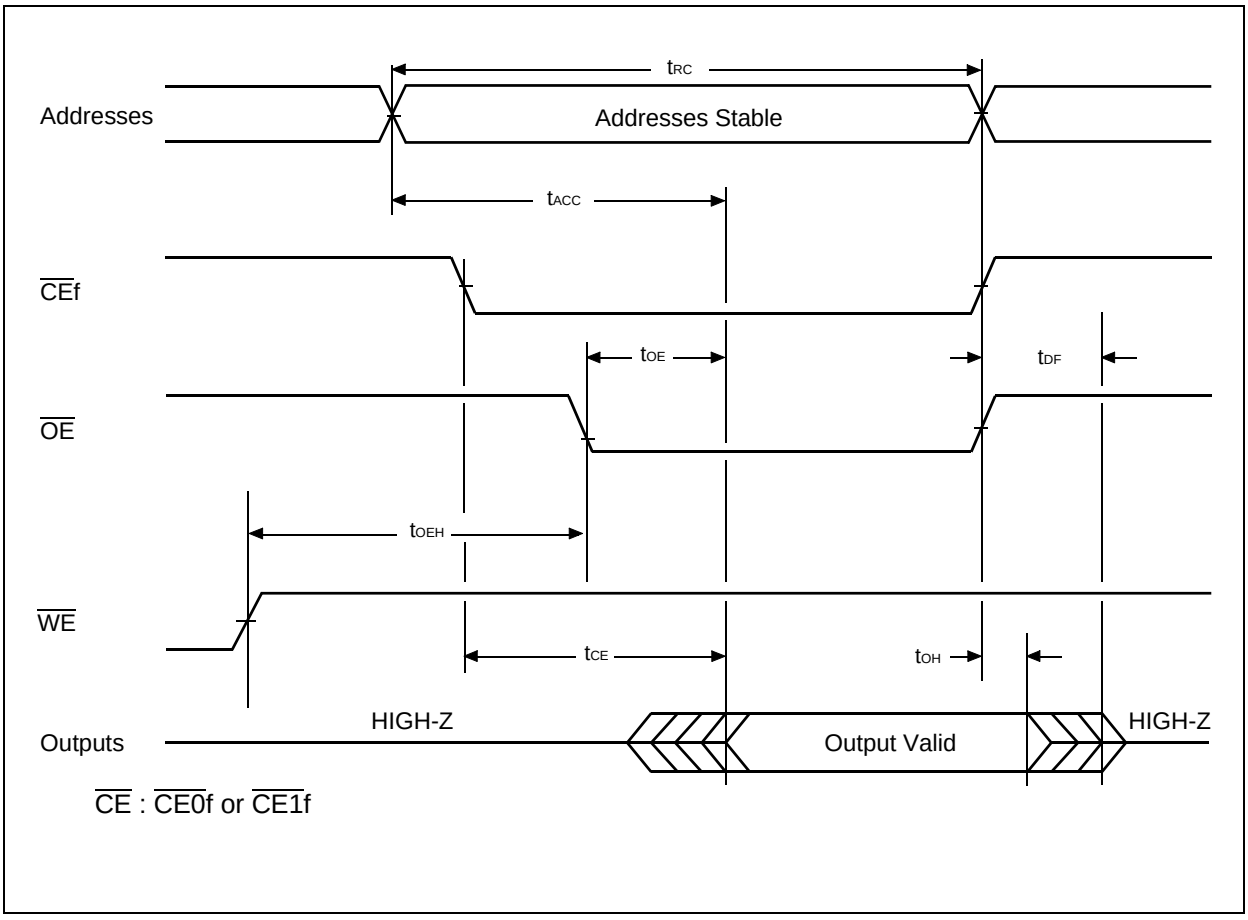
Note: Test Conditions– Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to $V_{CC}f$
Timing measurement reference level
Input: $0.5 \times V_{CC}f$
Output: $0.5 \times V_{CC}f$

- **Write/Erase/Program Operations (Flash)**

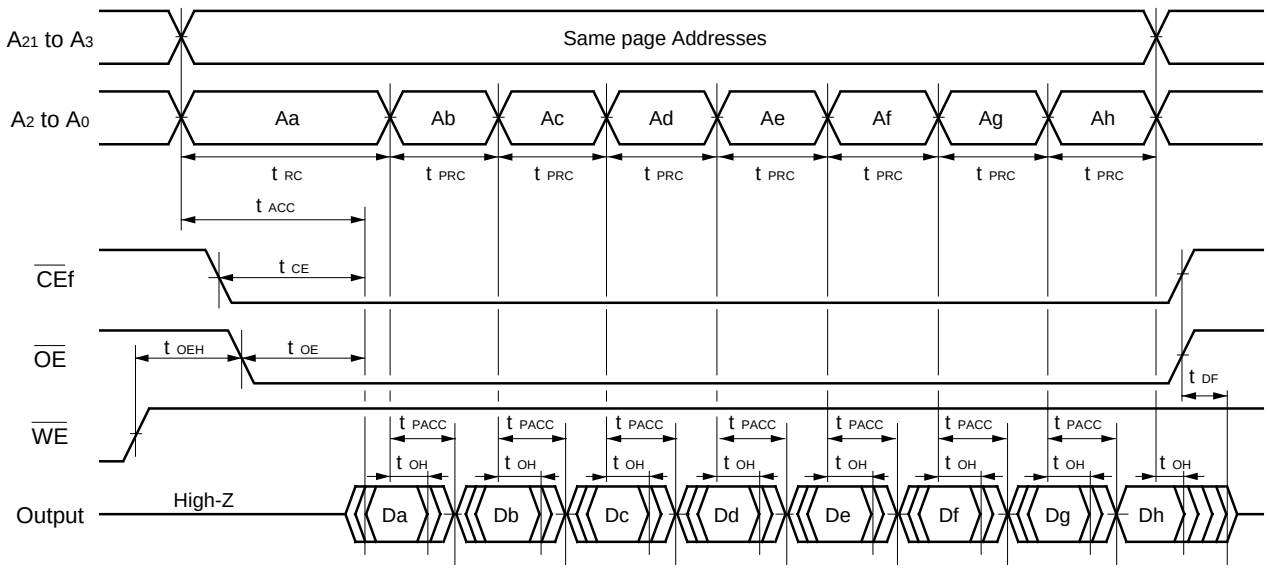
Parameter Symbols		Description			Value (Note1)	Unit
JEDEC	Standard					
t_{AVAV}	t_{WC}	Write Cycle Time		Min.	70	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min.	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min.	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min.	35	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min.	0	ns
—	t_{OEH}	Output Enable Hold Time	Read	Min.	0	ns
			Toggle and $\overline{\text{Data}}$ Polling	Min.	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min.	0	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ High to $\overline{CE}$f Low)		Min.	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$f Setup Time		Min.	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min.	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$f Hold Time		Min.	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min.	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min.	35	ns
t_{ELEH}	t_{CP}	$\overline{CE}$f Pulse Width		Min.	35	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min.	30	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$f Pulse Width High		Min.	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Typ.	6	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation *1		Typ.	0.5	s
—	t_{VCS}	V_{CC}f Setup Time		Min.	50	µs
—	t_{VIDR}	Rise Time to V_{ID} *2		Min.	500	ns
—	t_{VACCR}	Rise Time to V_{ACC} *3		Min.	500	ns
—	t_{VLHT}	Voltage Transition Time *2		Min.	4	µs
—	t_{RB}	Recover Time from RY/$\overline{BY}$		Min.	0	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		Min.	500	ns
—	t_{RH}	$\overline{RESET}$ High Level Period Before Read		Min.	50	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		Max.	90	ns
—	t_{EOE}	Delay Time from Embedded Output Enable		Max.	70	ns
—	t_{TOW}	Erase Time-out Time		Min.	50	µs
—	t_{SPD}	Erase Suspend Transition Time		Max.	20	µs

Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Group Protection / Unprotection .
3. This timing is for Accelerated Program operation.

- **Read Operation Timing Diagram**

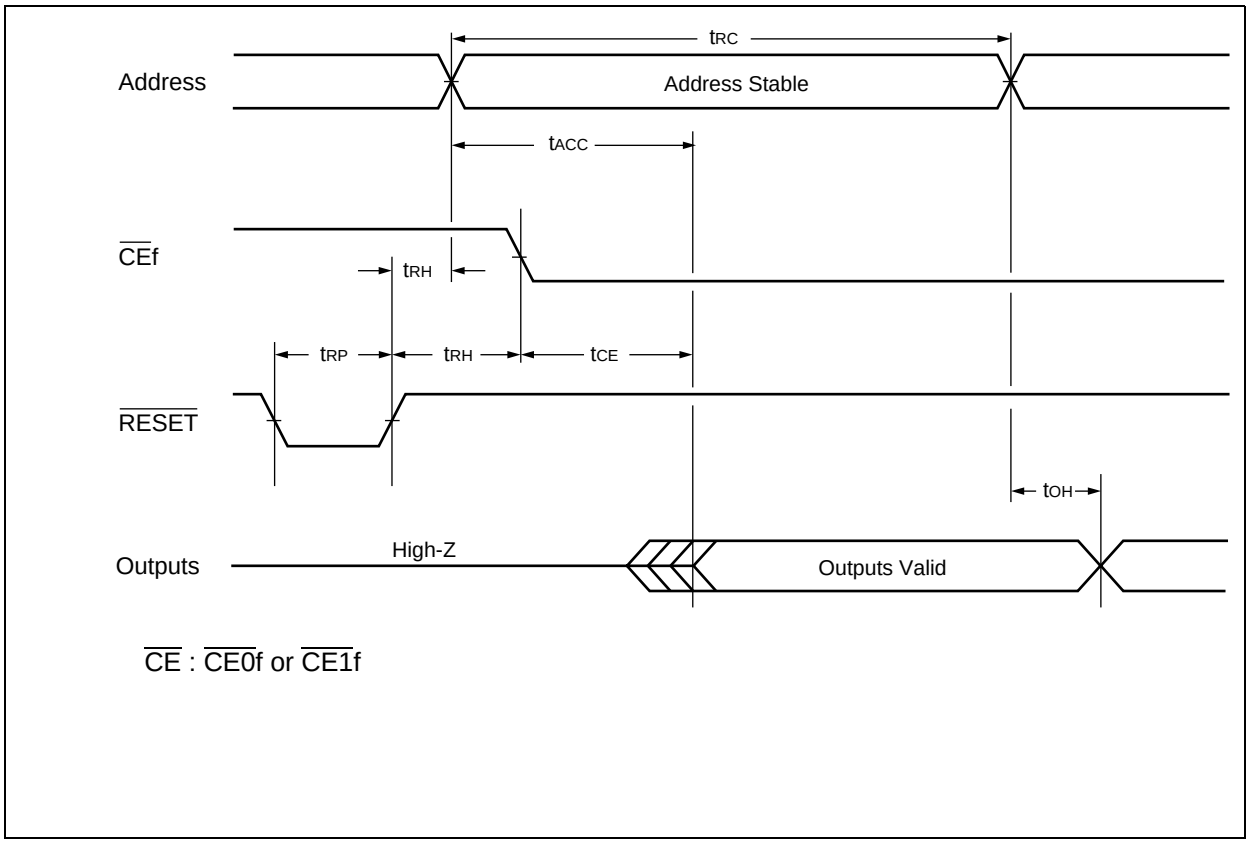


- **Page Read Operation Timing Diagram**

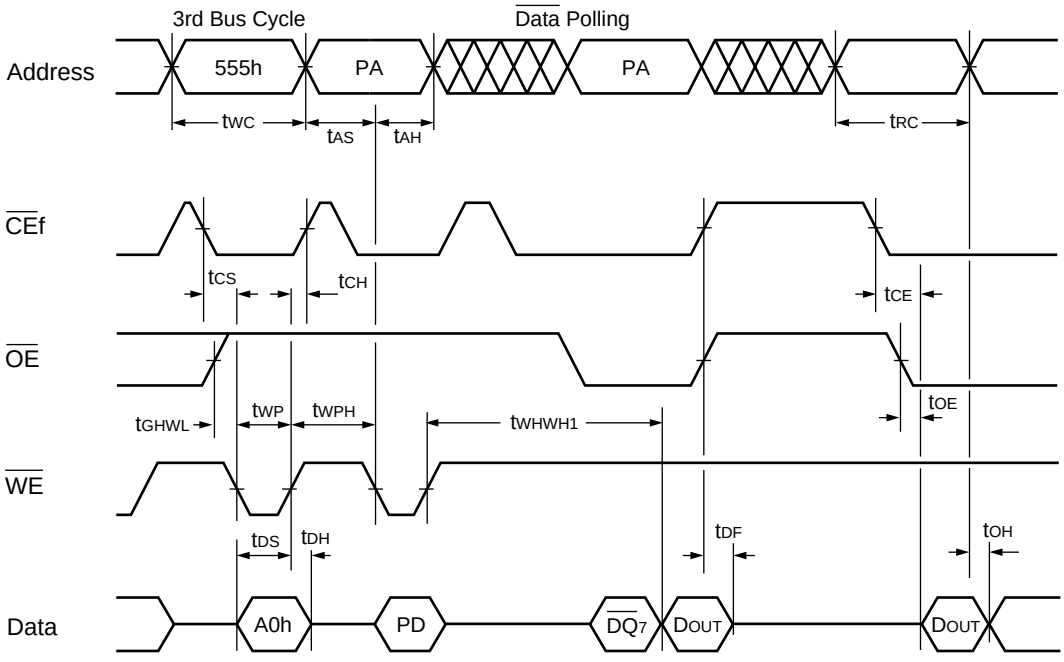


$\overline{CE}$: $\overline{CE0f}$ or $\overline{CE1f}$

- **Hardware Reset/Read Operation Timing Diagram**



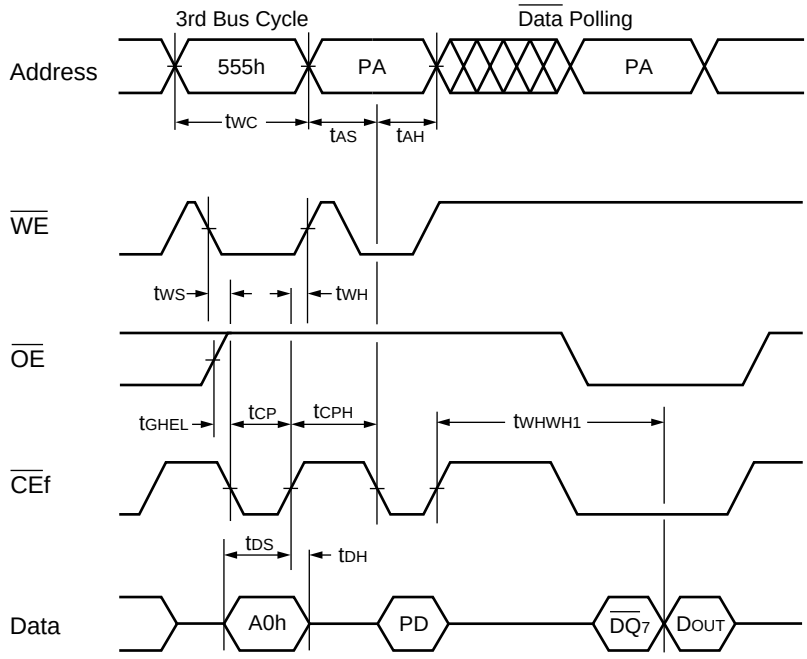
- **Alternate $\overline{WE}$ Controlled Program Operation Timing Diagram**



$\overline{CE}$: $\overline{CE0}$f or $\overline{CE1}$f

Notes : 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at word address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

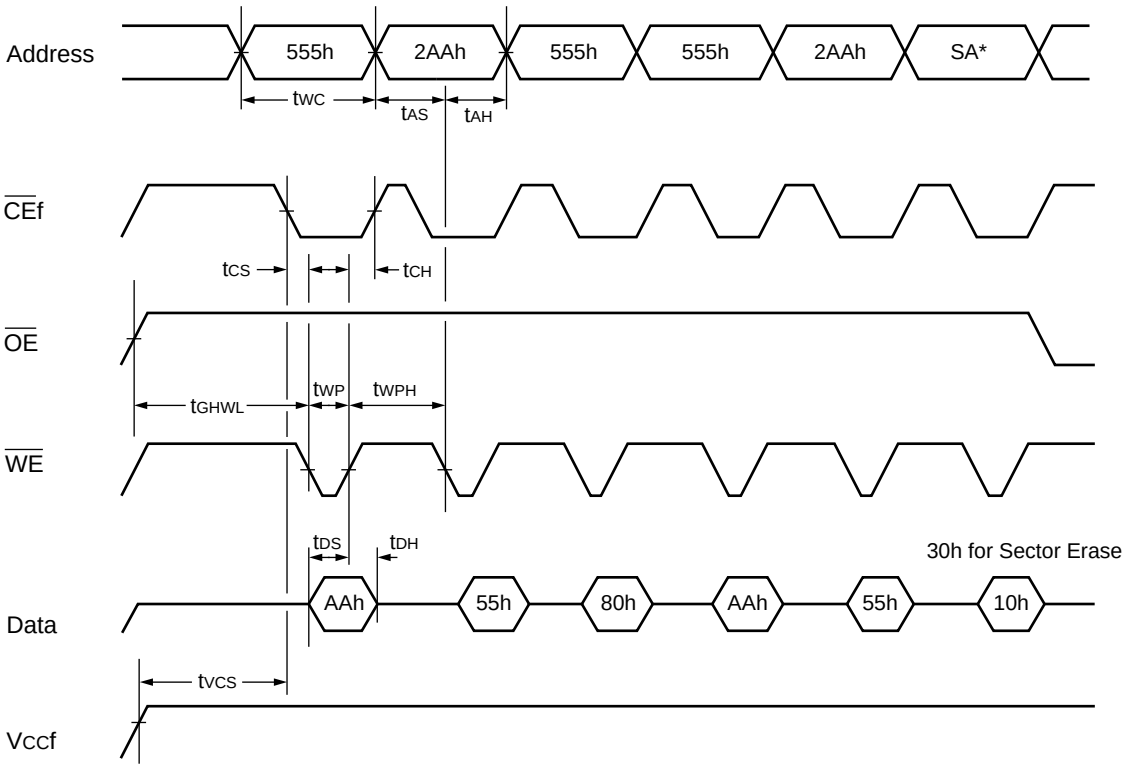
- **Alternate $\overline{CE}$ Controlled Program Operation Timing Diagram**



$\overline{CE}$: $\overline{CE0f}$ or $\overline{CE1f}$

Notes : 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at word address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

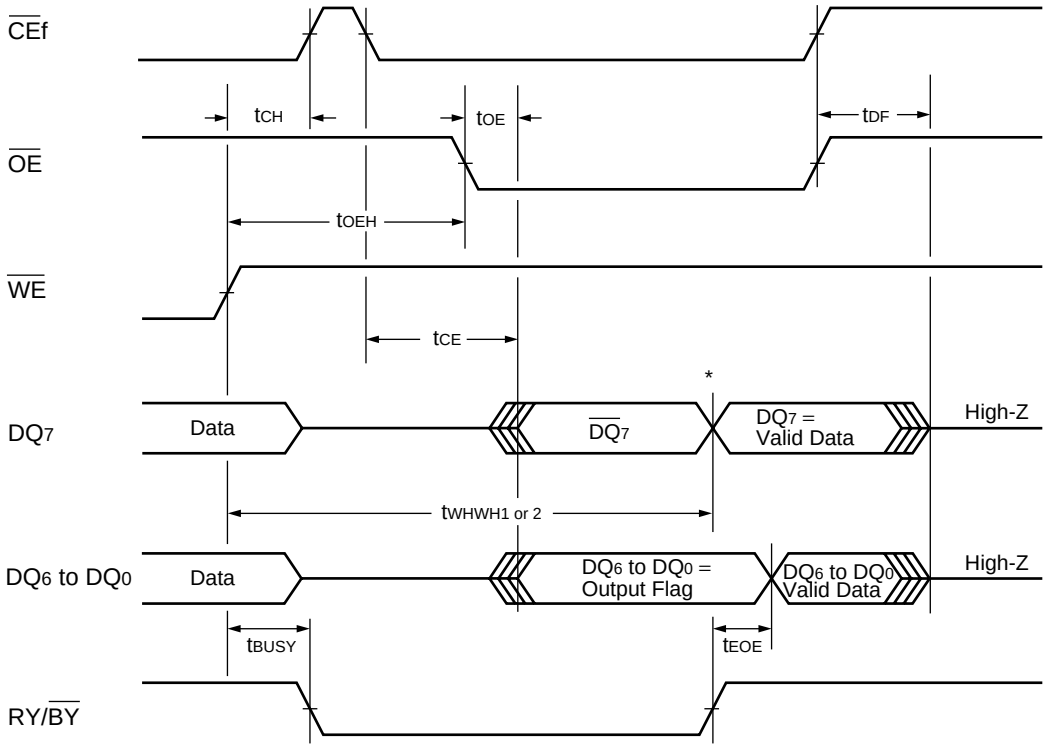
- **Chip/Sector Erase Operation Timing Diagram**



$\overline{CE}$: $\overline{CE0}$f or $\overline{CE1}$f

* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

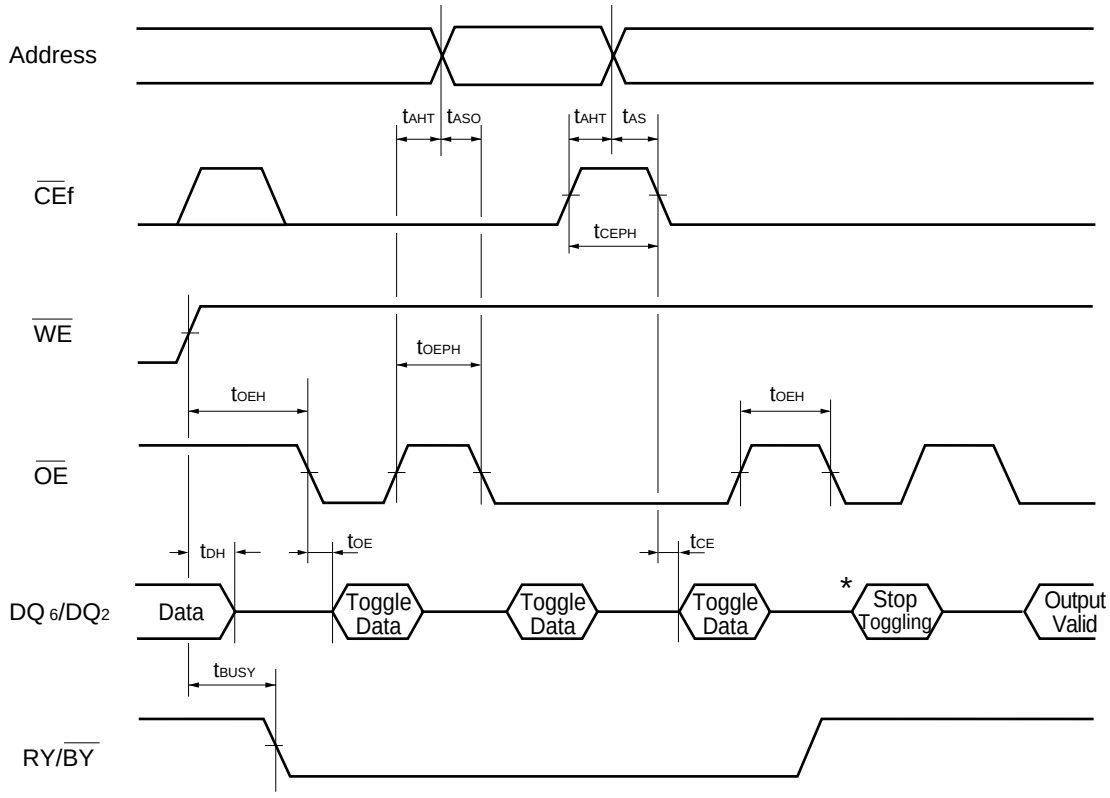
- **$\overline{\text{Data}}$ Polling during Embedded Algorithm Operation Timing Diagram**



$\overline{\text{CE}}$: $\overline{\text{CE0}}$f or $\overline{\text{CE1}}$f

* : DQ_7 = Valid Data (The device has completed the Embedded operation) .

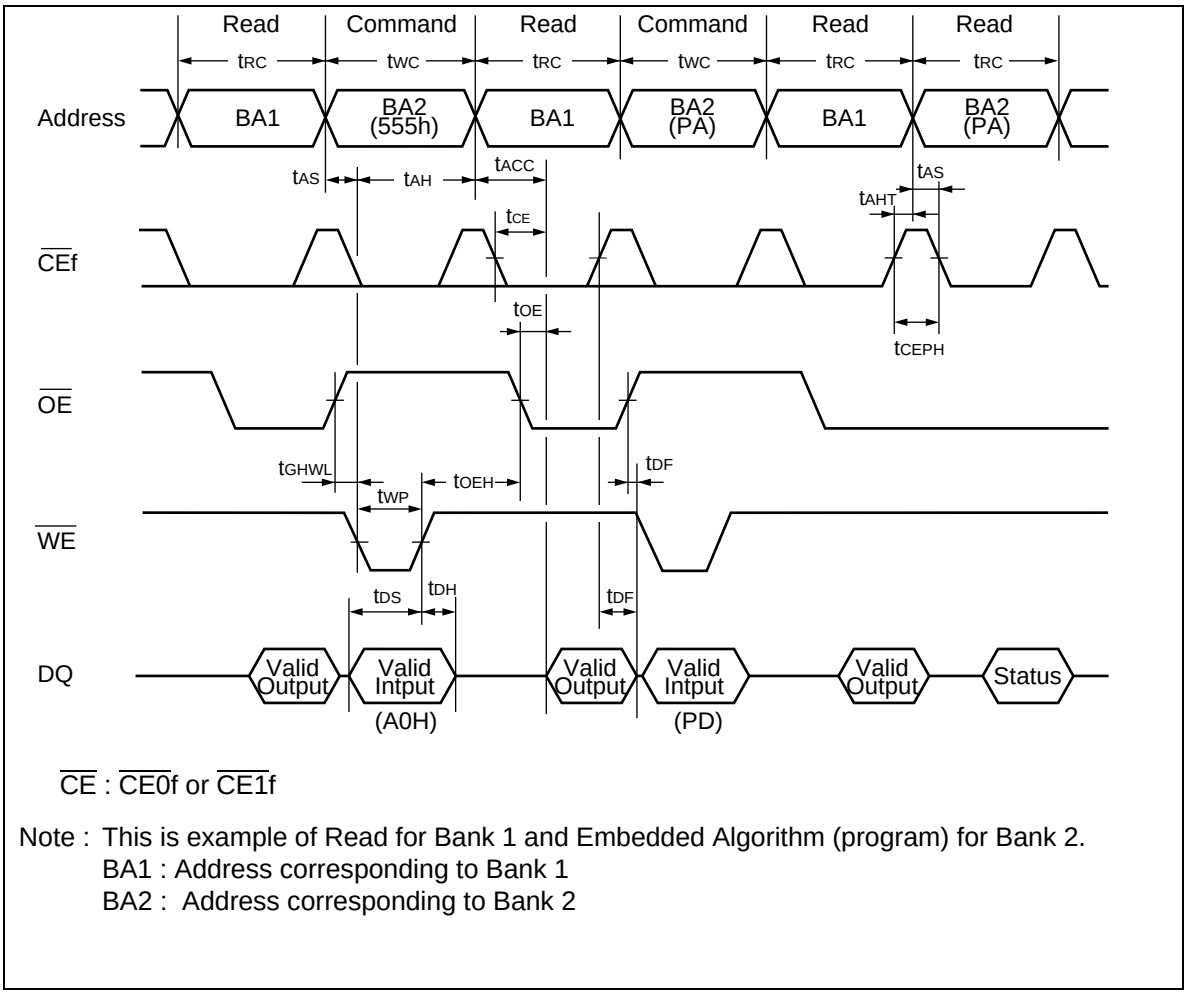
- **AC Waveforms for Toggle Bit I during Embedded Algorithm Operations**



CE : CE0f or CE1f

* : DQ_6 stops toggling (The device has completed the Embedded operation).

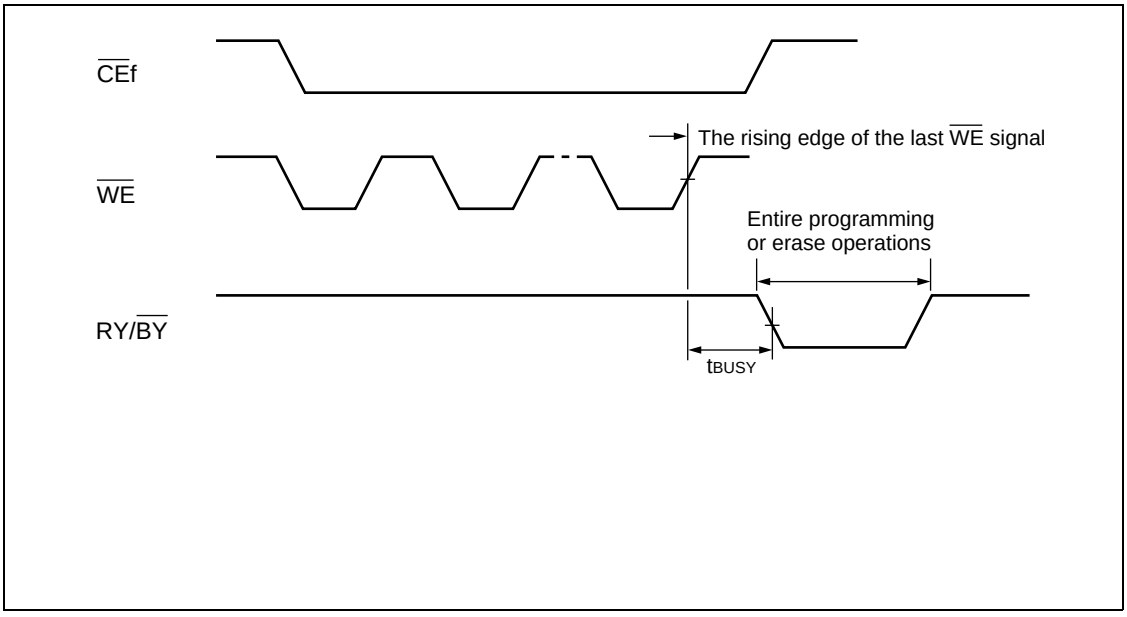
- **Bank-to-Bank Read/Write Timing Diagram**



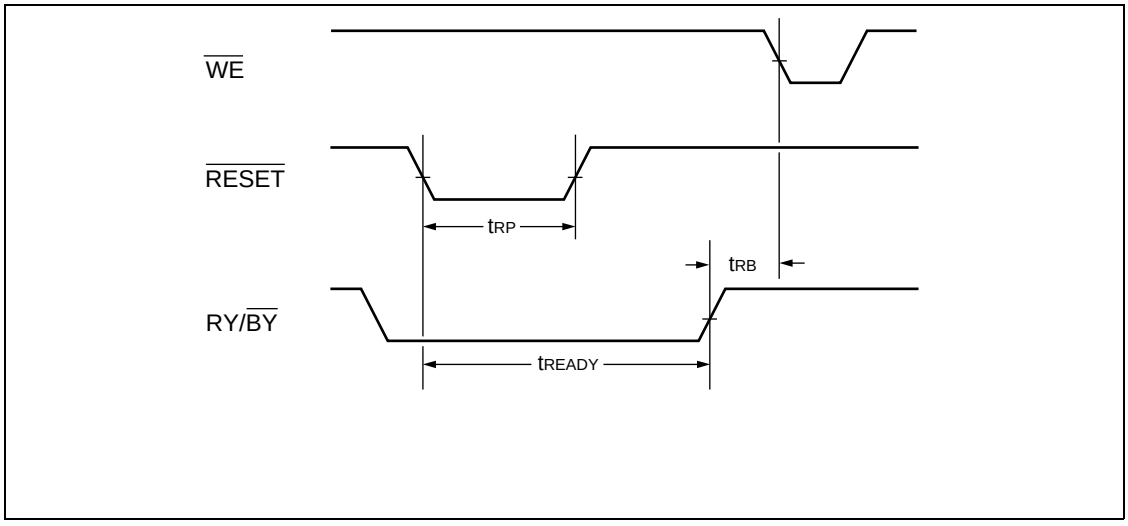
$\overline{CE}$: $\overline{CE0}$f or $\overline{CE1}$f

Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1 : Address corresponding to Bank 1
BA2 : Address corresponding to Bank 2

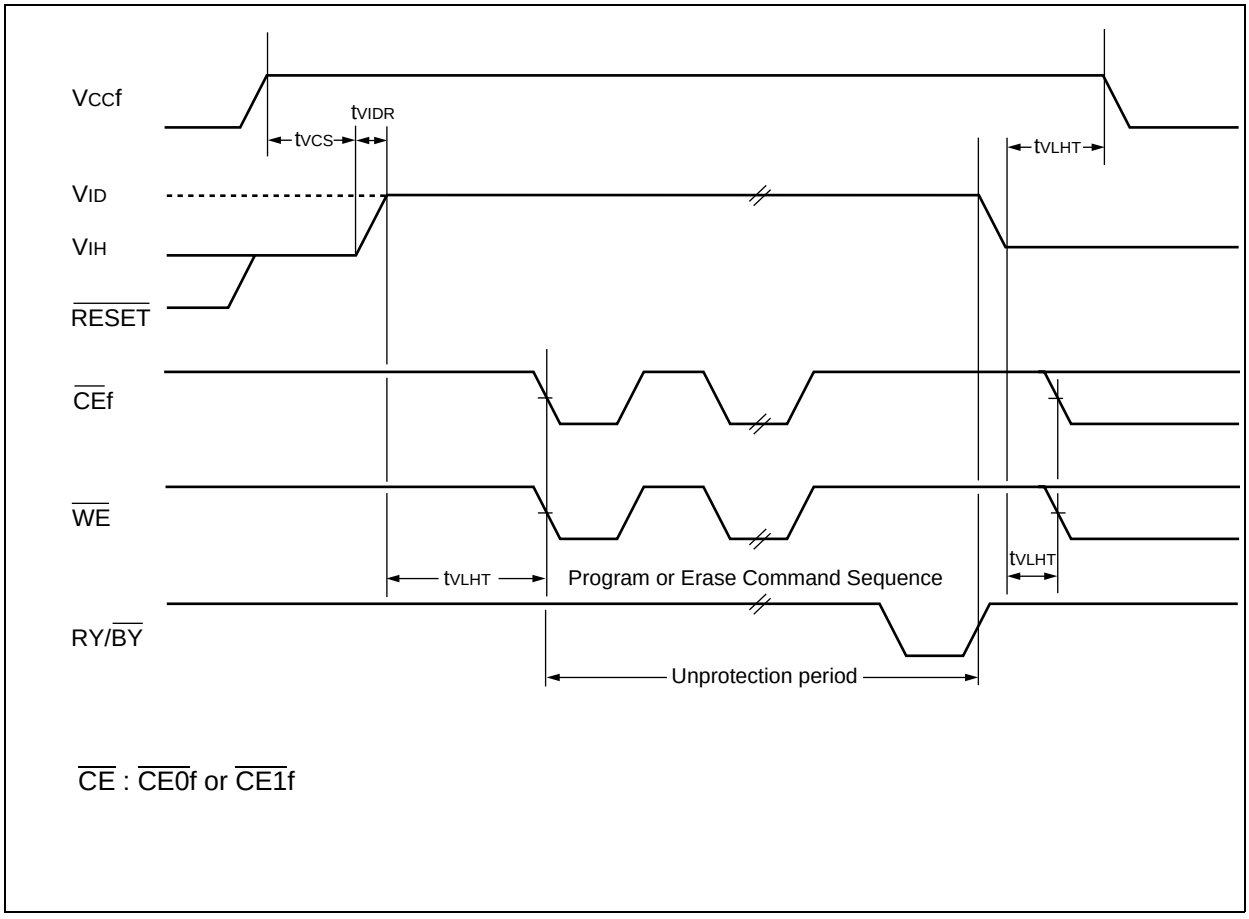
- **RY/$\overline{BY}$ Timing Diagram during Program/Erase Operation Timing Diagram**



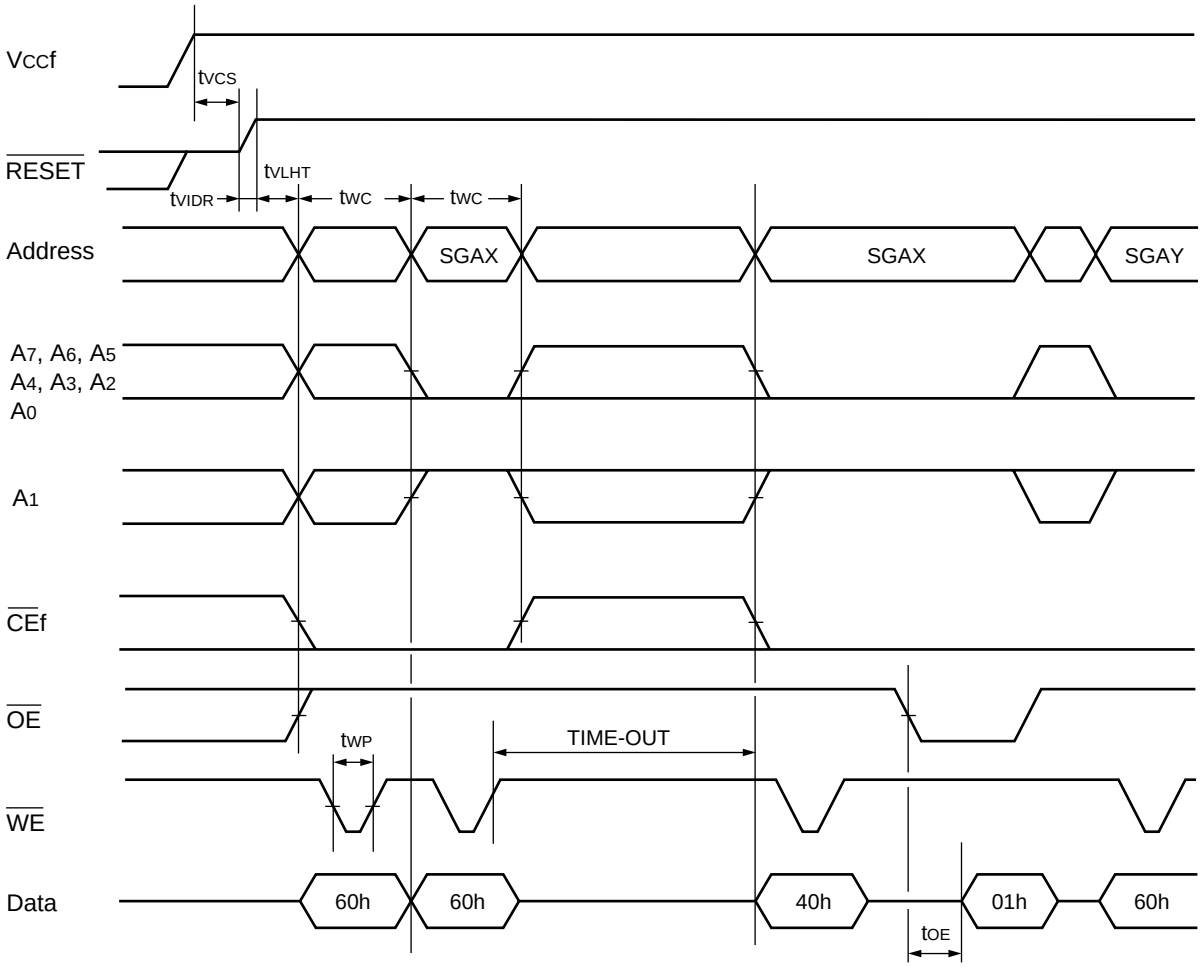
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram**



- **Temporary Sector Group Unprotection Timing Diagram**



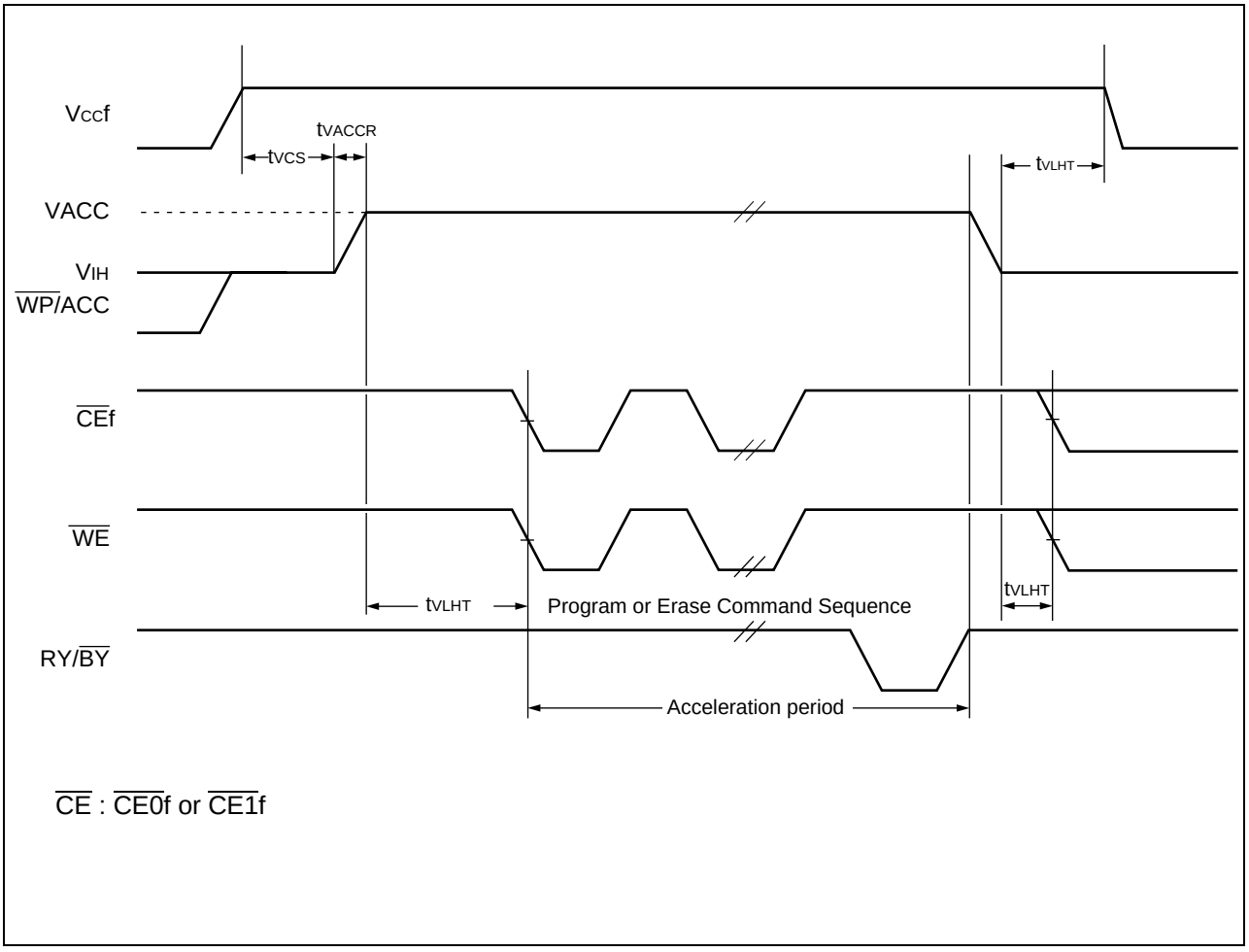
- **Extended Sector Group Protection Timing Diagram**



$\overline{CE}$: $\overline{CE0f}$ or $\overline{CE1f}$

SGAX : Sector Group Address to be protected
SGAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min.)

- **Accelerated Program Timing Diagram**



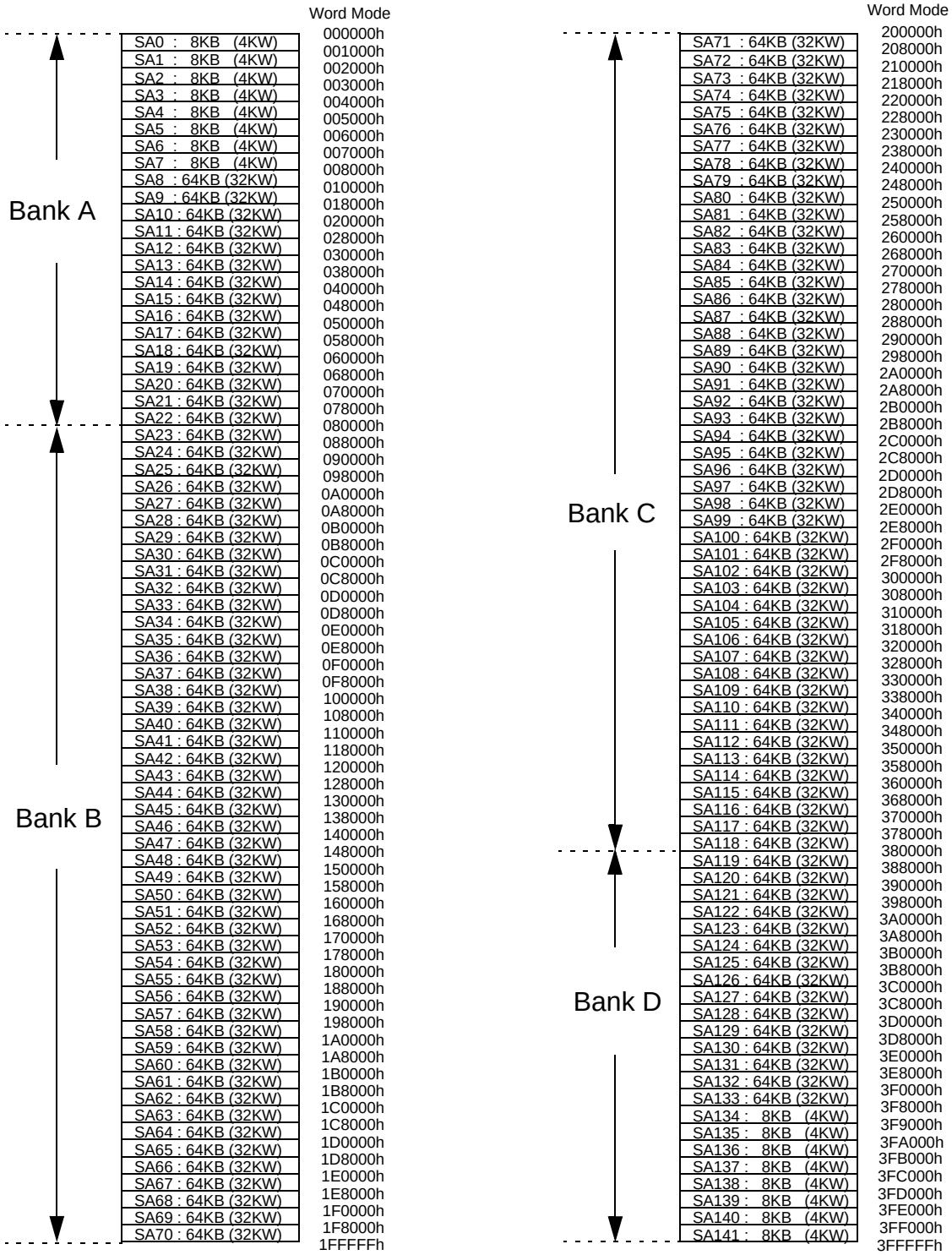
■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Sector Erase Time	—	0.5	2	s	Excludes programming time prior to erasure
Word Programming Time	—	6.0	100	µs	Excludes system-level overhead
Chip Programming Time	—	50.3	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	—

Note: Typical Erase conditions T_A = 25°C, V_{CC} = 2.9 V
Typical Program conditions T_A = 25°C, V_{CC} = 2.9 V, Data = checker

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Sixteen 4K words, and one hundred twenty-six 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



Sector Architecture

Table 1 FlexBank™ Architecture

Bank Splits	Bank 1		Bank 2	
	Volume	Combination	Volume	Combination
1	8 Mbit	Bank A	56 Mbit	Remainder (Bank B, C, D)
2	24 Mbit	Bank B	40 Mbit	Remainder (Bank A, C, D)
3	24 Mbit	Bank C	40 Mbit	Remainder (Bank A, B, D)
4	8 Mbit	Bank D	56 Mbit	Remainder (Bank A, B, C)

Table 2 Example of Virtual Banks Combination

Bank Splits	Bank 1			Bank 2		
	Volume	Combination	Sector Size	Volume	Combination	Sector Size
1	8 Mbit	Bank A	8 × 8 Kbyte/4 Kword + 15 × 64 Kbyte/32 Kword	56 Mbit	Bank B + Bank C + Bank D	8 × 8 Kbyte/4 Kword + 111 × 64 Kbyte/32 Kword
2	16 Mbit	Bank A + Bank D	16 × 8 Kbyte/4 Kword + 30 × 64 Kbyte/32 Kword	48 Mbit	Bank B + Bank C	96 × 64 Kbyte/32 Kword
3	24 Mbit	Bank B	48 × 64 Kbyte/32 Kword	40 Mbit	Bank A + Bank C + Bank D	16 × 8 Kbyte/4 Kword + 78 × 64 Kbyte/32 Kword
4	32 Mbit	Bank A + Bank B	8 × 8 Kbyte/4 Kword + 63 × 64 Kbyte/32 Kword	32 Mbit	Bank C + Bank D	8 × 8 Kbyte/4 Kword + 63 × 64 Kbyte/32 Kword

Note : When multiple sector erase over several banks is operated, the system cannot read out of the bank to which a sector being erased belongs. For example, suppose that erasing is taking place at both Bank A and Bank B, neither Bank A nor Bank B is read out (they would output the sequence flag once they were selected.) Meanwhile the system would get to read from either Bank C or Bank D.

Table 3 Simultaneous Operation

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

* : By writing erase suspend command on the bank address of sector being erased, the erase operation gets suspended so that it enables reading from or programming the remaining sectors.

Note: Bank 1 and Bank 2 are divided for the sake of convenience at Simultaneous Operation. Actually, the Bank consists of 4 banks, Bank A, Bank B, BankC and Bank D. Bank Address (BA) meant to specify each of the Banks.

Table 4 Sector Address Tables

Bank	Sector	Sector Address										Address Range
		Bank Address										Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank A	SA0	0	0	0	0	0	0	0	0	0	0	000000h to 000FFFh
	SA1	0	0	0	0	0	0	0	0	0	1	001000h to 001FFFh
	SA2	0	0	0	0	0	0	0	0	1	0	002000h to 002FFFh
	SA3	0	0	0	0	0	0	0	0	1	1	003000h to 003FFFh
	SA4	0	0	0	0	0	0	0	1	0	0	004000h to 004FFFh
	SA5	0	0	0	0	0	0	0	1	0	1	005000h to 005FFFh
	SA6	0	0	0	0	0	0	0	1	1	0	006000h to 006FFFh
	SA7	0	0	0	0	0	0	0	1	1	1	007000h to 007FFFh
	SA8	0	0	0	0	0	0	1	X	X	X	008000h to 00FFFFh
	SA9	0	0	0	0	0	1	0	X	X	X	010000h to 017FFFh
	SA10	0	0	0	0	0	1	1	X	X	X	018000h to 01FFFFh
	SA11	0	0	0	0	1	0	0	X	X	X	020000h to 027FFFh
	SA12	0	0	0	0	1	0	1	X	X	X	028000h to 02FFFFh
	SA13	0	0	0	0	1	1	0	X	X	X	030000h to 037FFFh
	SA14	0	0	0	0	1	1	1	X	X	X	038000h to 03FFFFh
	SA15	0	0	0	1	0	0	0	X	X	X	040000h to 047FFFh
	SA16	0	0	0	1	0	0	1	X	X	X	048000h to 04FFFFh
	SA17	0	0	0	1	0	1	0	X	X	X	050000h to 057FFFh
	SA18	0	0	0	1	0	1	1	X	X	X	058000h to 05FFFFh
	SA19	0	0	0	1	1	0	0	X	X	X	060000h to 067FFFh
	SA20	0	0	0	1	1	0	1	X	X	X	068000h to 06FFFFh
	SA21	0	0	0	1	1	1	0	X	X	X	070000h to 077FFFh
	SA22	0	0	0	1	1	1	1	X	X	X	078000h to 07FFFFh

(Continued)

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Bank	Sector	Sector Address										Address Range
		Bank Address										Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank B	SA23	0	0	1	0	0	0	0	X	X	X	080000h to 087FFFh
	SA24	0	0	1	0	0	0	1	X	X	X	088000h to 08FFFFh
	SA25	0	0	1	0	0	1	0	X	X	X	090000h to 097FFFh
	SA26	0	0	1	0	0	1	1	X	X	X	098000h to 09FFFFh
	SA27	0	0	1	0	1	0	0	X	X	X	0A0000h to 0A7FFFh
	SA28	0	0	1	0	1	0	1	X	X	X	0A8000h to 0AFFFFh
	SA29	0	0	1	0	1	1	0	X	X	X	0B0000h to 0B7FFFh
	SA30	0	0	1	0	1	1	1	X	X	X	0B8000h to 0BFFFFh
	SA31	0	0	1	1	0	0	0	X	X	X	0C0000h to 0C7FFFh
	SA32	0	0	1	1	0	0	1	X	X	X	0C8000h to 0CFFFFh
	SA33	0	0	1	1	0	1	0	X	X	X	0D0000h to 0D7FFFh
	SA34	0	0	1	1	0	1	1	X	X	X	0D8000h to 0DFFFFh
	SA35	0	0	1	1	1	0	0	X	X	X	0E0000h to 0E7FFFh
	SA36	0	0	1	1	1	0	1	X	X	X	0E8000h to 0EFFFFh
	SA37	0	0	1	1	1	1	0	X	X	X	0F0000h to 0F7FFFh
	SA38	0	0	1	1	1	1	1	X	X	X	0F8000h to 0FFFFFh
	SA39	0	1	0	0	0	0	0	X	X	X	100000h to 107FFFh
	SA40	0	1	0	0	0	0	1	X	X	X	108000h to 10FFFFh
	SA41	0	1	0	0	0	1	0	X	X	X	110000h to 117FFFh
	SA42	0	1	0	0	0	1	1	X	X	X	118000h to 11FFFFh
	SA43	0	1	0	0	1	0	0	X	X	X	120000h to 127FFFh
	SA44	0	1	0	0	1	0	1	X	X	X	128000h to 12FFFFh
	SA45	0	1	0	0	1	1	0	X	X	X	130000h to 137FFFh
	SA46	0	1	0	0	1	1	1	X	X	X	138000h to 13FFFFh
	SA47	0	1	0	1	0	0	0	X	X	X	140000h to 147FFFh
	SA48	0	1	0	1	0	0	1	X	X	X	148000h to 14FFFFh
	SA49	0	1	0	1	0	1	0	X	X	X	150000h to 157FFFh
	SA50	0	1	0	1	0	1	1	X	X	X	158000h to 15FFFFh
	SA51	0	1	0	1	1	0	0	X	X	X	160000h to 167FFFh
	SA52	0	1	0	1	1	0	1	X	X	X	168000h to 16FFFFh
	SA53	0	1	0	1	1	1	0	X	X	X	170000h to 177FFFh
	SA54	0	1	0	1	1	1	1	X	X	X	178000h to 17FFFFh
	SA55	0	1	1	0	0	0	0	X	X	X	180000h to 187FFFh
	SA56	0	1	1	0	0	0	1	X	X	X	188000h to 18FFFFh
	SA57	0	1	1	0	0	1	0	X	X	X	190000h to 197FFFh
	SA58	0	1	1	0	0	1	1	X	X	X	198000h to 19FFFFh
	SA59	0	1	1	0	1	0	0	X	X	X	1A0000h to 1A7FFFh
	SA60	0	1	1	0	1	0	1	X	X	X	1A8000h to 1AFFFFh
	SA61	0	1	1	0	1	1	0	X	X	X	1B0000h to 1B7FFFh
	SA62	0	1	1	0	1	1	1	X	X	X	1B8000h to 1BFFFFh
	SA63	0	1	1	1	0	0	0	X	X	X	1C0000h to 1C7FFFh
	SA64	0	1	1	1	0	0	1	X	X	X	1C8000h to 1CFFFFh
	SA65	0	1	1	1	0	1	0	X	X	X	1D0000h to 1D7FFFh
	SA66	0	1	1	1	0	1	1	X	X	X	1D8000h to 1DFFFFh
	SA67	0	1	1	1	1	0	0	X	X	X	1E0000h to 1E7FFFh
	SA68	0	1	1	1	1	0	1	X	X	X	1E8000h to 1EFFFFh
	SA69	0	1	1	1	1	1	0	X	X	X	1F0000h to 1F7FFFh
	SA70	0	1	1	1	1	1	1	X	X	X	1F8000h to 1FFFFFh

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Bank	Sector	Sector Address										Address Range
		Bank Address										Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank C	SA71	1	0	0	0	0	0	0	X	X	X	200000h to 207FFFh
	SA72	1	0	0	0	0	0	1	X	X	X	208000h to 20FFFFh
	SA73	1	0	0	0	0	1	0	X	X	X	210000h to 217FFFh
	SA74	1	0	0	0	0	1	1	X	X	X	218000h to 21FFFFh
	SA75	1	0	0	0	1	0	0	X	X	X	220000h to 227FFFh
	SA76	1	0	0	0	1	0	1	X	X	X	228000h to 22FFFFh
	SA77	1	0	0	0	1	1	0	X	X	X	230000h to 237FFFh
	SA78	1	0	0	0	1	1	1	X	X	X	238000h to 23FFFFh
	SA79	1	0	0	1	0	0	0	X	X	X	240000h to 247FFFh
	SA80	1	0	0	1	0	0	1	X	X	X	248000h to 24FFFFh
	SA81	1	0	0	1	0	1	0	X	X	X	250000h to 257FFFh
	SA82	1	0	0	1	0	1	1	X	X	X	258000h to 25FFFFh
	SA83	1	0	0	1	1	0	0	X	X	X	260000h to 267FFFh
	SA84	1	0	0	1	1	0	1	X	X	X	268000h to 26FFFFh
	SA85	1	0	0	1	1	1	0	X	X	X	270000h to 277FFFh
	SA86	1	0	0	1	1	1	1	X	X	X	278000h to 27FFFFh
	SA87	1	0	1	0	0	0	0	X	X	X	280000h to 287FFFh
	SA88	1	0	1	0	0	0	1	X	X	X	288000h to 28FFFFh
	SA89	1	0	1	0	0	1	0	X	X	X	290000h to 297FFFh
	SA90	1	0	1	0	0	1	1	X	X	X	298000h to 29FFFFh
	SA91	1	0	1	0	1	0	0	X	X	X	2A0000h to 2A7FFFh
	SA92	1	0	1	0	1	0	1	X	X	X	2A8000h to 2AFFFFh
	SA93	1	0	1	0	1	1	0	X	X	X	2B0000h to 2B7FFFh
	SA94	1	0	1	0	1	1	1	X	X	X	2B8000h to 2BFFFFh
	SA95	1	0	1	1	0	0	0	X	X	X	2C0000h to 2C7FFFh
	SA96	1	0	1	1	0	0	1	X	X	X	2C8000h to 2CFFFFh
	SA97	1	0	1	1	0	1	0	X	X	X	2D0000h to 2D7FFFh
	SA98	1	0	1	1	0	1	1	X	X	X	2D8000h to 2DFFFFh
	SA99	1	0	1	1	1	0	0	X	X	X	2E0000h to 2E7FFFh
	SA100	1	0	1	1	1	0	1	X	X	X	2E8000h to 2EFFFFh
	SA101	1	0	1	1	1	1	0	X	X	X	2F0000h to 2F7FFFh
	SA102	1	0	1	1	1	1	1	X	X	X	2F8000h to 2FFFFFh
	SA103	1	1	0	0	0	0	0	X	X	X	300000h to 307FFFh
	SA104	1	1	0	0	0	0	1	X	X	X	308000h to 30FFFFh
	SA105	1	1	0	0	0	1	0	X	X	X	310000h to 317FFFh
	SA106	1	1	0	0	0	1	1	X	X	X	318000h to 31FFFFh
	SA107	1	1	0	0	1	0	0	X	X	X	320000h to 327FFFh
	SA108	1	1	0	0	1	0	1	X	X	X	328000h to 32FFFFh
	SA109	1	1	0	0	1	1	0	X	X	X	330000h to 337FFFh
	SA110	1	1	0	0	1	1	1	X	X	X	338000h to 33FFFFh
	SA111	1	1	0	1	0	0	0	X	X	X	340000h to 347FFFh
	SA112	1	1	0	1	0	0	1	X	X	X	348000h to 34FFFFh
	SA113	1	1	0	1	0	1	0	X	X	X	350000h to 357FFFh
	SA114	1	1	0	1	0	1	1	X	X	X	358000h to 35FFFFh
	SA115	1	1	0	1	1	0	0	X	X	X	360000h to 367FFFh
	SA116	1	1	0	1	1	0	1	X	X	X	368000h to 36FFFFh
	SA117	1	1	0	1	1	1	0	X	X	X	370000h to 377FFFh
	SA118	1	1	0	1	1	1	1	X	X	X	378000h to 37FFFFh

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Bank	Sector	Sector Address										Address Range
		Bank Address										Word Mode
		A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	
Bank D	SA119	1	1	1	0	0	0	0	X	X	X	380000h to 387FFFh
	SA120	1	1	1	0	0	0	1	X	X	X	388000h to 38FFFFh
	SA121	1	1	1	0	0	1	0	X	X	X	390000h to 397FFFh
	SA122	1	1	1	0	0	1	1	X	X	X	398000h to 39FFFFh
	SA123	1	1	1	0	1	0	0	X	X	X	3A0000h to 3A7FFFh
	SA124	1	1	1	0	1	0	1	X	X	X	3A8000h to 3AFFFFh
	SA125	1	1	1	0	1	1	0	X	X	X	3B0000h to 3B7FFFh
	SA126	1	1	1	0	1	1	1	X	X	X	3B8000h to 3BFFFFh
	SA127	1	1	1	1	0	0	0	X	X	X	3C0000h to 3C7FFFh
	SA128	1	1	1	1	0	0	1	X	X	X	3C8000h to 3CFFFFh
	SA129	1	1	1	1	0	1	0	X	X	X	3D0000h to 3D7FFFh
	SA130	1	1	1	1	0	1	1	X	X	X	3D8000h to 3DFFFFh
	SA131	1	1	1	1	1	0	0	X	X	X	3E0000h to 3E7FFFh
	SA132	1	1	1	1	1	0	1	X	X	X	3E8000h to 3EFFFFh
	SA133	1	1	1	1	1	1	0	X	X	X	3F0000h to 3F7FFFh
	SA134	1	1	1	1	1	1	1	0	0	0	3F8000h to 3F8FFFh
	SA135	1	1	1	1	1	1	1	0	0	1	3F9000h to 3F9FFFh
	SA136	1	1	1	1	1	1	1	0	1	0	3FA000h to 3FAFFFh
	SA137	1	1	1	1	1	1	1	0	1	1	3FB000h to 3FBFFFh
	SA138	1	1	1	1	1	1	1	1	0	0	3FC000h to 3FCFFFh
	SA139	1	1	1	1	1	1	1	1	0	1	3FD000h to 3FDFFFh
	SA140	1	1	1	1	1	1	1	1	1	0	3FE000h to 3FEFFFh
	SA141	1	1	1	1	1	1	1	1	1	1	3FF000h to 3FFFFFh

Table 5 Sector Group Addresses

Sector Group	A_{21}	A_{20}	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	0	0	1	X	X	X	SA8 to SA10
						1	0				
						1	1				
SGA9	0	0	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	0	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	0	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	0	0	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	0	0	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	0	0	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	0	0	1	1	1	X	X	X	X	X	SA35 to SA38
SGA16	0	1	0	0	0	X	X	X	X	X	SA39 to SA42
SGA17	0	1	0	0	1	X	X	X	X	X	SA43 to SA46
SGA18	0	1	0	1	0	X	X	X	X	X	SA47 to SA50
SGA19	0	1	0	1	1	X	X	X	X	X	SA51 to SA54
SGA20	0	1	1	0	0	X	X	X	X	X	SA55 to SA58
SGA21	0	1	1	0	1	X	X	X	X	X	SA59 to SA62
SGA22	0	1	1	1	0	X	X	X	X	X	SA63 to SA66
SGA23	0	1	1	1	1	X	X	X	X	X	SA67 to SA70
SGA24	1	0	0	0	0	X	X	X	X	X	SA71 to SA74
SGA25	1	0	0	0	1	X	X	X	X	X	SA75 to SA78
SGA26	1	0	0	1	0	X	X	X	X	X	SA79 to SA82
SGA27	1	0	0	1	1	X	X	X	X	X	SA83 to SA86
SGA28	1	0	1	0	0	X	X	X	X	X	SA87 to SA90
SGA29	1	0	1	0	1	X	X	X	X	X	SA91 to SA94
SGA30	1	0	1	1	0	X	X	X	X	X	SA95 to SA98
SGA31	1	0	1	1	1	X	X	X	X	X	SA99 to SA102
SGA32	1	1	0	0	0	X	X	X	X	X	SA103 to SA106
SGA33	1	1	0	0	1	X	X	X	X	X	SA107 to SA110
SGA34	1	1	0	1	0	X	X	X	X	X	SA111 to SA114
SGA35	1	1	0	1	1	X	X	X	X	X	SA115 to SA118
SGA36	1	1	1	0	0	X	X	X	X	X	SA119 to SA122
SGA37	1	1	1	0	1	X	X	X	X	X	SA123 to SA126
SGA38	1	1	1	1	0	X	X	X	X	X	SA127 to SA130
SGA39	1	1	1	1	1	0	0	X	X	X	SA131 to SA133
						0	1				
						1	0				
SGA40	1	1	1	1	1	1	1	0	0	0	SA134
SGA41	1	1	1	1	1	1	1	0	0	1	SA135
SGA42	1	1	1	1	1	1	1	0	1	0	SA136
SGA43	1	1	1	1	1	1	1	0	1	1	SA137
SGA44	1	1	1	1	1	1	1	1	0	0	SA138
SGA45	1	1	1	1	1	1	1	1	0	1	SA139
SGA46	1	1	1	1	1	1	1	1	1	0	SA140
SGA47	1	1	1	1	1	1	1	1	1	1	SA141

Table 6 Flash Memory Autoselect Codes

Type	A_{21} to A_{12}	A_6	A_3	A_2	A_1	A_0	Code (HEX)
Manufacture's Code	BA	L	L	L	L	L	04h
Device Code	BA	L	L	L	L	H	227Eh
Extended Device Code *2	BA	L	H	H	H	L	2202h
	BA	L	H	H	H	H	2201h
Sector Group Protection	Sector Group Addresses	L	L	L	H	L	01h*1

Legend: L = V_{IL}, H = V_{IH}. See DC Characteristics for voltage levels.

*1 : Outputs 01h at protected sector group addresses and outputs 00h at unprotected sector group addresses.

*2 : A read cycle at address (BA) 01h outputs device code. When 227Eh was output, this indicates that there will require two additional codes, called Extended Device Codes. Therefore the system may continue reading out these Extended Device Codes at the address of (BA) 0Eh, as well as at (BA) 0Fh.

Table 7 Flash Memory Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
Autoselect	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
Program Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Program Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Sector Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
Erase Suspend	1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume	1	BA	30h	—	—	—	—	—	—	—	—	—	—
Extended Sector Group Protection *2	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
Set to Fast Mode	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
Fast Program *1	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
Reset from Fast Mode *1	2	BA	90h	XXXh	*4 F0h	—	—	—	—	—	—	—	—
Query	1	(BA) 55h	98h	—	—	—	—	—	—	—	—	—	—
Hi-ROM Entry	3	555h	AAh	2AAh	55h	555h	88h	—	—	—	—	—	—
Hi-ROM Program *3	4	555h	AAh	2AAh	55h	555h	A0h	(HRA) PA	PD	—	—	—	—
Hi-ROM Exit *3	4	555h	AAh	2AAh	55h	(HRBA)5 55h	90h	XXXh	00h	—	—	—	—

(Continued)

(Continued)

*1: This command is valid during Fast Mode.

*2: This command is valid while $\overline{\text{RESET}}$ = V_{ID}.

*3: This command is valid during Hi-ROM mode.

*4: The data “00h” is also acceptable.

Notes: 1. Address bits A_{21} to A_{11} = X = “H” or “L” for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA), and Sector Group Address (SPA).

2. Bus operations are defined in ■ DEVICE BUS OPERATION.

3. RA =Address of the memory location to be read
PA = Address of the memory location to be programmed
Addresses are latched on the falling edge of the write pulse.
SA = Address of the sector to be erased. The combination of A_{21}, A_{20}, A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
BA = Bank Address (A_{21}, A_{20}, A_{19})

4. RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA. Data is latched on the falling edge of write pulse.

5. SPA =Sector group address to be protected. Set sector group address and (A_6, A_3, A_2, A_1, A_0) = (0, 0, 0, 1, 0).
SD = Sector group protection verify data. Output 01h at protected sector group addresses and output 00h at unprotected sector group addresses.

6. HRA = Address of the Hi-ROM area: 000000h to 00007Fh

7. HRBA = Bank Address of the Hi-ROM area (A_{21} = A_{20} = A_{19} = V_{IL})

8. The system should generate the following address patterns: 555h or 2AAh to addresses A_{10} to A_0

9. Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.

10. The command combinations not described in this table are illegal.

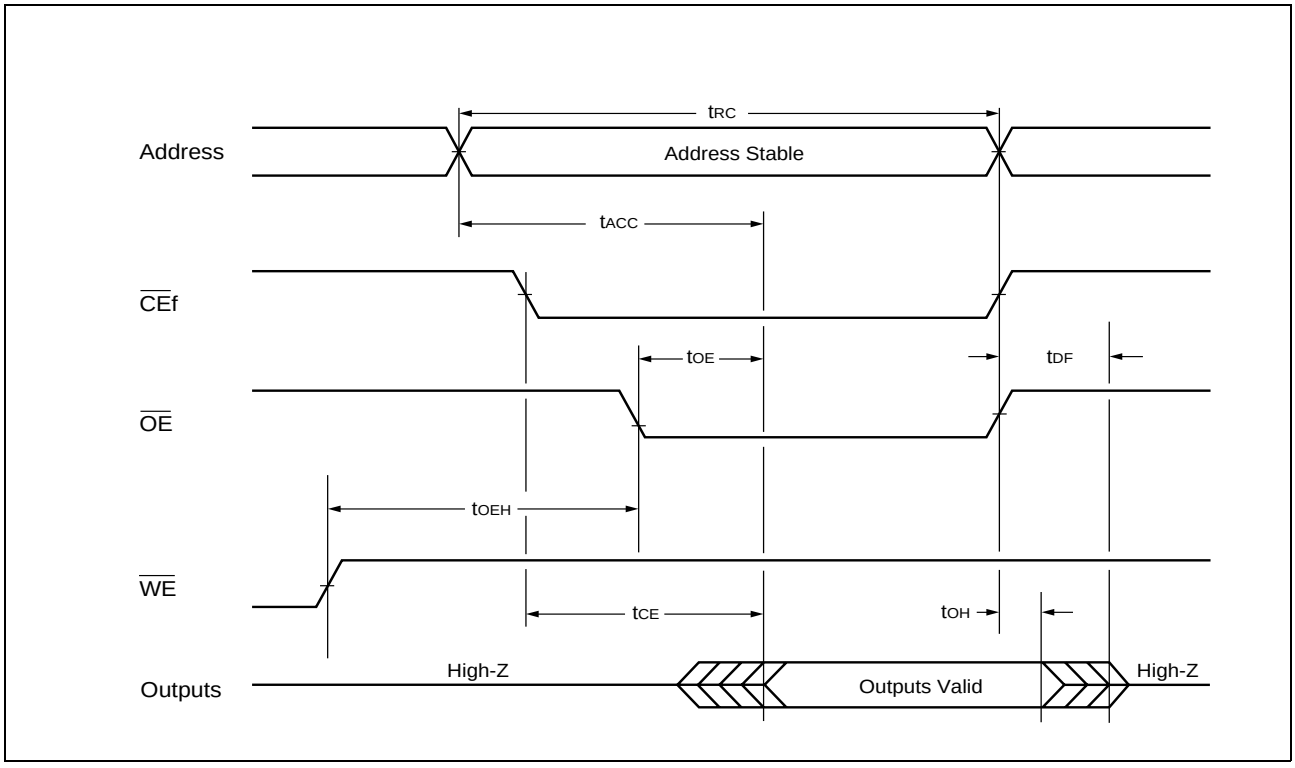
■ ELECTRICAL CHARACTERISTICS (AC Characteristics)

- Read Only Operations Characteristics (Flash)

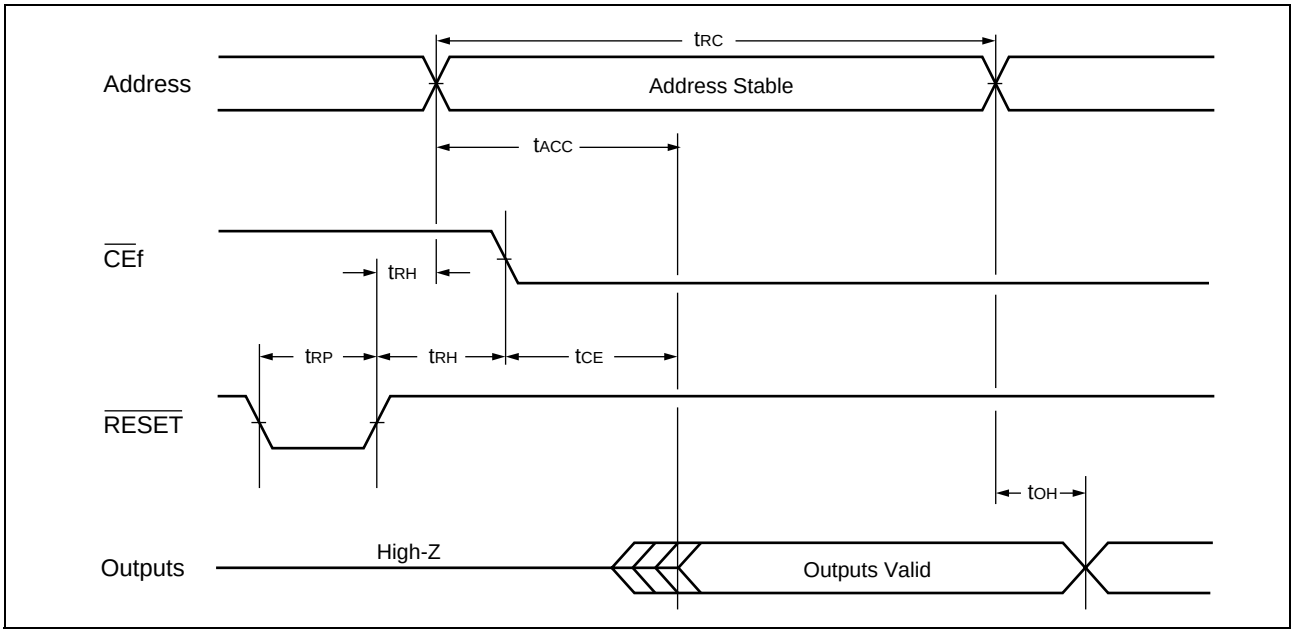
Parameter	Symbol		Condition	Value (Note)		Unit
	JEDEC	Standard		Min.	Max.	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
Chip Enable to Output Delay	t_{ELQV}	$t_{CE}f$	$\overline{OE} = V_{IL}$	—	70	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	ns
Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	µs

Note: Test Conditions– Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to $V_{CC}f$
Timing measurement reference level
Input: $0.5 \times V_{CC}f$
Output: $0.5 \times V_{CC}f$

- **Read Operation Timing Diagram (Flash)**



- **Hardware Reset/Read Operation Timing Diagram (Flash)**



- **Write/Erase/Program Operations (Flash)**

Parameter		Symbol		Value			Unit
		JEDEC	Standard	Min.	Typ.	Max.	
Write Cycle Time		t_{AVAV}	t_{WC}	70	—	—	ns
Address Setup Time		t_{AVWL}	t_{AS}	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling		—	t_{ASO}	12	—	—	ns
Address Hold Time		t_{WLAX}	t_{AH}	30	—	—	ns
Address Hold Time from $\overline{CEf}$ or $\overline{OE}$ High During Toggle Bit Polling		—	t_{AHT}	0	—	—	ns
Data Setup Time		t_{DVWH}	t_{DS}	25	—	—	ns
Data Hold Time		t_{WHDX}	t_{DH}	0	—	—	ns
Output Enable Hold Time	Read	—	t_{OEH}	0	—	—	ns
	Toggle and $\overline{Data}$ Polling			10	—	—	ns
$\overline{CEf}$ High During Toggle Bit Polling		—	t_{CEPH}	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling		—	t_{OEPH}	20	—	—	ns
Read Recover Time Before Write		t_{GHWL}	t_{GHWL}	0	—	—	ns
Read Recover Time Before Write		t_{GHEL}	t_{GHEL}	0	—	—	ns
$\overline{CEf}$ Setup Time		t_{ELWL}	t_{CS}	0	—	—	ns
$\overline{WE}$ Setup Time		t_{WLEL}	t_{WS}	0	—	—	ns
$\overline{CEf}$ Hold Time		t_{WHEH}	t_{CH}	0	—	—	ns
$\overline{WE}$ Hold Time		t_{EHWH}	t_{WH}	0	—	—	ns
Write Pulse Width		t_{WLWH}	t_{WP}	35	—	—	ns
$\overline{CEf}$ Pulse Width		t_{ELEH}	t_{CP}	35	—	—	ns
Write Pulse Width High		t_{WHWL}	t_{WPH}	20	—	—	ns
$\overline{CEf}$ Pulse Width High		t_{EHEL}	t_{CPH}	20	—	—	ns
Programming Operation		t_{WHWH1}	t_{WHWH1}	—	6	—	µs
Sector Erase Operation *1		t_{WHWH2}	t_{WHWH2}	—	0.5	—	s
$V_{CC}f$ Setup Time		—	t_{VCS}	50	—	—	µs
Rise Time to V_{ID} *2		—	t_{VIDR}	500	—	—	ns
Rise Time to V_{ACC} *3		—	t_{VACCR}	500	—	—	ns
Voltage Transition Time *2		—	t_{VLHT}	4	—	—	µs
Write Pulse Width *2		—	t_{WPP}	100	—	—	µs

(Continued)

(Continued)

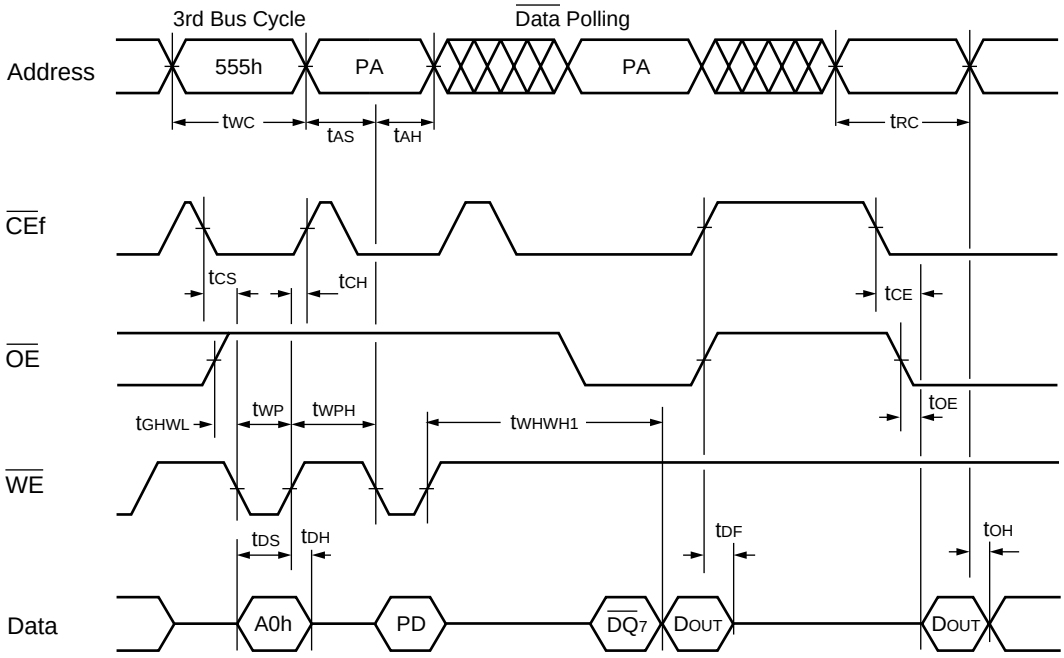
Parameter	Symbol		Value			Unit
	JEDEC	Standard	Min.	Typ.	Max.	
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{OESP}	4	—	—	µs
$\overline{CE}$f Setup Time to $\overline{WE}$ Active *2	—	t_{CSP}	4	—	—	µs
Recover Time from RY/$\overline{BY}$	—	t_{RB}	0	—	—	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	ns
$\overline{RESET}$ High Level Period Before Read	—	t_{RH}	200	—	—	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay	—	t_{BUSY}	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	70	ns
Erase Time-out Time	—	t_{TOW}	50		—	µs
Erase Suspend Transition Time	—	t_{SPD}	—	—	20	µs

*1: This does not include preprogramming time.

*2: This timing is for Sector Group Protection operation.

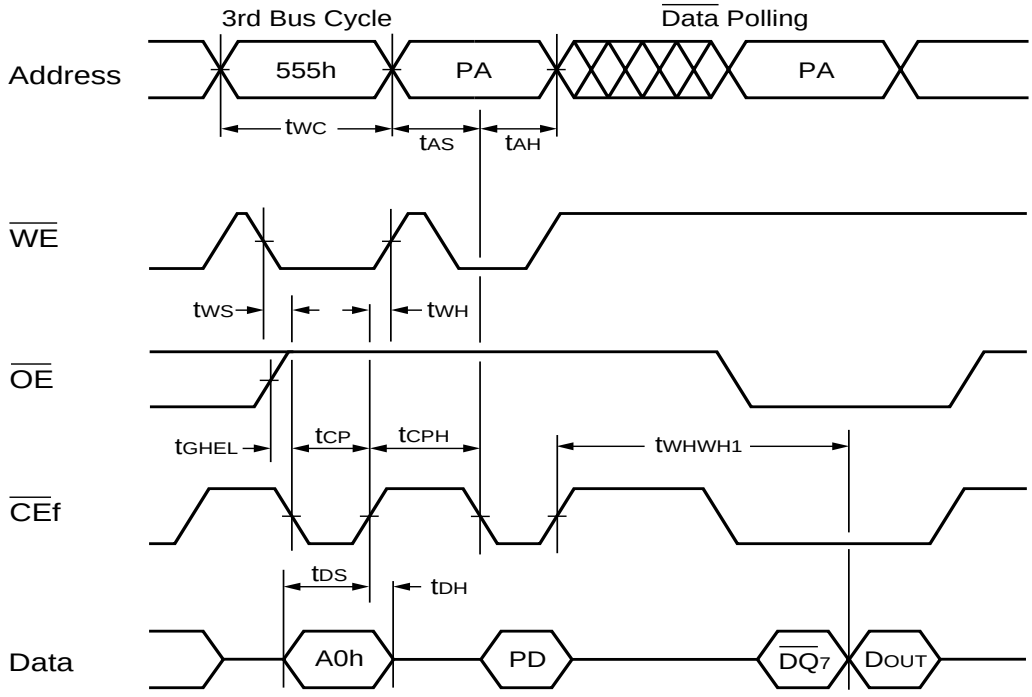
*3: This timing is for Accelerated Program operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**



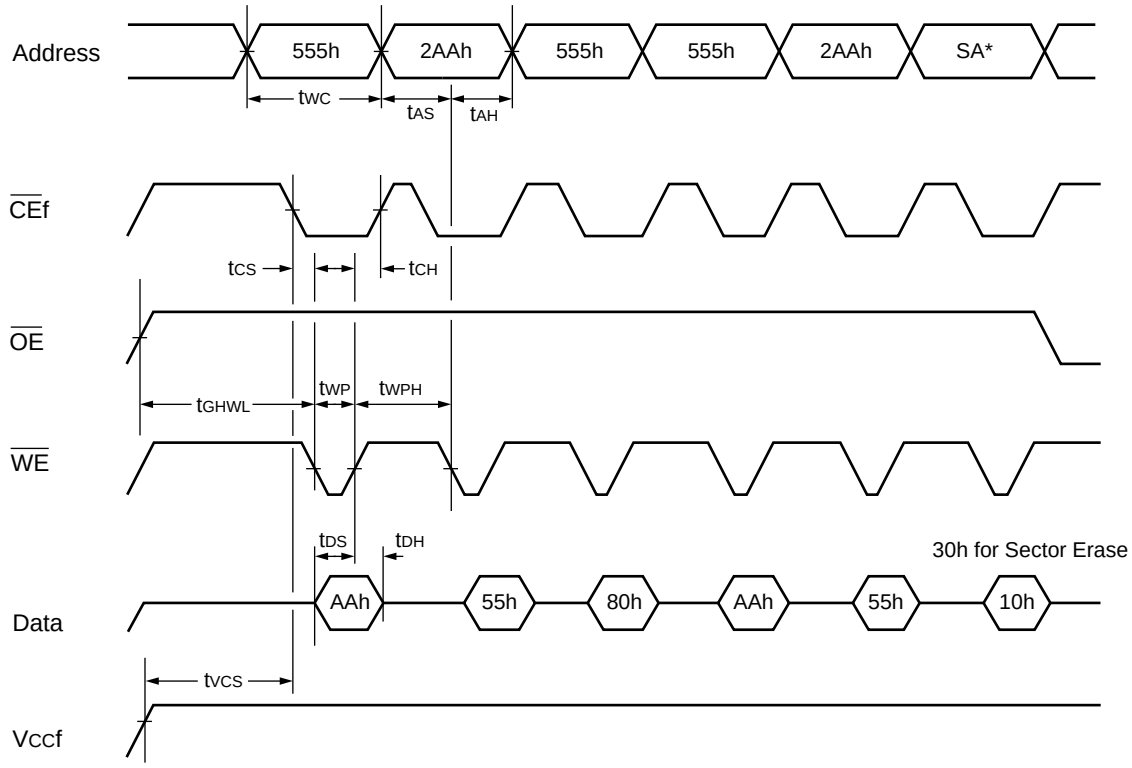
Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at word address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

- **Write Cycle ($\overline{CE}$f control) (Flash)**



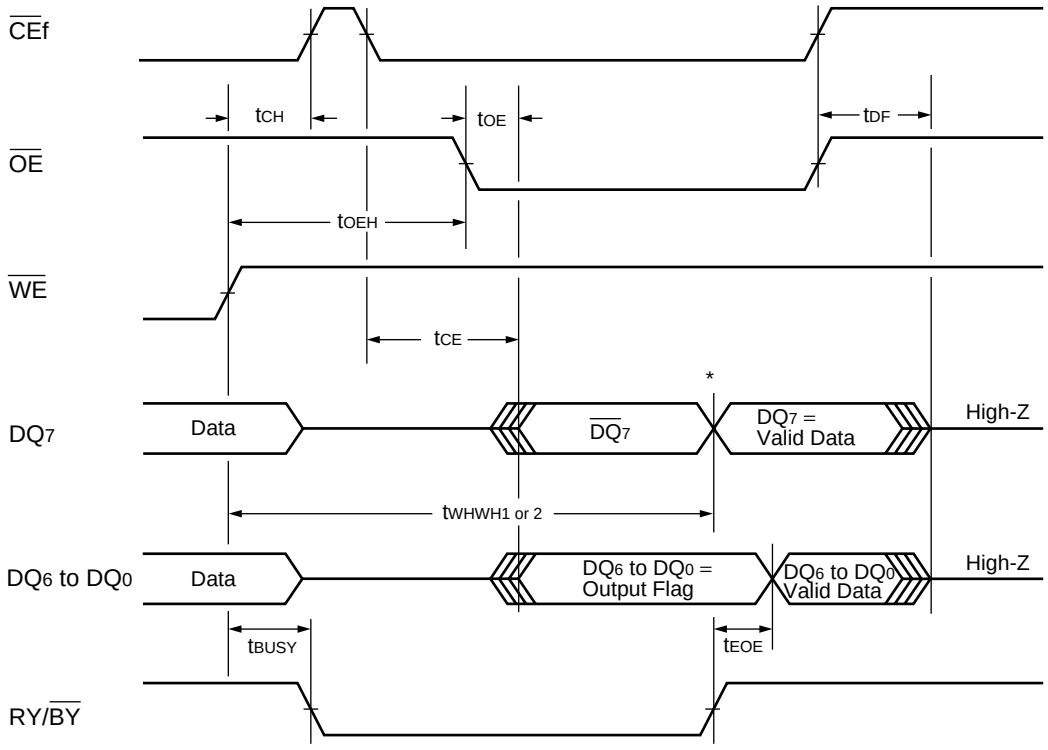
Notes:
1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at word address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



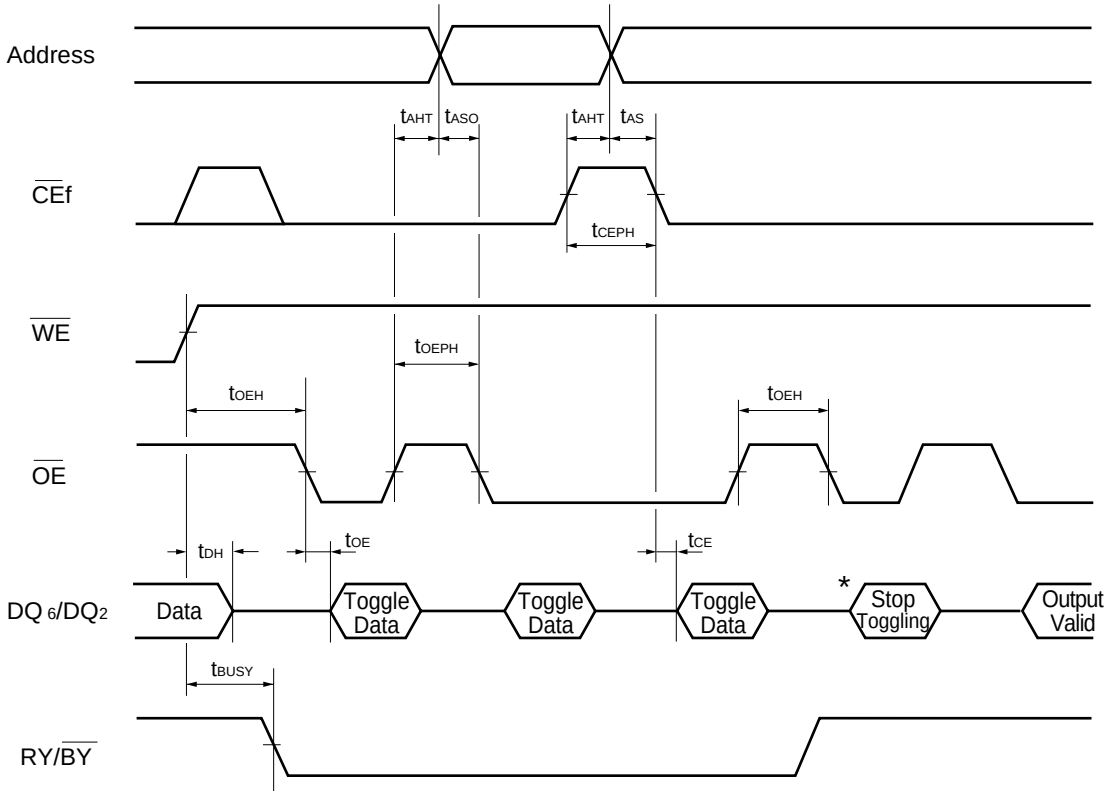
* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



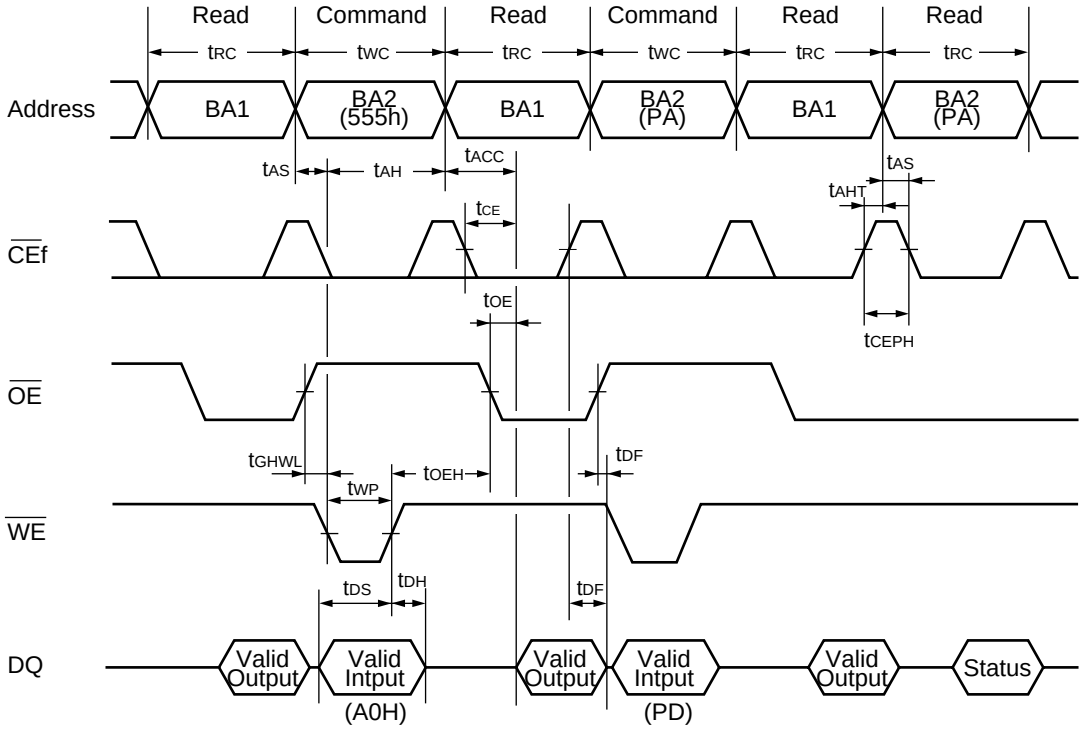
* : DQ_7 = Valid Data (the device has completed the Embedded operation) .

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**



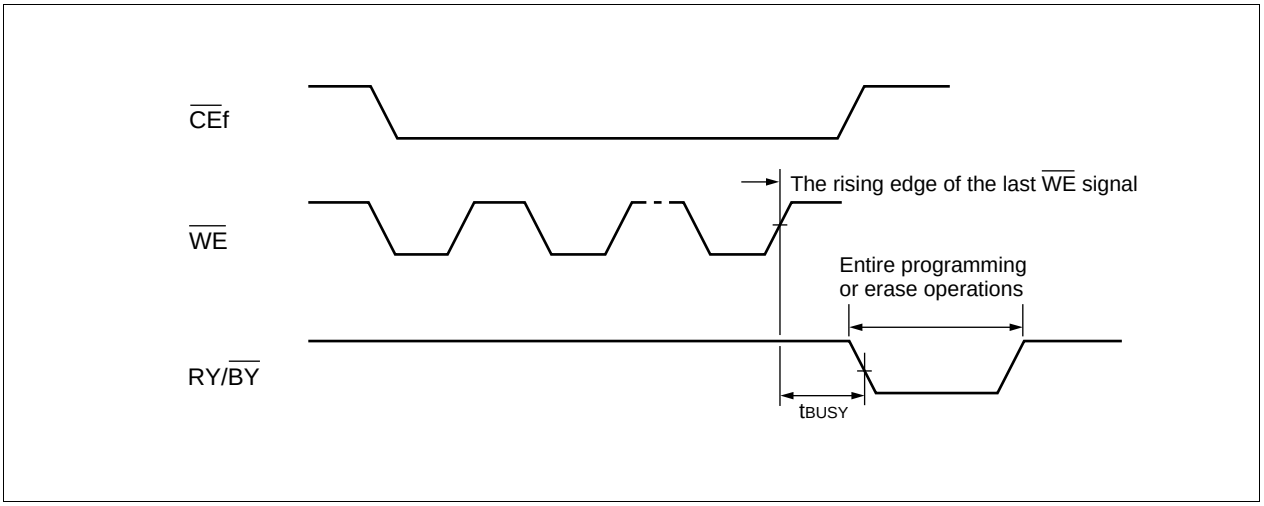
* : DQ_6 stops toggling (the device has completed the Embedded operation).

- **Back-to-back Read/Write Timing Diagram (Flash)**

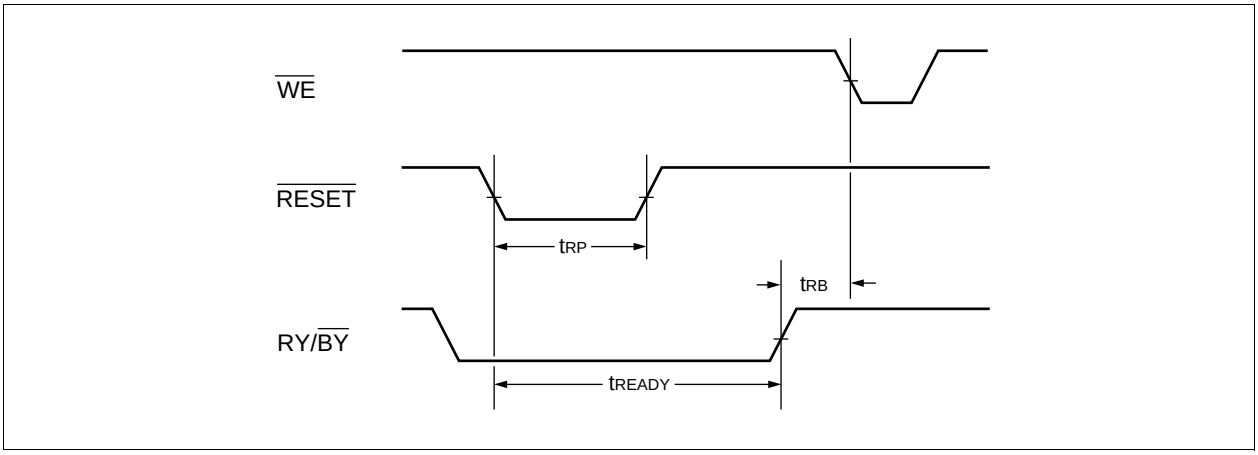


Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1 : Address corresponding to Bank 1
BA2 : Address corresponding to Bank 2

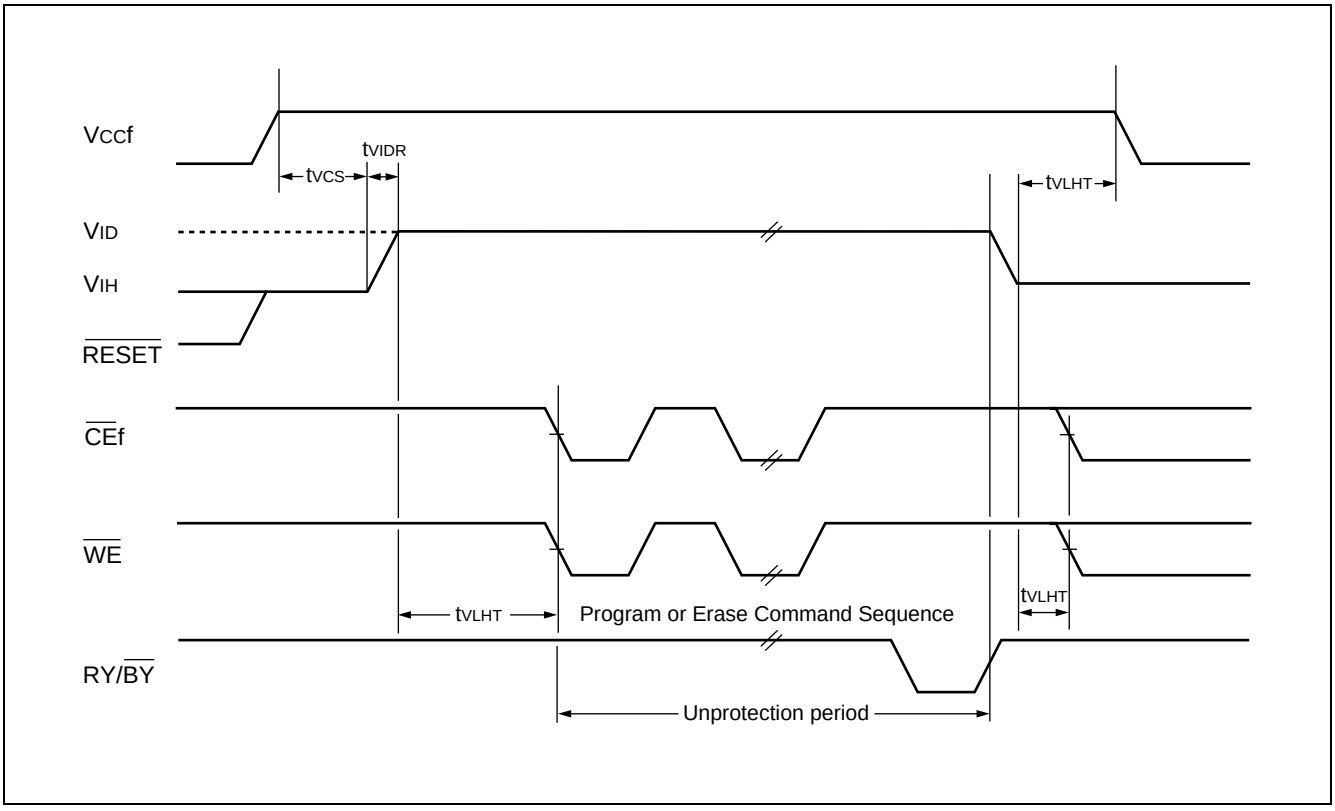
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



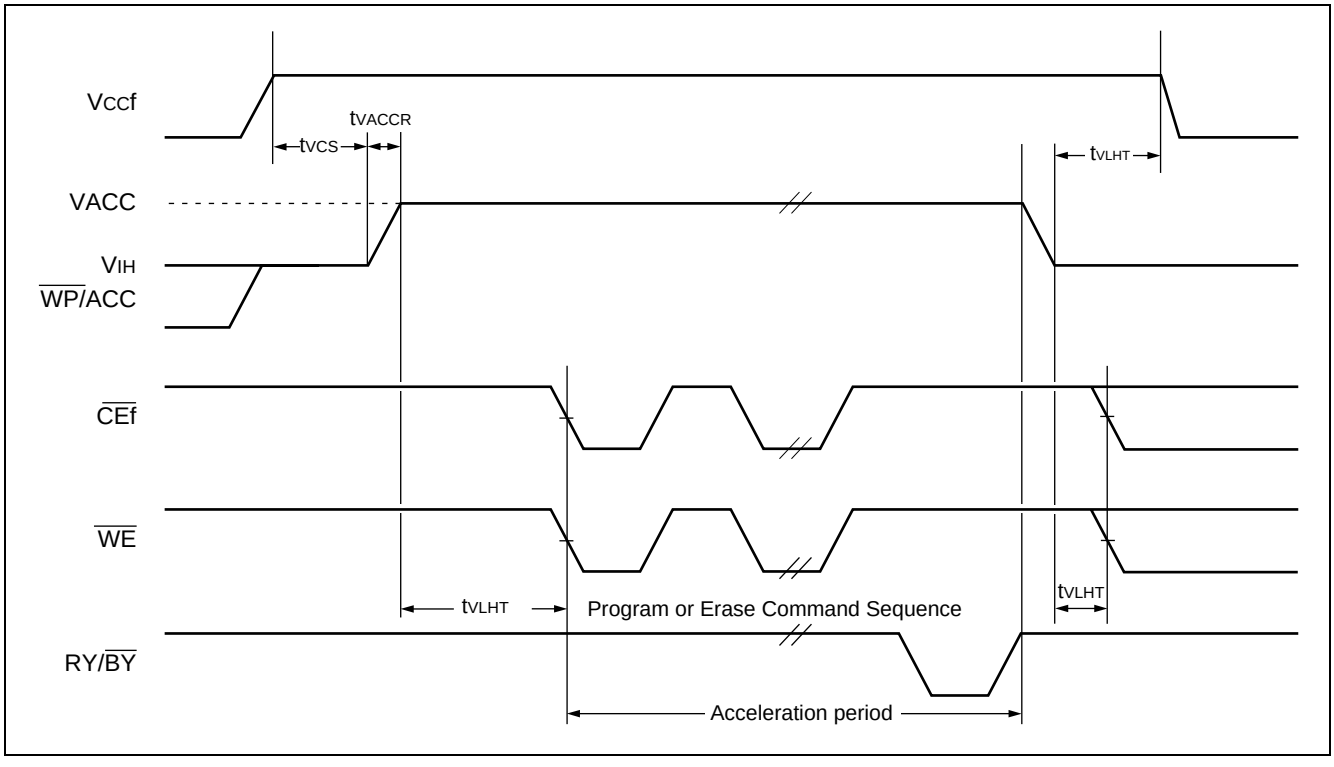
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



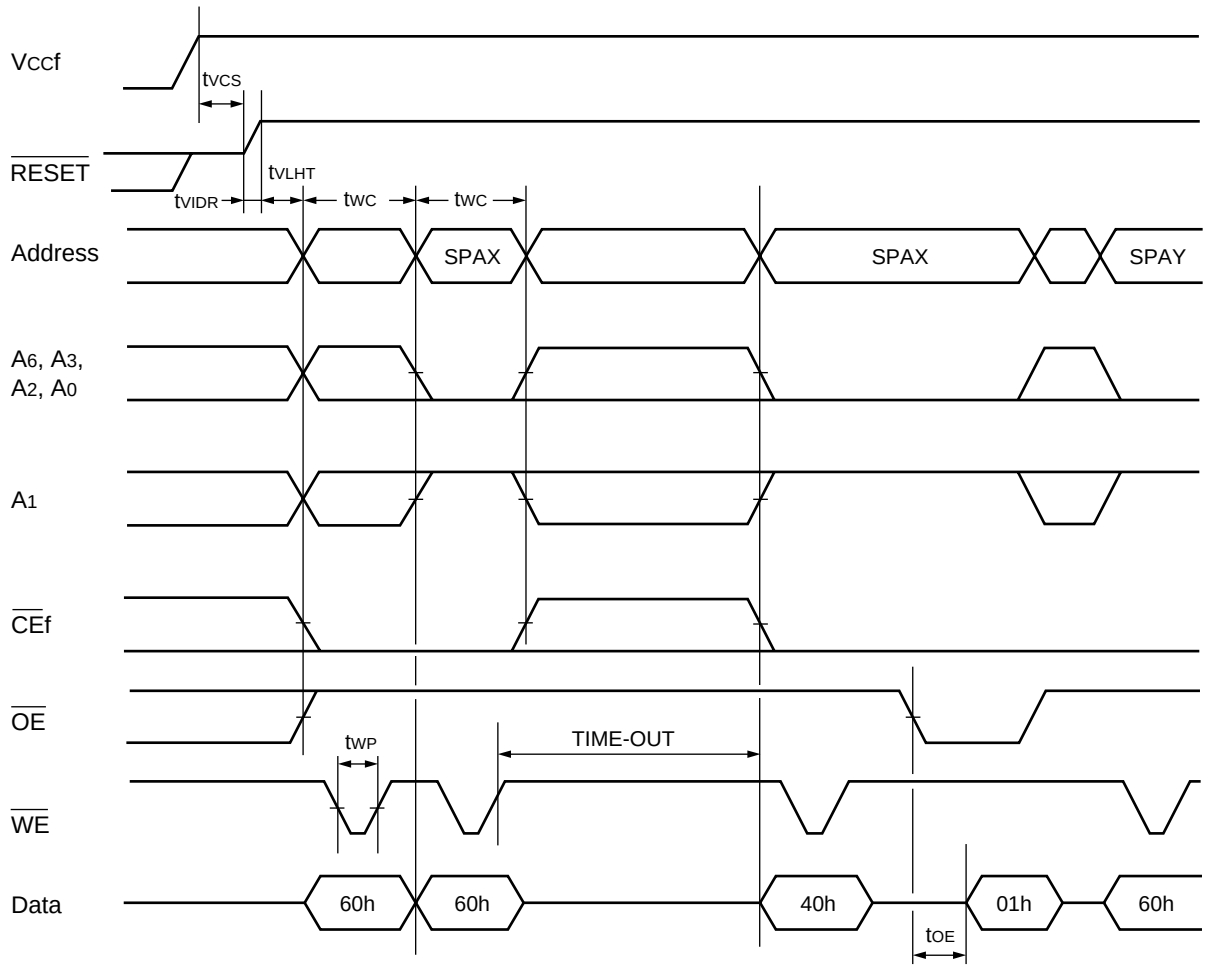
- **Temporary Sector Unprotection (Flash)**



- **Acceleration Mode Timing Diagram (Flash)**



- **Extended Sector Group Protection (Flash)**



SPAX : Sector Group Address to be protected
SPAY : Next Sector Group Address to be protected
TIME-OUT : Time-Out window = 250 μs (Min.)

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Value			Unit	Remarks
	Min.	Typ.	Max.		
Sector Erase Time	—	0.5	2.0	s	Excludes programming time prior to erasure
Word Programming Time	—	6	100	µs	Excludes system-level overhead
Chip Programming Time	—	—	200	s	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycle	

Typical Erase conditions T_A = 25°C, VCCf_1 & VCCf_2 = 2.9V

Typical Program conditions T_A = 25°C, VCCf_1 & VCCf_2 = 2.9V Data= Checker

■ FCRAM Power Down Program Key Table

Basic Key Table

Definition	A16	A17	A19	A20	A21
KEY	Mode Select		Area Select		

A19	A20	A21	AREA
L	L	L	BOTTOM *2
L	H	X	RESERVED
H	L	X	RESERVED
H	H	H	TOP *3

A16	A17	MODE
L	L	NAP *4
L	H	RESERVED
H	L	16M Partial
H	H	SLEEP *4, *5

Available Key Table

MODE	A16	A17	A19	A20	A21	Data Retention Area
	Mode Select		Area Select			
NAP	L	L	X	X	X	None
16M Partial	H	L	L	L	L	Bottom 16M only
	H	L	H	H	H	Top 16M only
SLEEP	H	H	X	X	X	None

Notes *1: The Power Down Program can be performed one time after compliance of Power-up timings and it should not be re-programmed after regular Read or Write.
Unspecified addresses, A0 to A15, can be either High or Low during the programming.
The RESERVED key should not be used.

*2: BOTTOM area is from the lowest address location. (i.e., A(20:0) = L)

*3: TOP area is from the highest address location. (i.e., A(20:0) = H)

*4: NAP and SLEEP do not retain the data and Area Select is ignored.

*5: Default state. Power Down Program to this SLEEP mode can be omitted.

■ ELECTRICAL CHARACTERISTICS (AC Characteristics)

- **READ OPERATION (FCRAM)**

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{RC}	70	—	ns	
Chip Enable Access Time	t_{CE}	—	65	ns	*1,*3
Output Enable Access Time	t_{OE}	—	40	ns	*1
Address Access Time	t_{AA}	—	65	ns	*1,*4
Output Data Hold Time	t_{OH}	5	—	ns	*1
$\overline{CE}$1r Low to Output Low-Z	t_{CLZ}	5	—	ns	*2
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*2
$\overline{CE}$1r High to Output High-Z	t_{CHZ}	—	20	ns	*2
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*2
Address Setup Time to $\overline{CE}$1r Low	t_{ASC}	–5	—	ns	*5
Address Setup Time to $\overline{OE}$	t_{ASO}	25	—	ns	*3,*6
	$t_{ASO(ABS)}$	10	—	ns	*7
$\overline{LB}$ / $\overline{UB}$ Setup Time to $\overline{CE}$1r Low	t_{BSC}	–5	—		*5
$\overline{LB}$ / $\overline{UB}$ Setup Time to $\overline{OE}$ Low	t_{BSO}	10	—		
Address Invalid Time	t_{AX}	—	5	ns	*4,*8
Address Hold Time from $\overline{CE}$1r Low	t_{CLAH}	70	—	ns	*4
Address Hold Time from $\overline{OE}$ Low	t_{OLAH}	45	—	ns	*4,*9
Address Hold Time from $\overline{CE}$1r High	t_{CHAH}	–5	—	ns	
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{LB}$ / $\overline{UB}$ Hold Time from $\overline{CE}$1r High	t_{CHBH}	–5	—		
$\overline{LB}$ / $\overline{UB}$ Hold Time from $\overline{OE}$ High	t_{OHBH}	–5	—		
$\overline{CE}$1r Low to $\overline{OE}$ Low Delay Time	t_{CLOL}	25	1000	ns	*3,*6,*9,*10
$\overline{OE}$ Low to $\overline{CE}$1r High Delay Time	t_{OLCH}	45	—	ns	*9
$\overline{CE}$1r High Pulse Width	t_{CP}	12	—	ns	
$\overline{OE}$ High Pulse Width	t_{OP}	25	1000	ns	*6,*9,*10
	$t_{OP(ABS)}$	12	—	ns	*7

Notes *1: The output load is 30pF.

*2: The output load is 5pF.

*3: The t_{CE} is applicable if $\overline{OE}$ is brought to Low before $\overline{CE}$1r goes Low and is also applicable if actual value of both or either t_{ASO} or t_{CLOL} is shorter than specified value.

*4: Applicable only to A0 and A1 when both $\overline{CE}$1r and $\overline{OE}$ are kept at Low for the address access.

*5: Applicable if $\overline{OE}$ is brought to Low before $\overline{CE}$1r goes Low.

*6: The t_{ASO}, t_{CLOL}(min) and t_{OP}(min) are reference values when the access time is determined by t_{OE}. If actual value of each parameter is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value. For example, if actual t_{ASO}, t_{ASO}(actual), is shorter than specified minimum value, t_{ASO}(min), during $\overline{OE}$ control access (ie., $\overline{CE}$1r stays Low), the t_{OE} become t_{OE}(max) + t_{ASO}(min) – t_{ASO}(actual).

*7: The $t_{ASO(ABS)}$ and $t_{OP(ABS)}$ is the absolute minimum value during $\overline{OE}$ control access.

*8: The t_{AX} is applicable when both A0 and A1 are switched from previous state.

*9: If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become t_{RC}(min) – t_{CLOL}(actual) or t_{RC}(min) – t_{OP}(actual).

*10: Maximum value is applicable if $\overline{CE}$1r is kept at Low.

- **WRITE OPERATION (FCRAM)**

Parameter	Symbol	Value		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{WC}	70	—	ns	*1
Address Setup Time	t_{AS}	0	—	ns	*2
Address Hold Time	t_{AH}	35	—	ns	*2
$\overline{CE}$1r Write Setup Time	t_{CS}	0	1000	ns	
$\overline{CE}$1r Write Hold Time	t_{CH}	0	1000	ns	
$\overline{WE}$ Setup Time	t_{WS}	0	—	ns	
$\overline{WE}$ Hold Time	t_{WH}	0	—	ns	
$\overline{LB}$ and $\overline{UB}$ Setup Time	t_{BS}	–5	—	ns	
$\overline{LB}$ and $\overline{UB}$ Hold Time	t_{BH}	–5	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	0	1000	ns	*3
$\overline{OE}$ Hold Time	t_{OEH}	25	1000	ns	*3, *4
	$t_{OEH(ABS)}$	12	—	ns	*5
$\overline{OE}$ High to $\overline{CE}$1r Low Setup Time	t_{OHCL}	–5	—	ns	*6
$\overline{OE}$ High to Address Hold Time	t_{OHAH}	–5	—	ns	*7
$\overline{CE}$1r Write Pulse Width	t_{CW}	45	—	ns	*1, *8
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*1, *8
$\overline{CE}$1r Write Recovery Time	t_{WRC}	10	—	ns	*1, *9
$\overline{WE}$ Write Recovery Time	t_{WR}	10	1000	ns	*1, *3, *9
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{CE}$1r High Pulse Width	t_{CP}	12	—	ns	*9

Notes: *1: Minimum value must be equal or greater then the sum of actual t_{CW} (or t_{WP}) and t_{WRC} (or t_{WR}).

*2: New write address is valid from either $\overline{CE}$1r or $\overline{WE}$ is bought to High.

*3: The t_{OEH} is specified from end of t_{WC}(min). The t_{OEH}(min) is a reference value when the access time is determined by t_{OE}.

If actual value, t_{OEH}(actual) is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.

*4: The t_{OEH}(max) is applicable if $\overline{CE}$1r is kept at Low and both $\overline{WE}$ and $\overline{OE}$ are kept at High.

*5: The $t_{OEH(ABS)}$ is the absolute minimum value if write cycle is termnated by $\overline{WE}$ and $\overline{CE}$1r stays Low.

*6: t_{OHCL}(min) must be satisfied if read operation is not performed prior to write operation.
In case $\overline{OE}$ is disabled after t_{OHCL}(min), $\overline{WE}$ Low must be asserted after t_{RC}(min) from $\overline{CE}$1r Low.
In other words, read operation is initiated if t_{OHCL} (min) is not satisfied.

*7: Applicable if $\overline{CE}$1r stays Low after read operation.

*8: t_{CW} and t_{WP} is applicable if write operation is initiated by $\overline{CE}$1r and $\overline{WE}$, respectively.

*9: t_{WRC} and t_{WR} is applicable if write operation is terminated by $\overline{CE}$1r and $\overline{WE}$, respectively.
The t_{WR}(min) can be ignored if $\overline{CE}$1r is brought to High together or after $\overline{WE}$ is brought to High.
In such case, the t_{CP}(min) must be satisfied.

- **POWER DOWN and POWER DOWN PROGRAM PARAMETERS (FCRAM)**

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
CE2r Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2r Low Hold Time after Power Down Entry	t_{C2LP}	70	—	ns	
$\overline{CE}$1r High Hold Time following CE2r High after Power Down Exit(SLEEP mode only)	t_{CHH}	350	—	µs	
$\overline{CE}$1r High Setup Time following CE2r High after Power Down Exit(Except for SLEEP mode)	t_{CHHN}	1	—	µs	
$\overline{CE1}$r High Setup Time following CE2r High after Power Down Exit	t_{CHS}	10	—	ns	
$\overline{CE1}$r High to $\overline{PE}$ Low Setup Time	t_{EPS}	70	—	ns	*1
$\overline{PE}$ Power Down Program Pulse Width	t_{EP}	70	—	ns	*1
$\overline{PE}$ High to $\overline{CE1}$r Low Hold Time	t_{EPH}	70	—	ns	*1
Address Setup Time to $\overline{PE}$ High	t_{EAS}	15	—	ns	*1
Address Setup Time from $\overline{PE}$ High	t_{EAH}	0	—	ns	*1

Notes: *1: Applicable to Down Program.

- **OTHER TIMING PARAMETERS (FCRAM)**

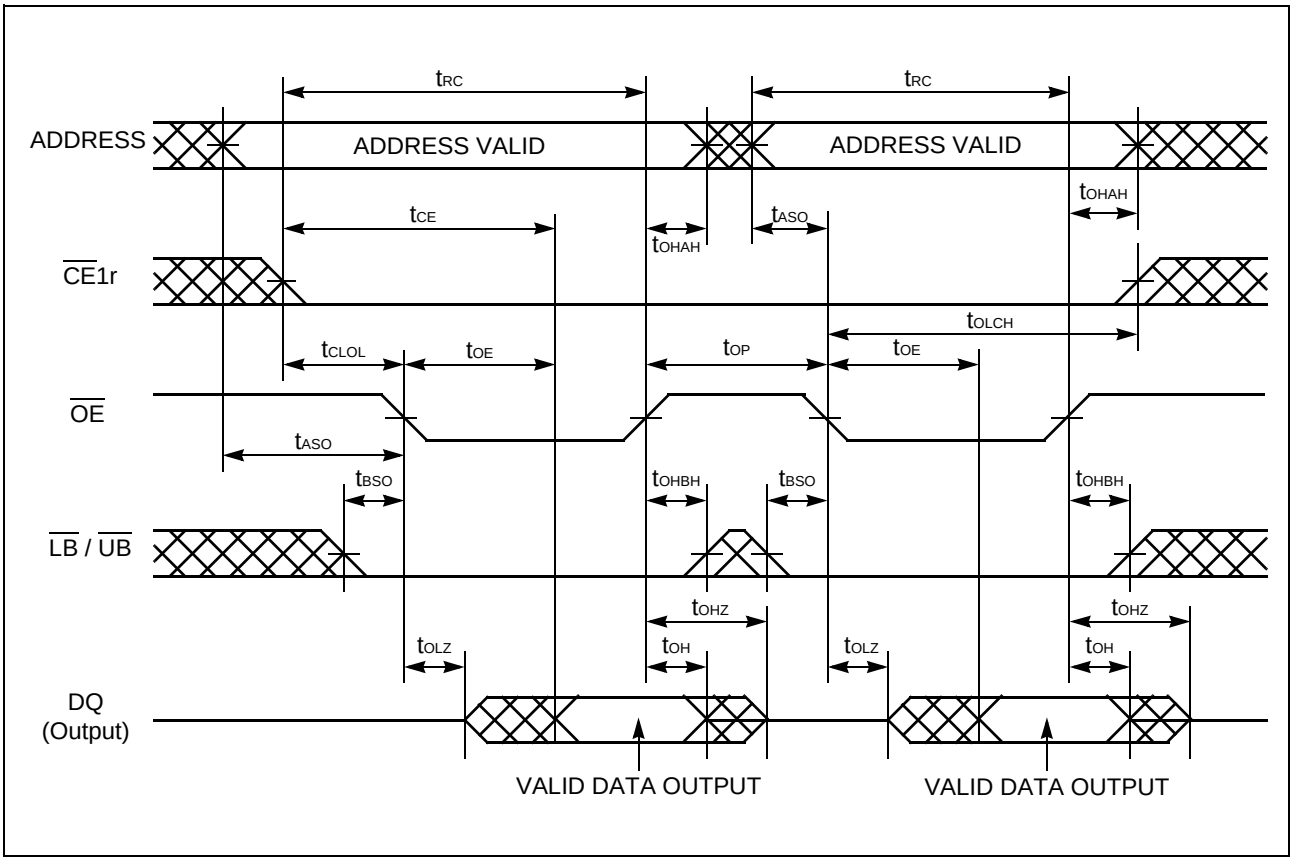
Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
$\overline{CE}$1r High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1r High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2r Low Hold Time after Power-up	t_{C2LH}	50	—	µs	*2
CE2r High Hold Time after Power-up	t_{C2HL}	50	—	µs	*3
$\overline{CE}$1r High Hold Time following CE2r High after Power-up	t_{CHH}	350	—	µs	*2
Input Transition Time	t_T	1	25	ns	*4

Notes: *1: It may write some data into any address location if t_{CHWX} is not satisfied.
*2: Must satisfy t_{CHH}(min) after t_{C2LH}(min).
*3: Requires Power Down mode entry and exit after t_{C2HL}.
*4: The input Trasition Time(t_T) at AC testing is 5ns as shown in below. If actual t_T is longer than 5ns, it may violate AC specification of some timing parameters.

- **AC TEST CONDITIONS (FCRAM)**

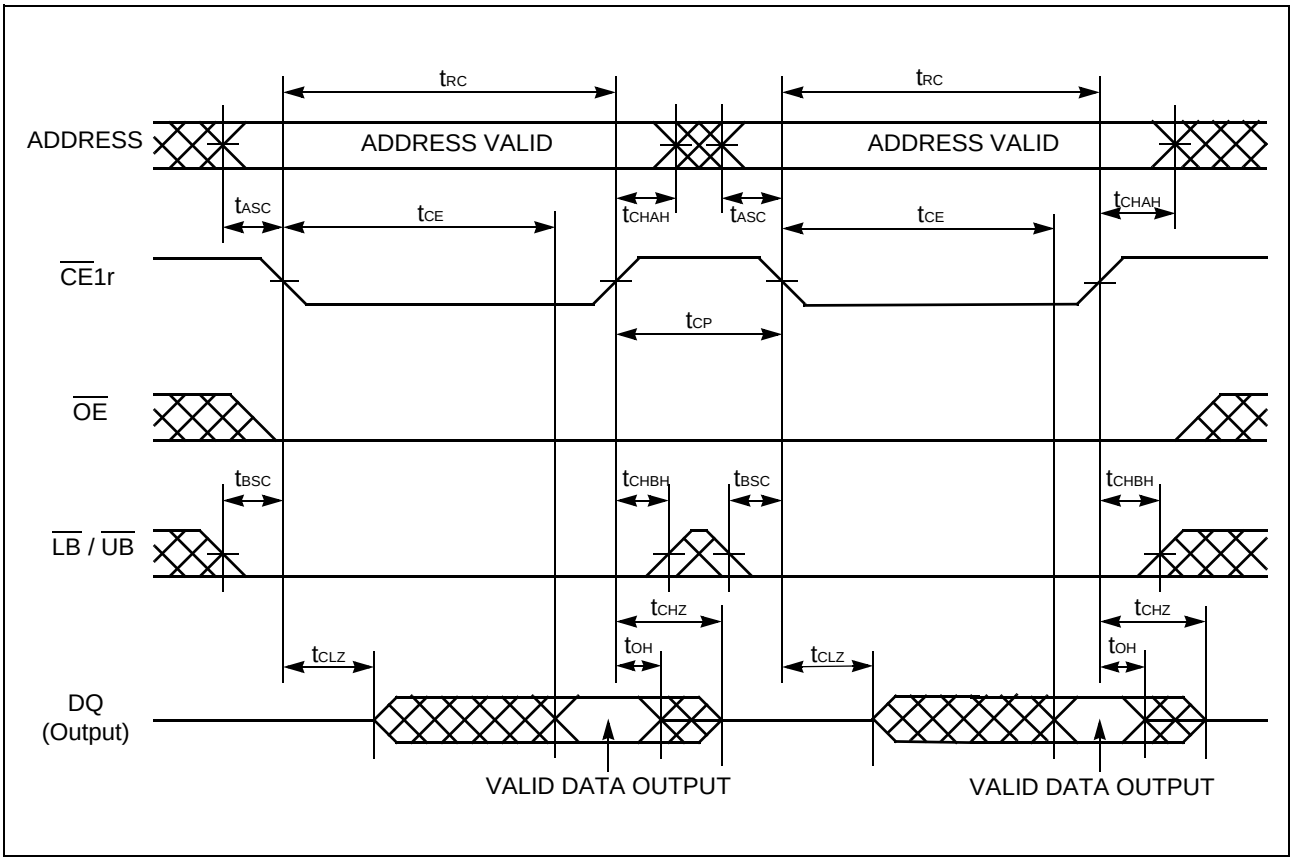
Symbol	Description	Test Setup	Value	Unit	Note
V_{IH}	Input High Level	V_{CC}r = 2.7V to 3.1V	2.3	V	
V_{IL}	Input Low Level	V_{CC}r = 2.7V to 3.1V	0.4	V	
V_{REF}	Input Timing Measurement Level	V_{CC}r = 2.7V to 3.1V	1.3	V	
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns	

- **READ Timing #1 ($\overline{OE}$ Control Access) (FCRAM)**



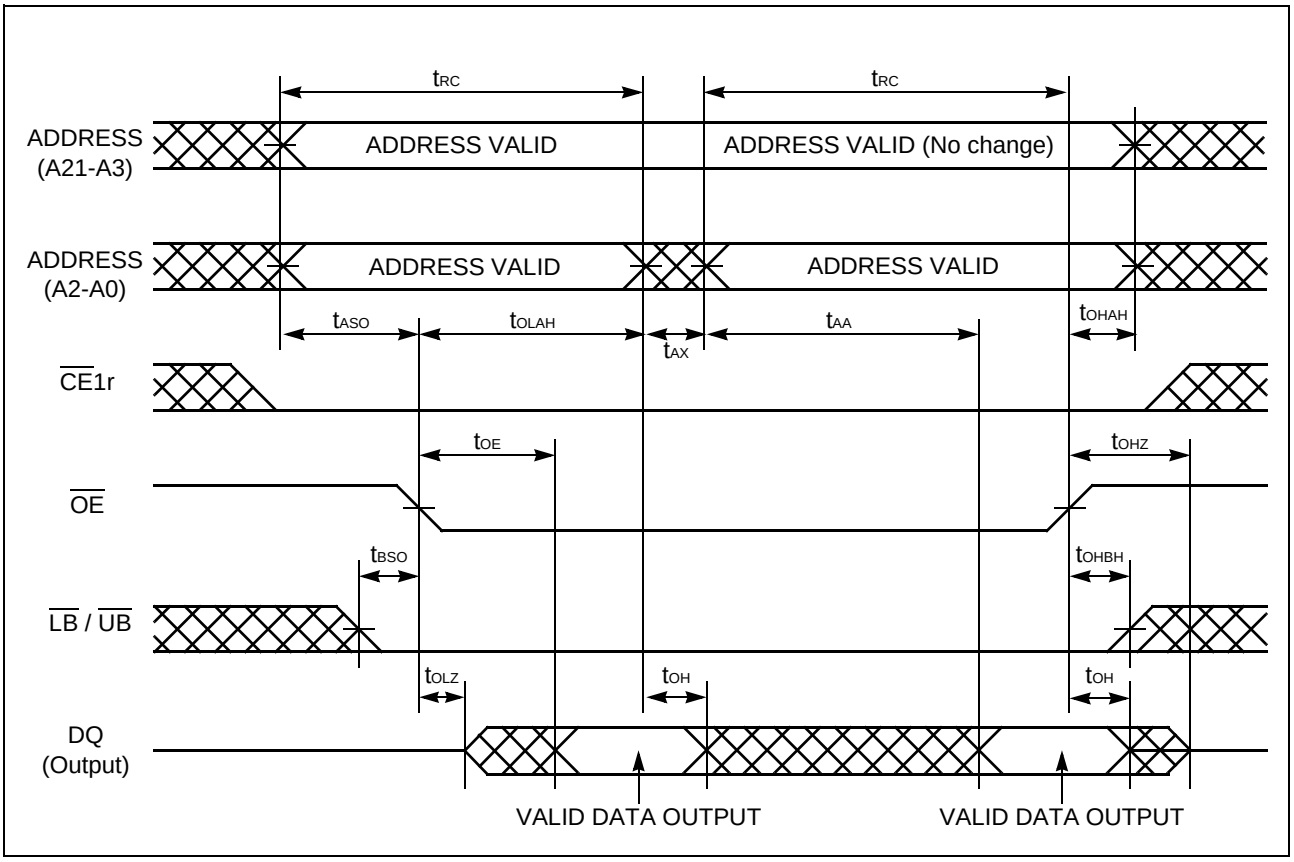
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High for entire read cycle.
Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE1r}$ and $\overline{OE}$ are Low.

- **READ Timing #2 ($\overline{CE}$1r Control Access) (FCRAM)**



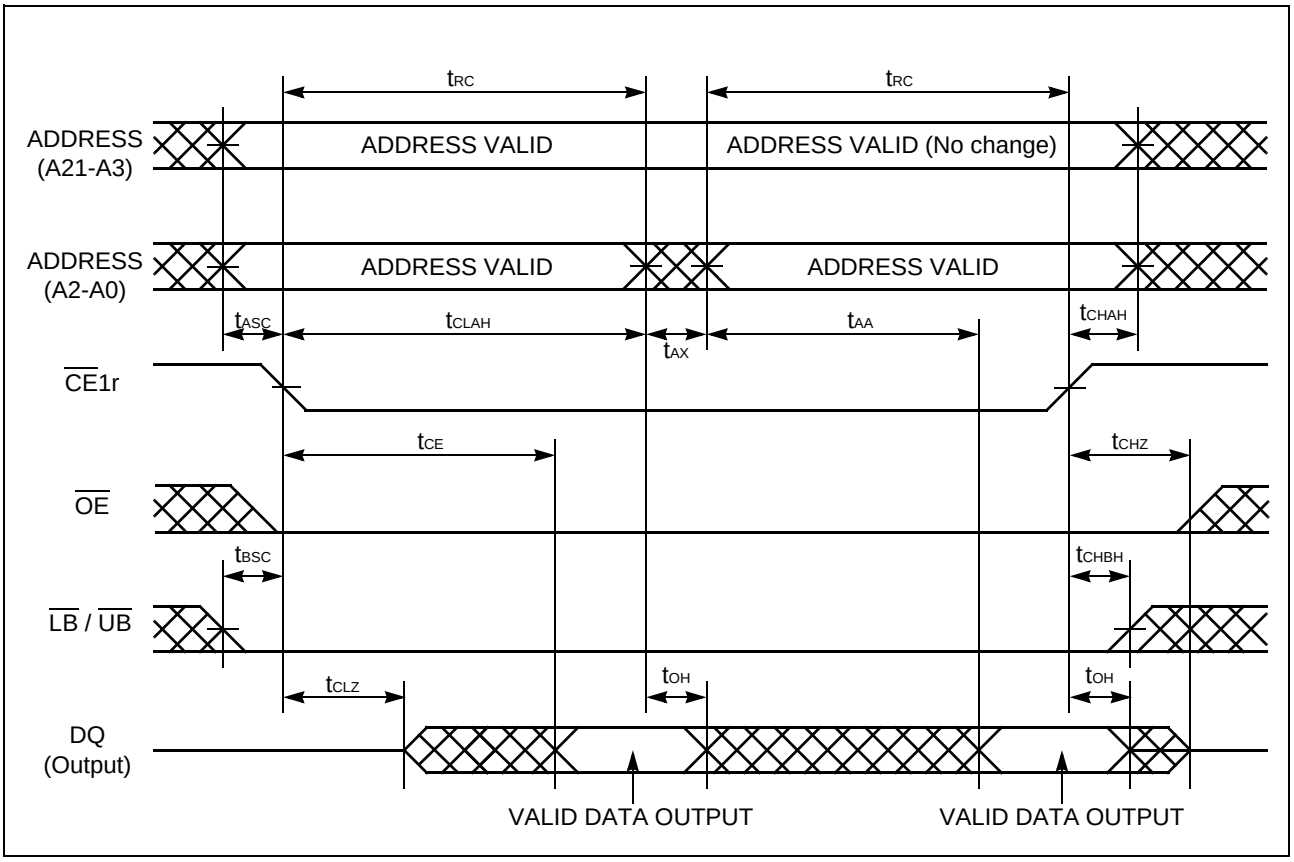
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High for entire read cycle.
Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

- **READ Timing #3 (Address Access after $\overline{OE}$ Control Access) (FCRAM)**



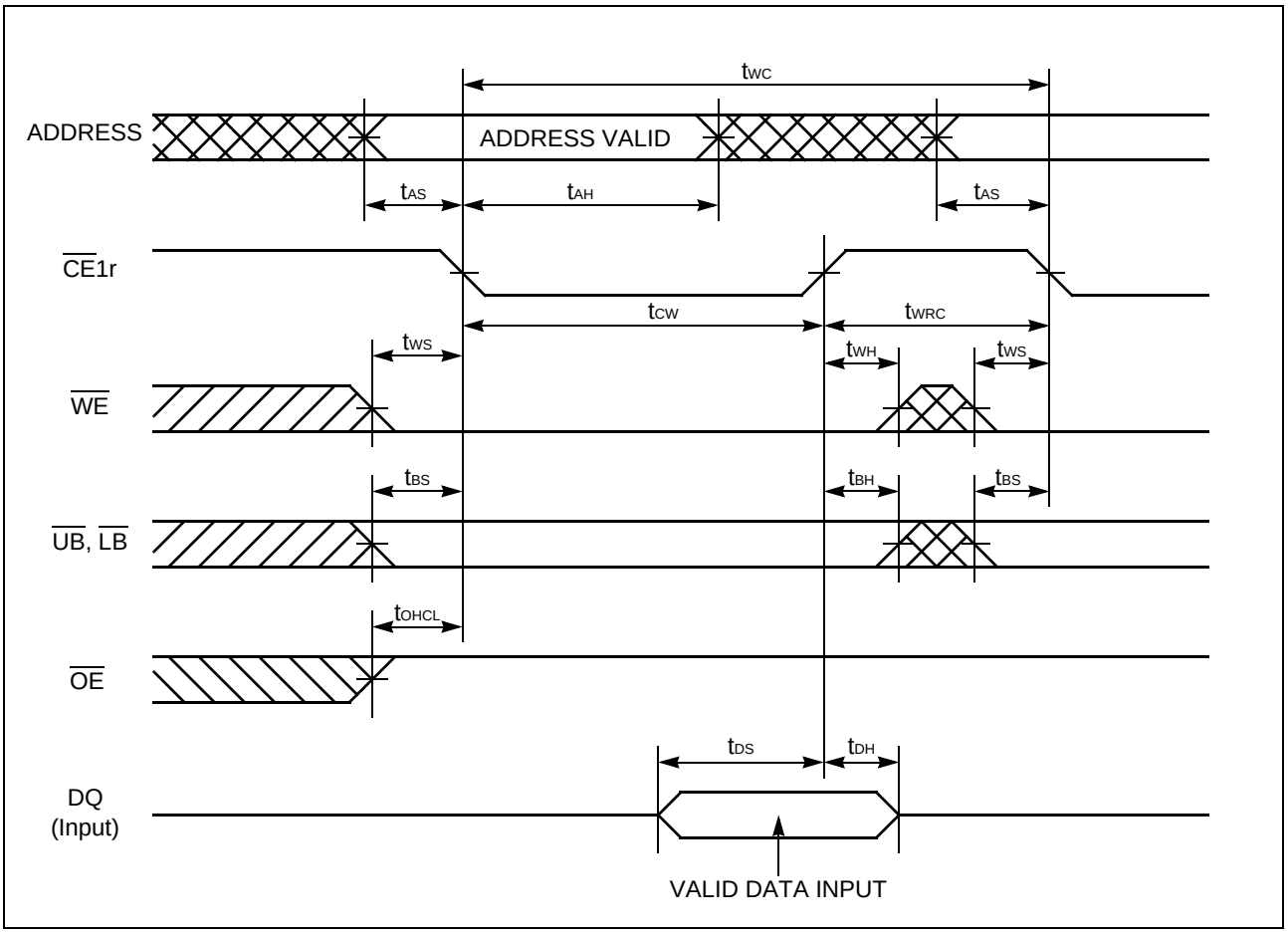
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High for entire read cycle.
Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE1r}$ and $\overline{OE}$ are Low.

- **READ Timing #4 (Address Access after $\overline{CE}$1r Control Access) (FCRAM)**



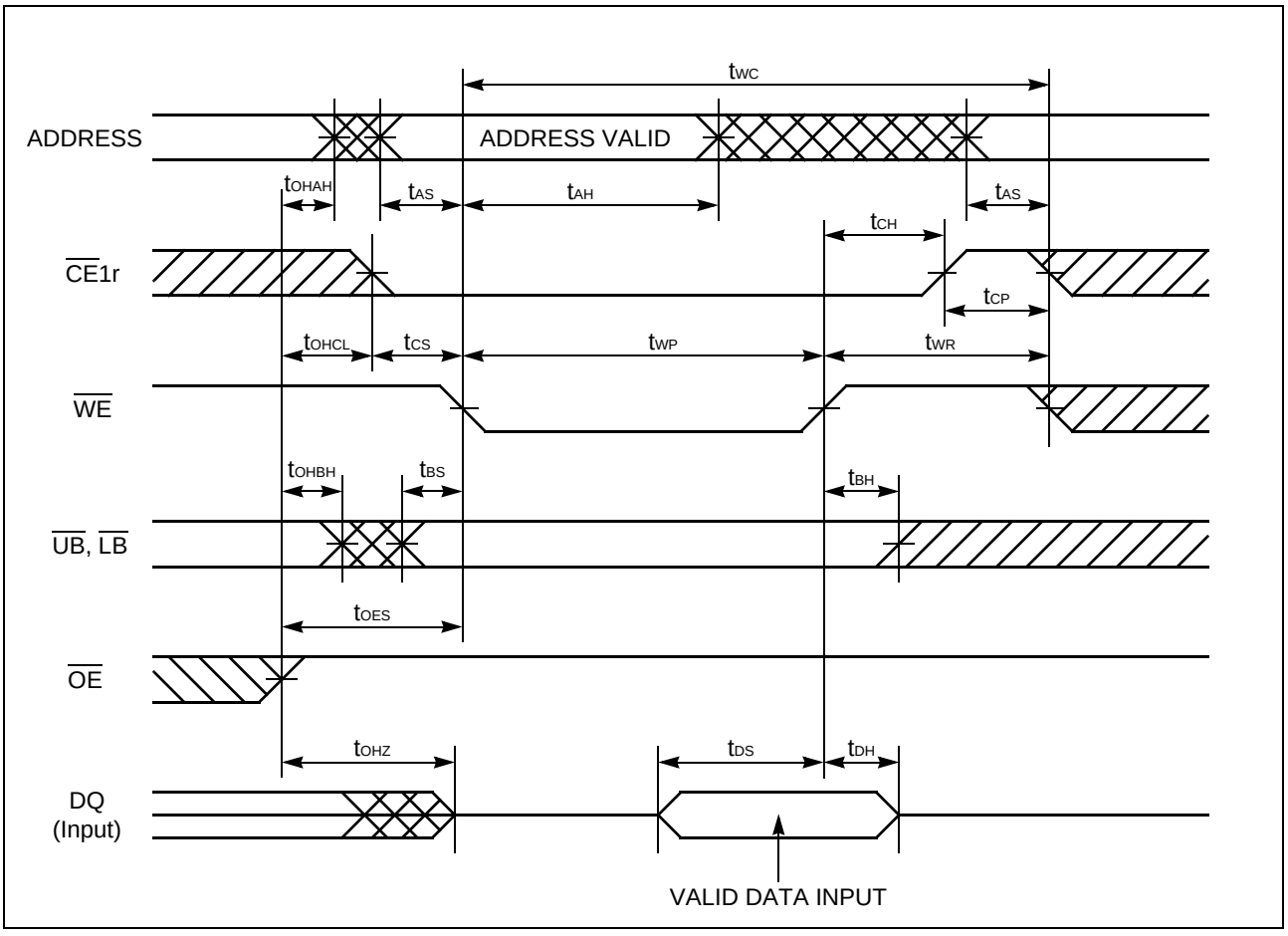
Note: CE2r, $\overline{PE}$ and $\overline{WE}$ must be High for entire read cycle.
Either or both $\overline{LB}$ and $\overline{UB}$ must be Low when both $\overline{CE}$1r and $\overline{OE}$ are Low.

- **WRITE Timing #1 ($\overline{CE}$1r Control) (FCRAM)**



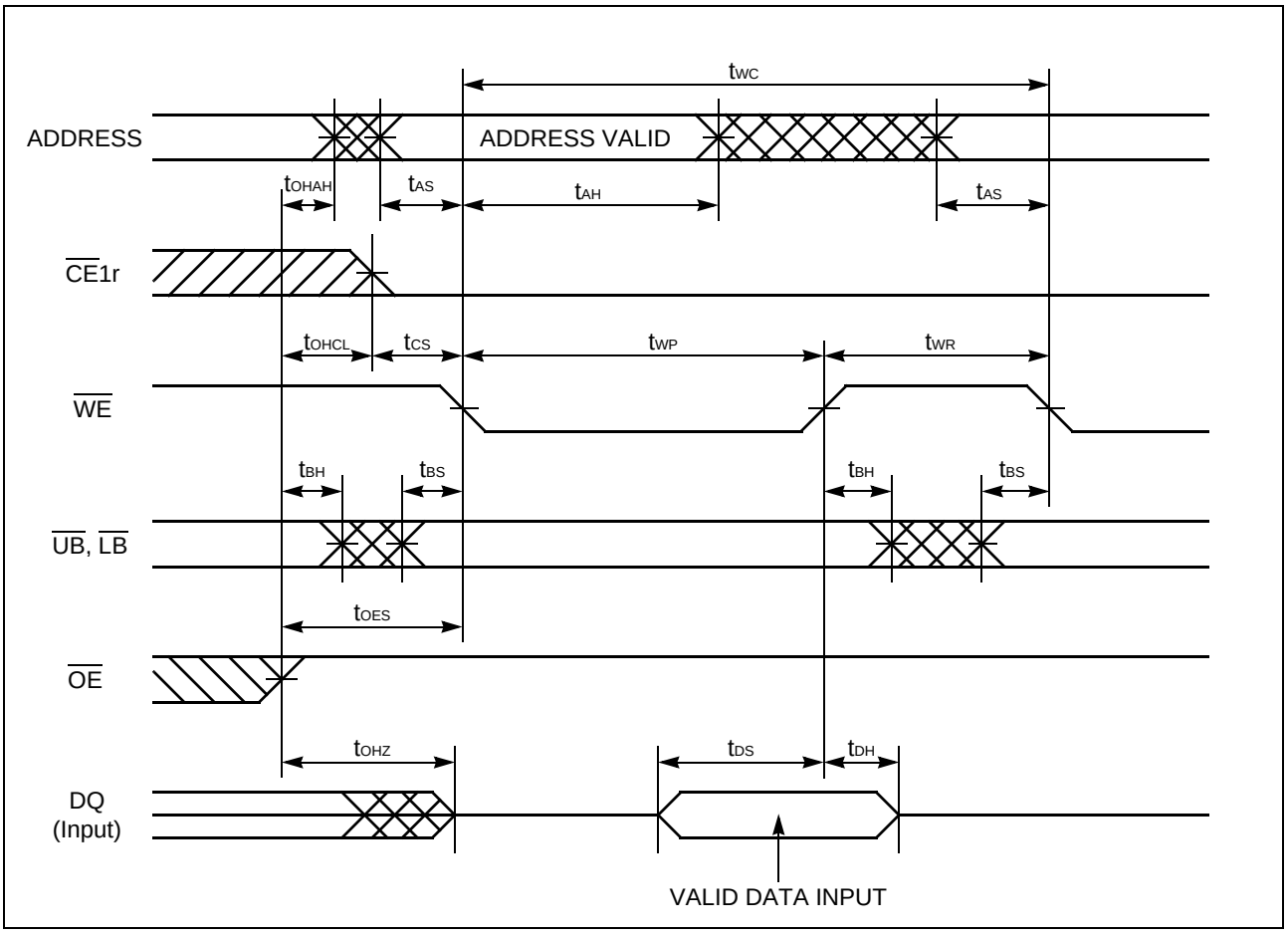
Note: CE2r and $\overline{PE}$ must be High for write cycle.

- **WRITE Timing #2-1 ($\overline{WE}$ Control,Single Write Operetion) (FCRAM)**



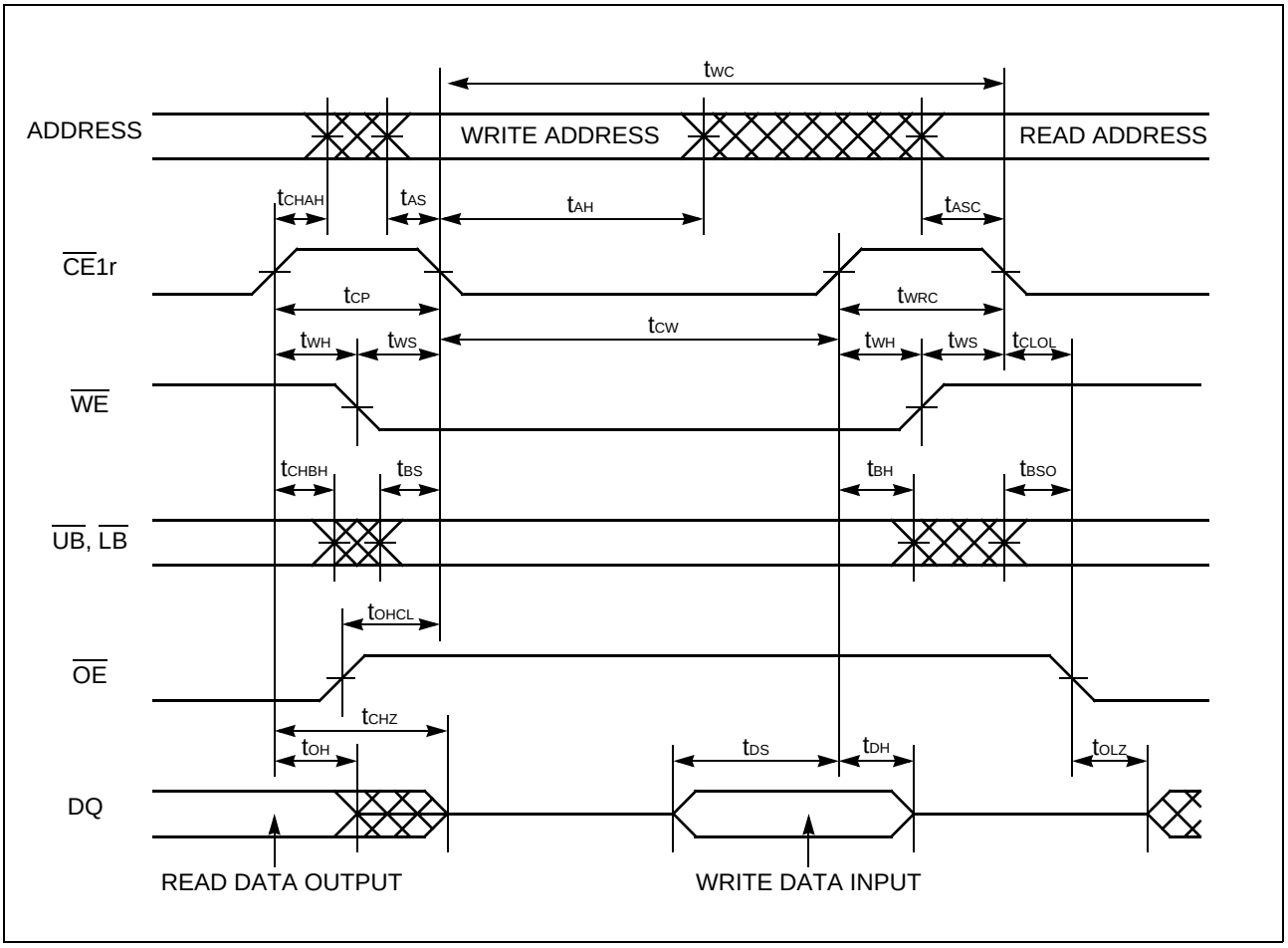
Note: CE2r and $\overline{PE}$ must be High for write cycle.

- **WRITE Timing #2-2 ($\overline{WE}$ Control,Continuous Write Operetion) (FCRAM)**



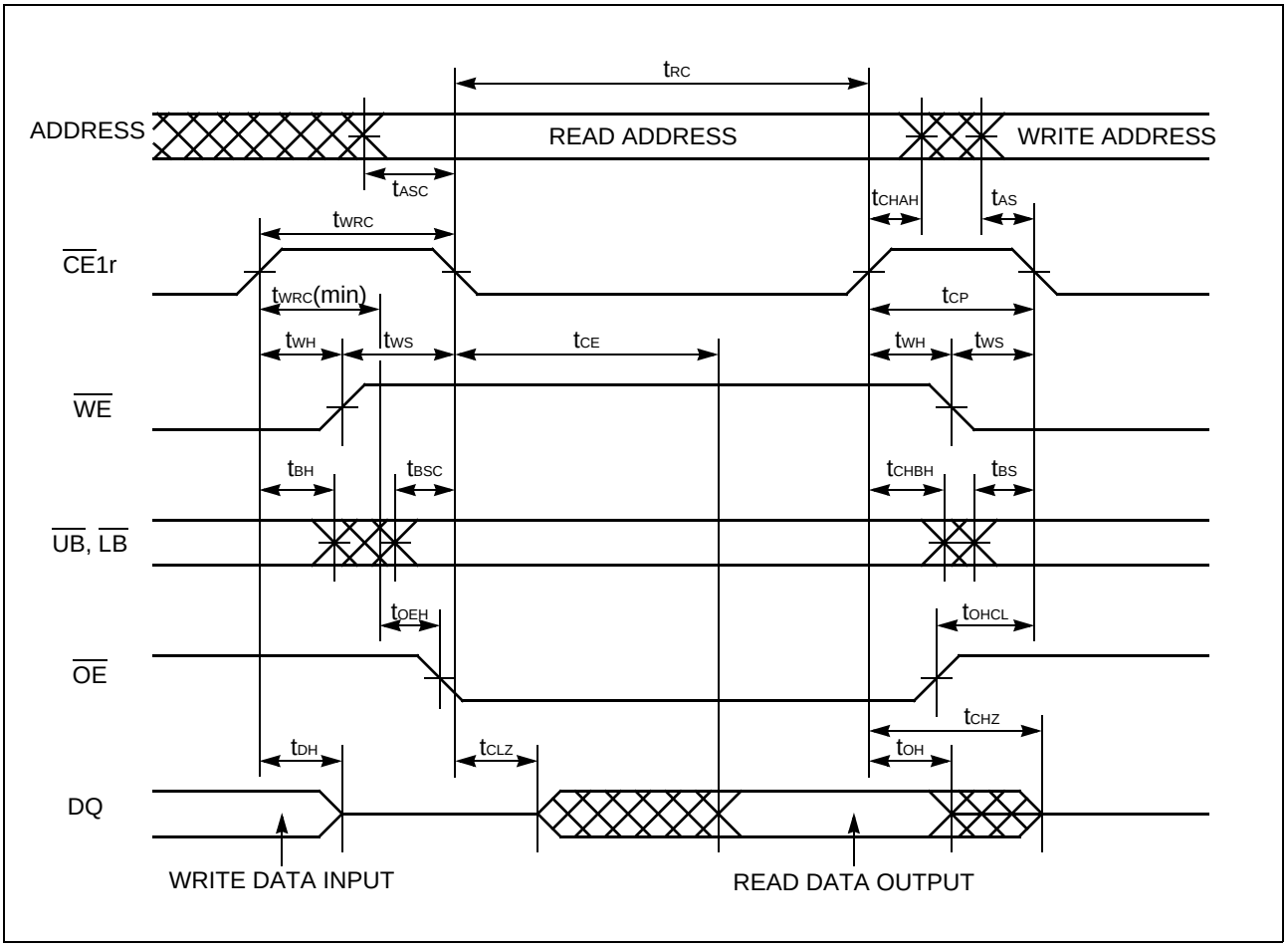
Note: CE2r and $\overline{PE}$ must be High for write cycle.

- **READ / WRITE Timing #1-1 ($\overline{CE}$1r Control) (FCRAM)**



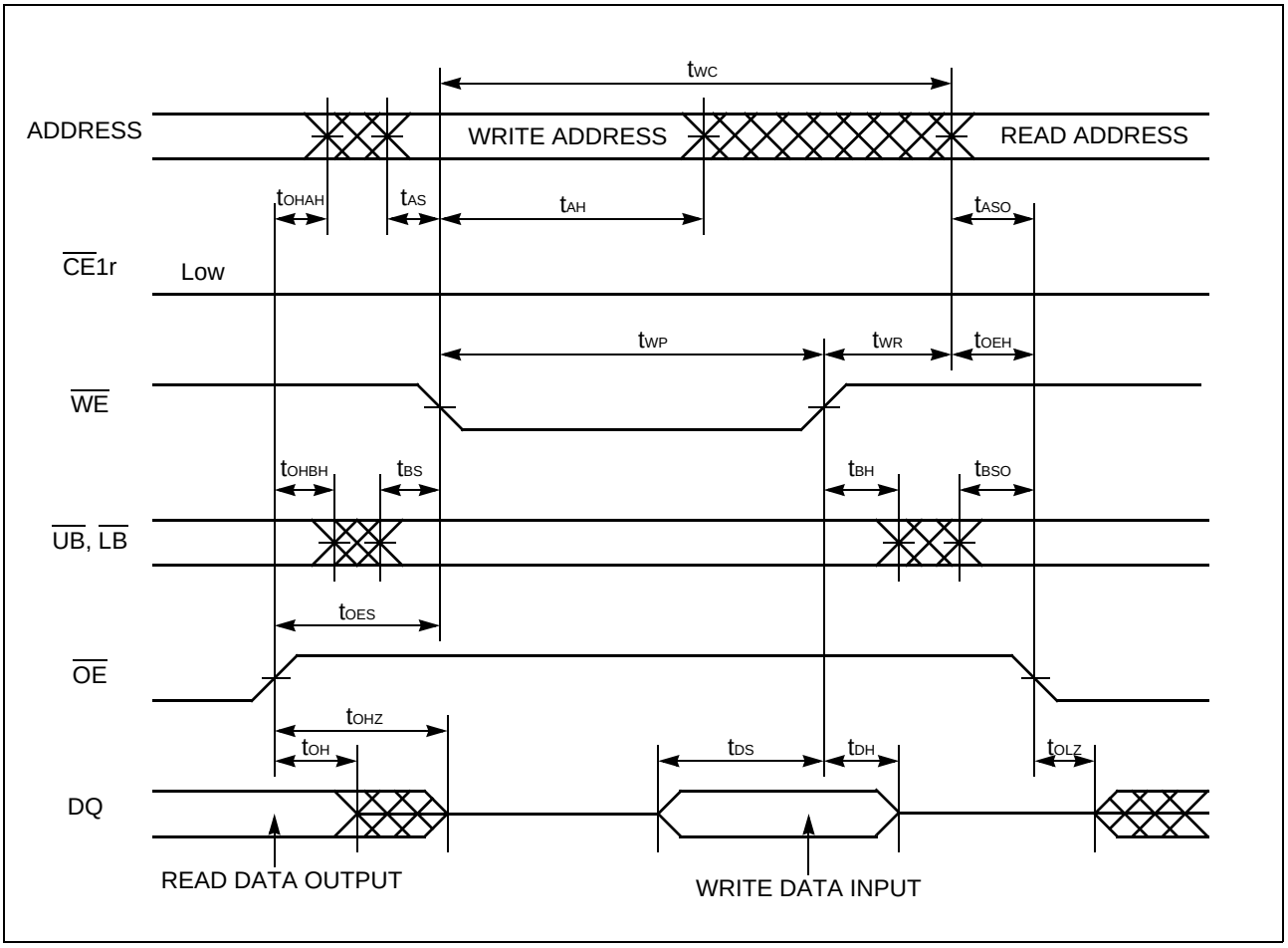
Note: Write address is valid from either $\overline{CE}$1r or $\overline{WE}$ of last falling edge.

- **READ / WRITE Timing #1-2 ($\overline{CE}$1r Control) (FCRAM)**



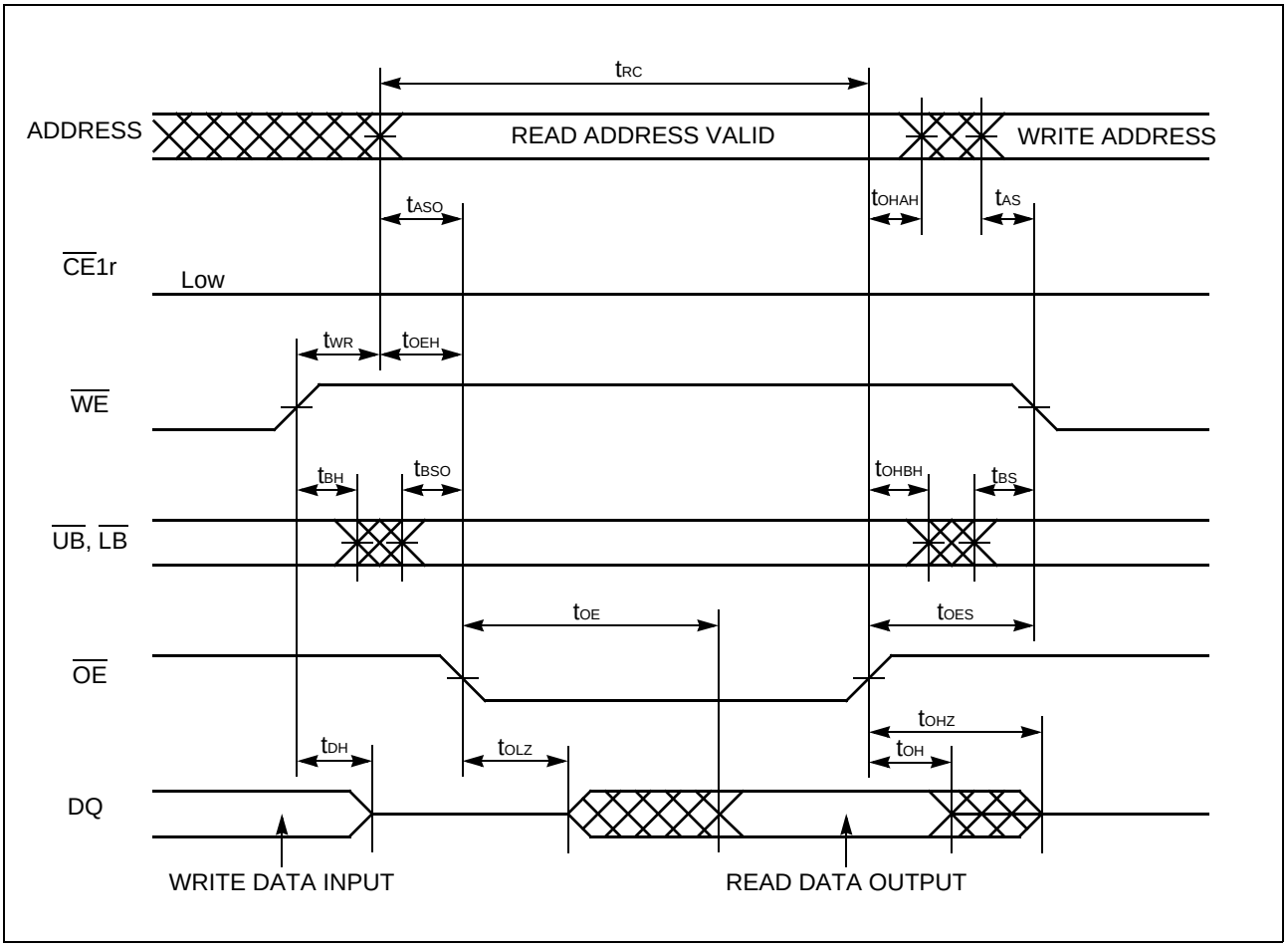
Note: The t_{OEH} is specified from the time satisfied both t_{WRC} and t_{WR}(min).

- **READ($\overline{OE}$ Control) / WRITE($\overline{WE}$ Control) Timing #2-1 (FCRAM)**



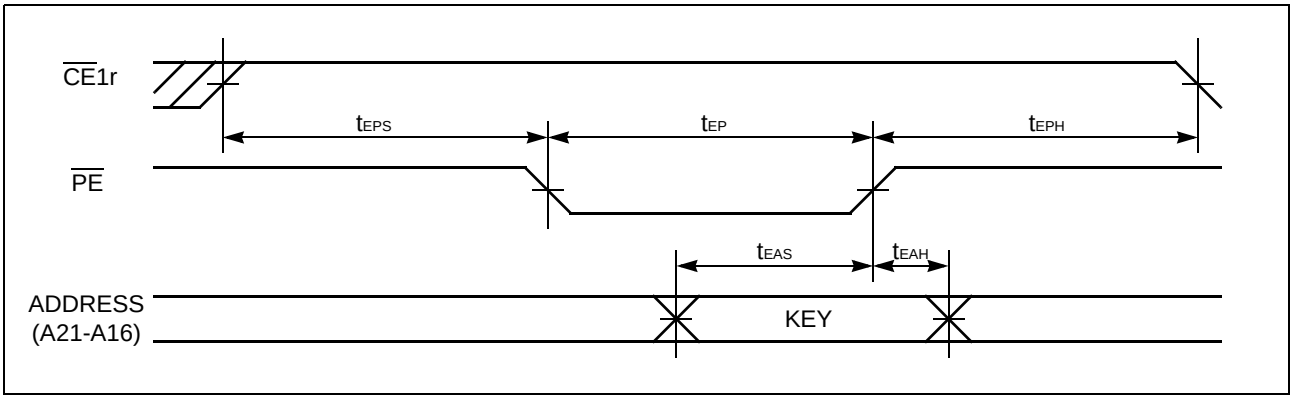
Note: $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}$1r is tied to Low, output is exclusively controlled by $\overline{OE}$.

- **READ($\overline{OE}$ Control) / WRITE($\overline{WE}$ Control) Timing #2-2**



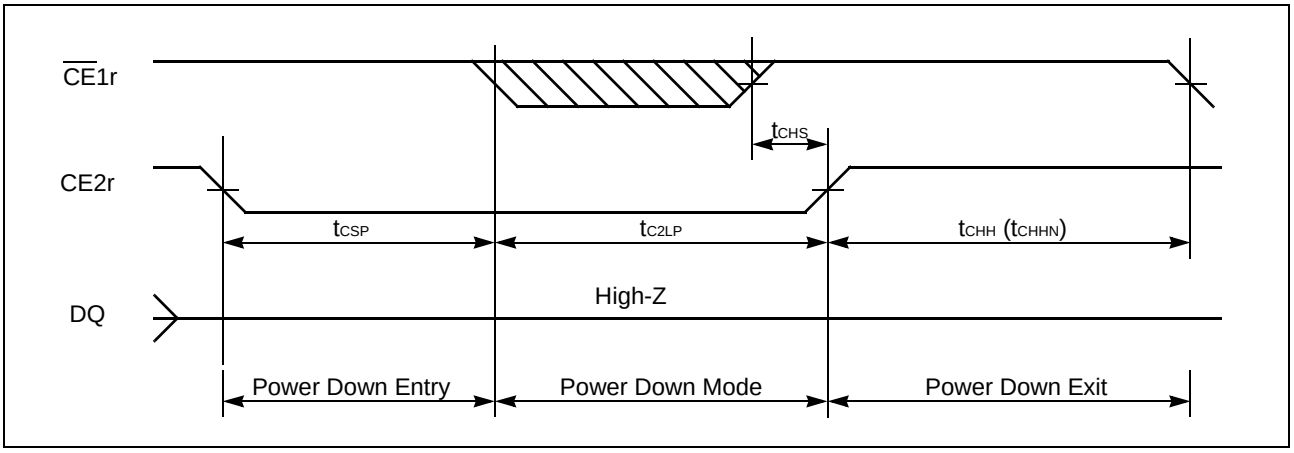
Note: $\overline{CE}$1r can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}$1r is tied to Low, output is exclusively controlled by $\overline{OE}$.

- **POWER DOWN PROGRAM Timing (FCRAM)**



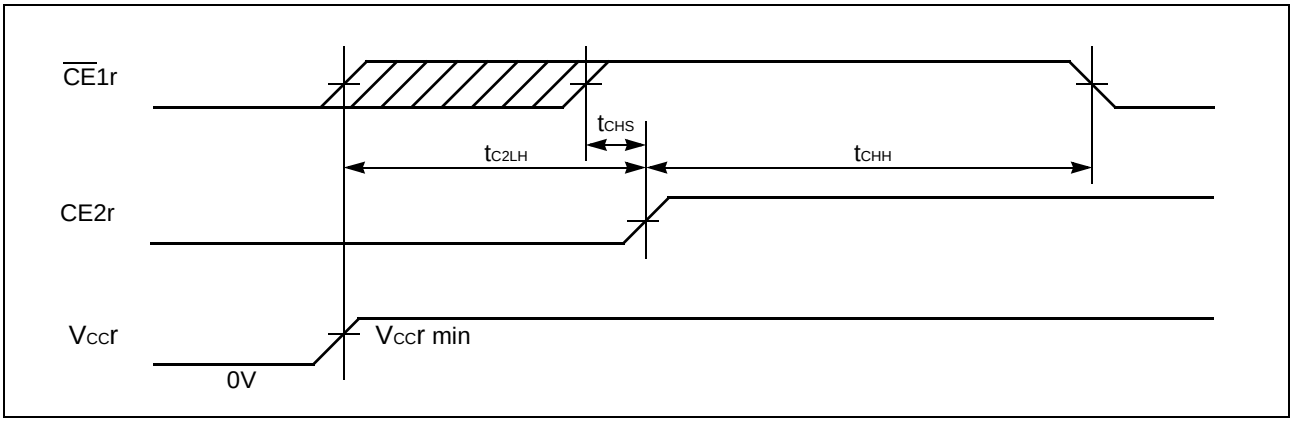
Note: CE2r must be High for Power Down Programming.
Any other inputs not specified above can be either High or Low.

- **POWER DOWN Entry and Exit Timing (FCRAM)**



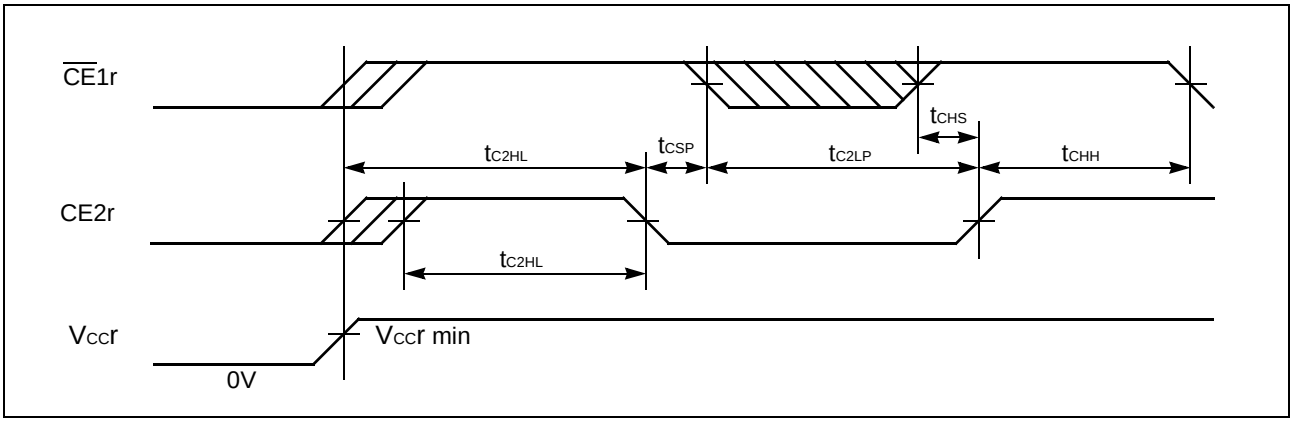
Note: This Power Down mode can be also used for Power-up #2 below except that t_{CHHN} can not be used at Power-up timing.

- **POWER-UP Timing #1 (FCRAM)**



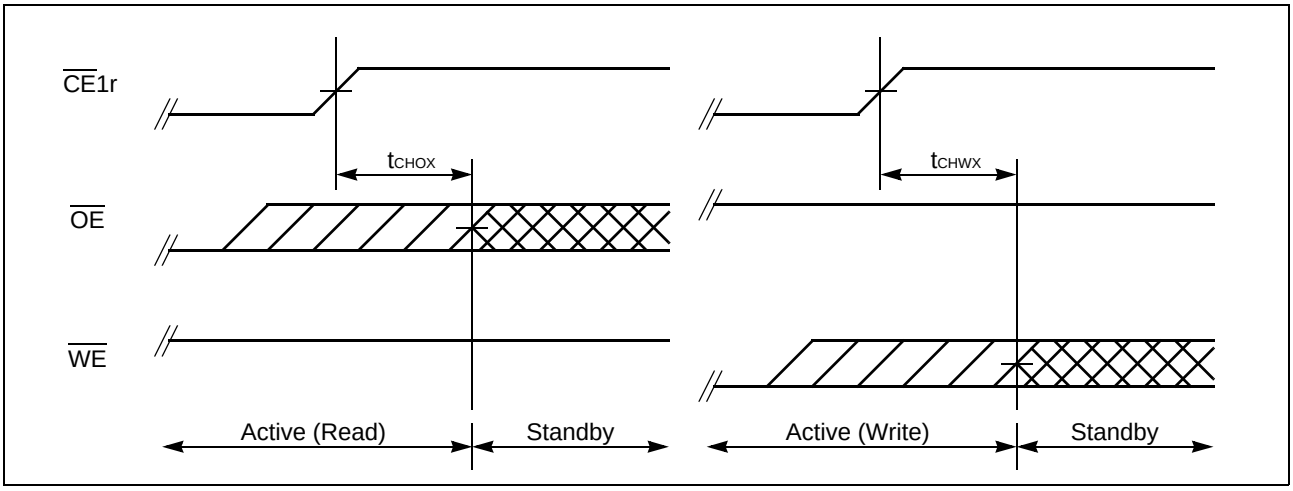
Note: The t_{C2LH} specifies after $V_{CC}r$ reaches specified minimum level.

- **POWER-UP Timing #2 (FCRAM)**



Note: The t_{C2HL} specifies from CE2r Low to High transition after $V_{CC}r$ reaches specified minimum level.
$\overline{CE}$1r must be brought to High prior to or together with CE2r Low to High transition.

- **Standby Entry Timing after Read or Write (FCRAM)**



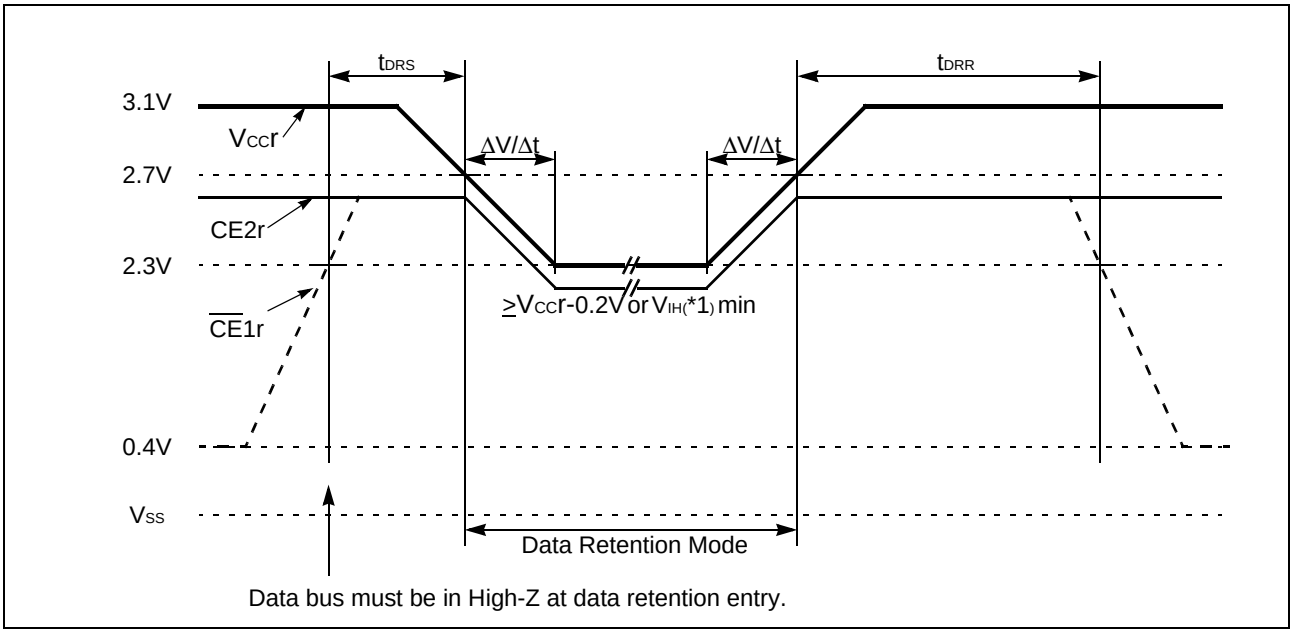
Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period from either last address transition of A0 and A1, or $\overline{CE}$1r Low to High transition.

■ DATA RETENTION Low $V_{CC}r$ Characteristics (FCRAM)

Parameter	Symbol	Test Conditions	Value		Unit
			Min.	Max.	
$V_{CC}r$ Data Retention Supply Voltage	V_{DR}	$\overline{CE}1r = CE2r \geq V_{CC}r - 0.2V$ or, $\overline{CE}1r = CE2r = V_{IH}$,	2.3	3.1	V
$V_{CC}r$ Data Retention Supply Current	I_{DR}	2.3V ≤ $V_{CC}r$ ≤ 2.7V, $V_{IN} = V_{IH}$(*1) or V_{IL} $\overline{CE}1r = CE2r = V_{IH}$(*1), I_{OUT}=0mA	—	1.5	mA
	I_{DR1}	2.3V ≤ $V_{CC}r$ ≤ 2.7V, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}r - 0.2V$, $\overline{CE}1r = CE2r \geq V_{CC}r - 0.2V$, I_{OUT}=0mA	—	150	µA
Data Retention Setup Time	t_{DRS}	2.7V ≤ $V_{CC}r$ ≤ 3.1V at data retention entry	0	—	ns
Data Retention Recovery Time	t_{DRR}	2.7V ≤ $V_{CC}r$ ≤ 3.1V after data retention	200	—	ns
$V_{CC}r$ Voltage Transition Time	ΔV/Δt		0.2	—	V/µs

Notes: *1: $2.0 \leq V_{IH} \leq V_{CC}r+0.3V$

- **Data Retention Timing**



■ ELECTRICAL CHARACTERISTICS (AC Characteristics)

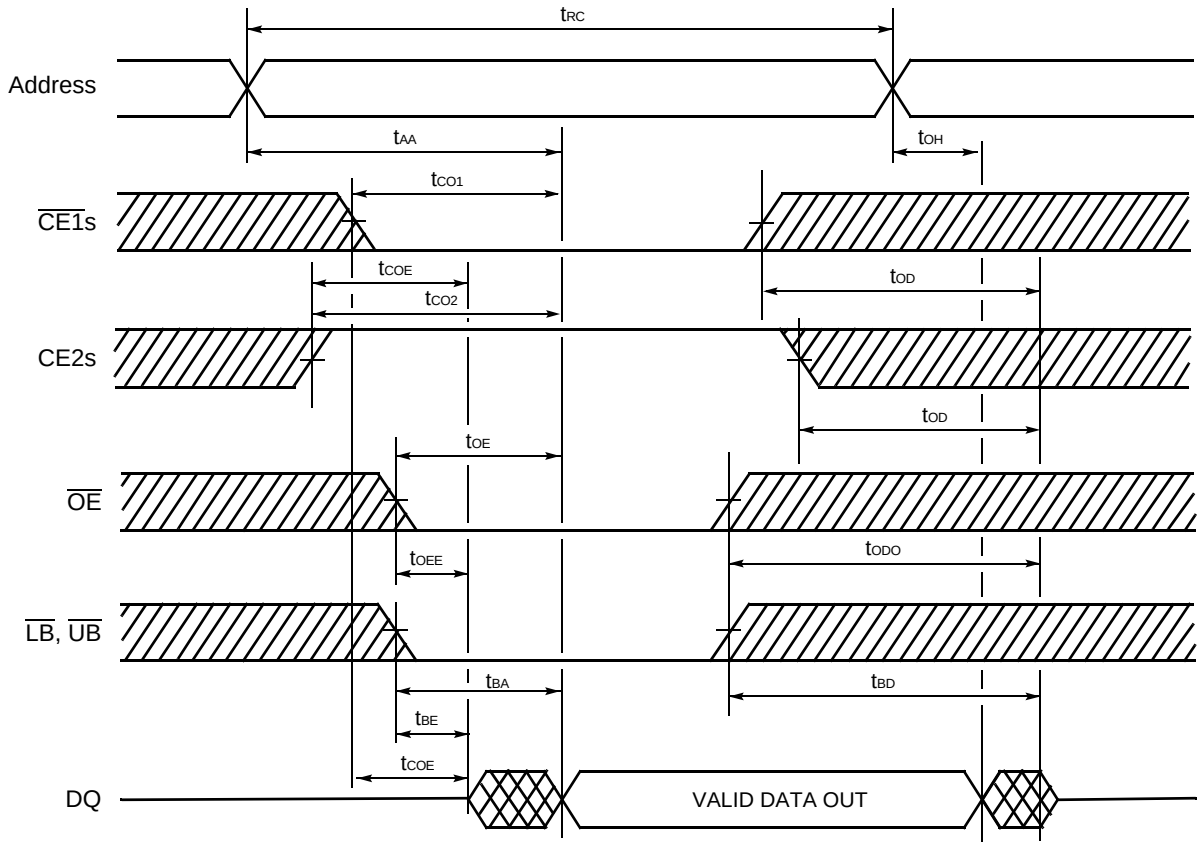
- **Read Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	70	—	ns
Address Access Time	t_{AA}	—	70	ns
Chip Enable ($\overline{CE1}$s) Access Time	t_{CO1}	—	70	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	70	ns
Output Enable Access Time	t_{OE}	—	35	ns
$\overline{LB}$, $\overline{UB}$ to Output Valid	t_{BA}	—	70	ns
Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Enable Low to Output Active	t_{BE}	0	—	ns
Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z	t_{OD}	—	25	ns
Output Enable High to Output High-Z	t_{ODO}	—	25	ns
$\overline{LB}$, $\overline{UB}$ Output Enable to Output High-Z	t_{BD}	—	25	ns
Output Data Hold Time	t_{OH}	10	—	ns

Note: Test Conditions–Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 0.5 × V_{CC}s
Output: 0.5 × V_{CC}s

8M SRAM for MCP

- **Read Cycle (SRAM)**

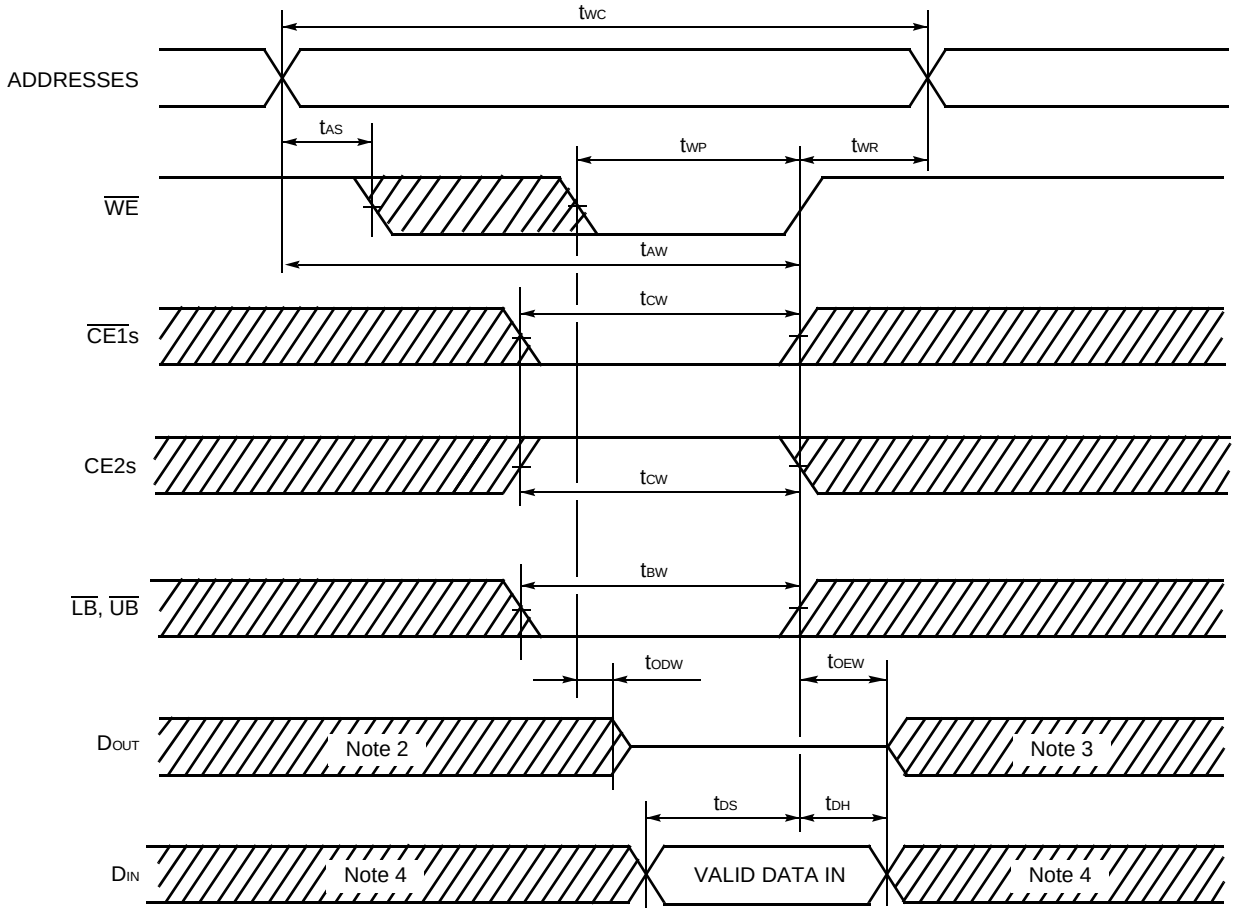


Note: $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

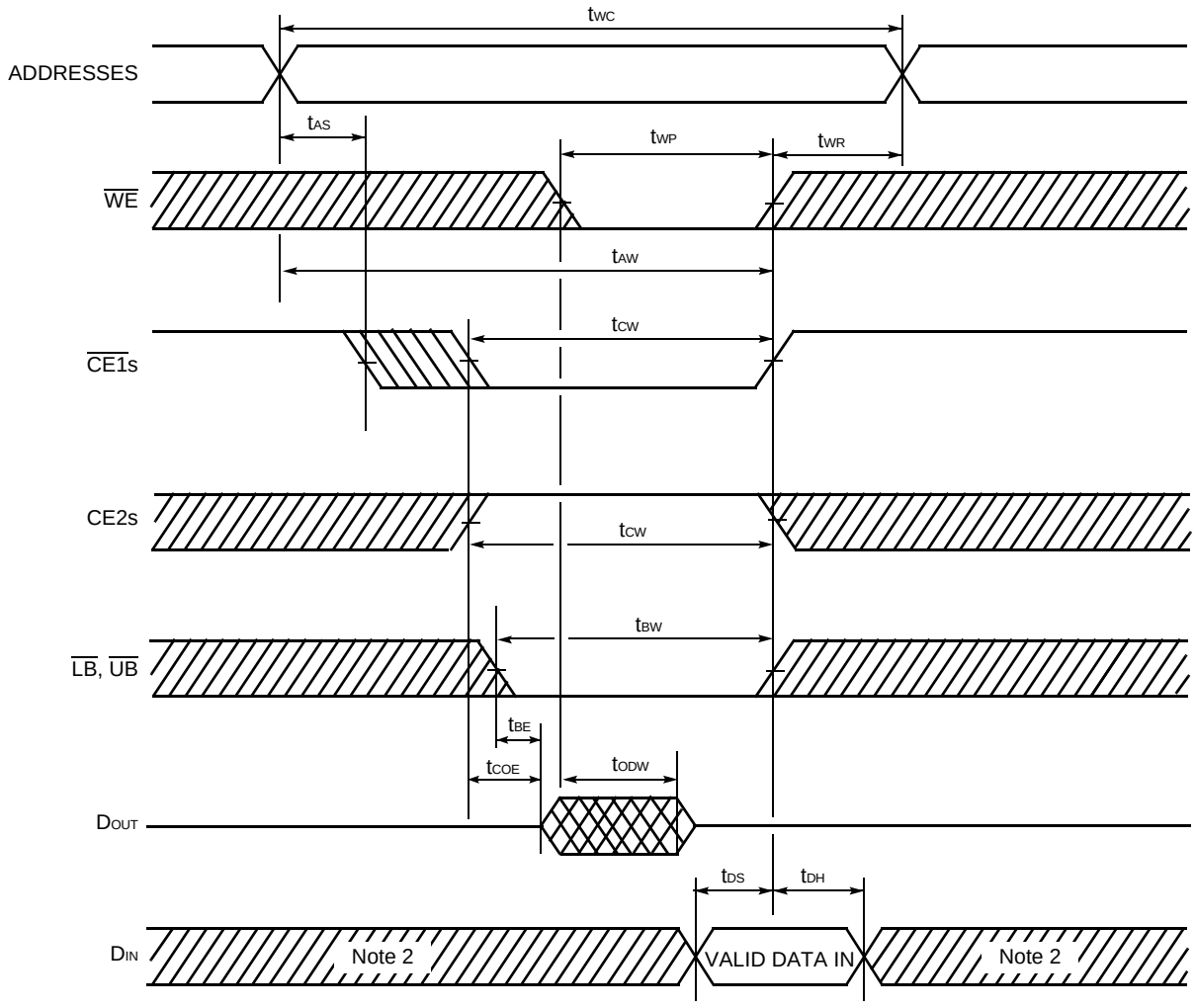
Parameter	Symbol	Value		Unit
		Min.	Max.	
Write Cycle Time	t_{WC}	70	—	ns
Write Pulse Width	t_{WP}	50	—	ns
Chip Enable to End of Write	t_{CW}	55	—	ns
Address valid to End of Write	t_{AW}	55	—	ns
$\overline{LB}$, $\overline{UB}$ to End of Write	t_{BW}	55	—	ns
Address Setup Time	t_{AS}	0	—	ns
Write Recovery Time	t_{WR}	0	—	ns
$\overline{WE}$ Low to Output High-Z	t_{ODW}	—	25	ns
$\overline{WE}$ High to Output Active	t_{OEW}	0	—	ns
Data Setup Time	t_{DS}	30	—	ns
Data Hold Time	t_{DH}	0	—	ns

- **Write Cycle (Note 1) ($\overline{WE}$ control) (SRAM)**



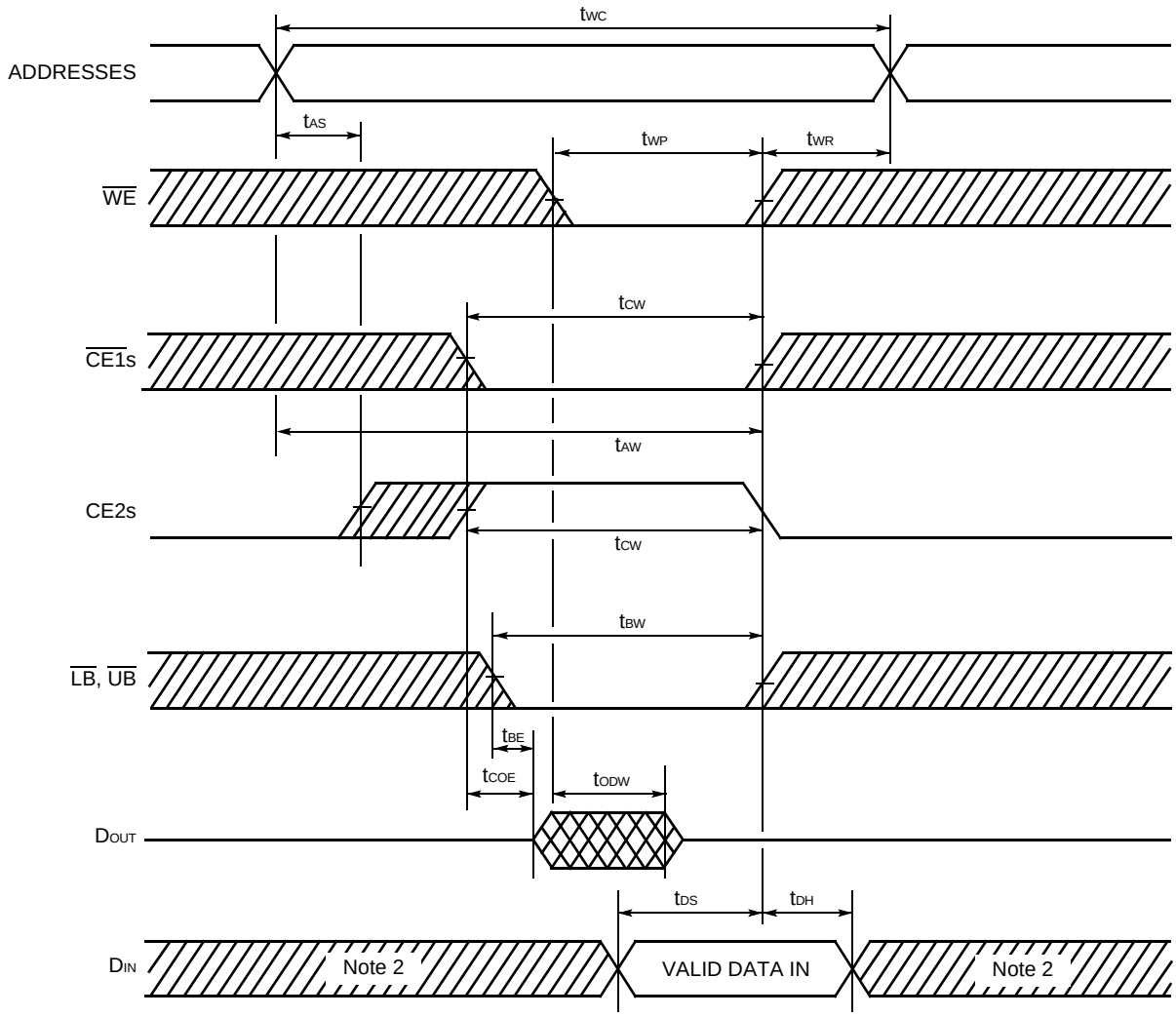
Note 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) ($\overline{CE1}$s control) (SRAM)**



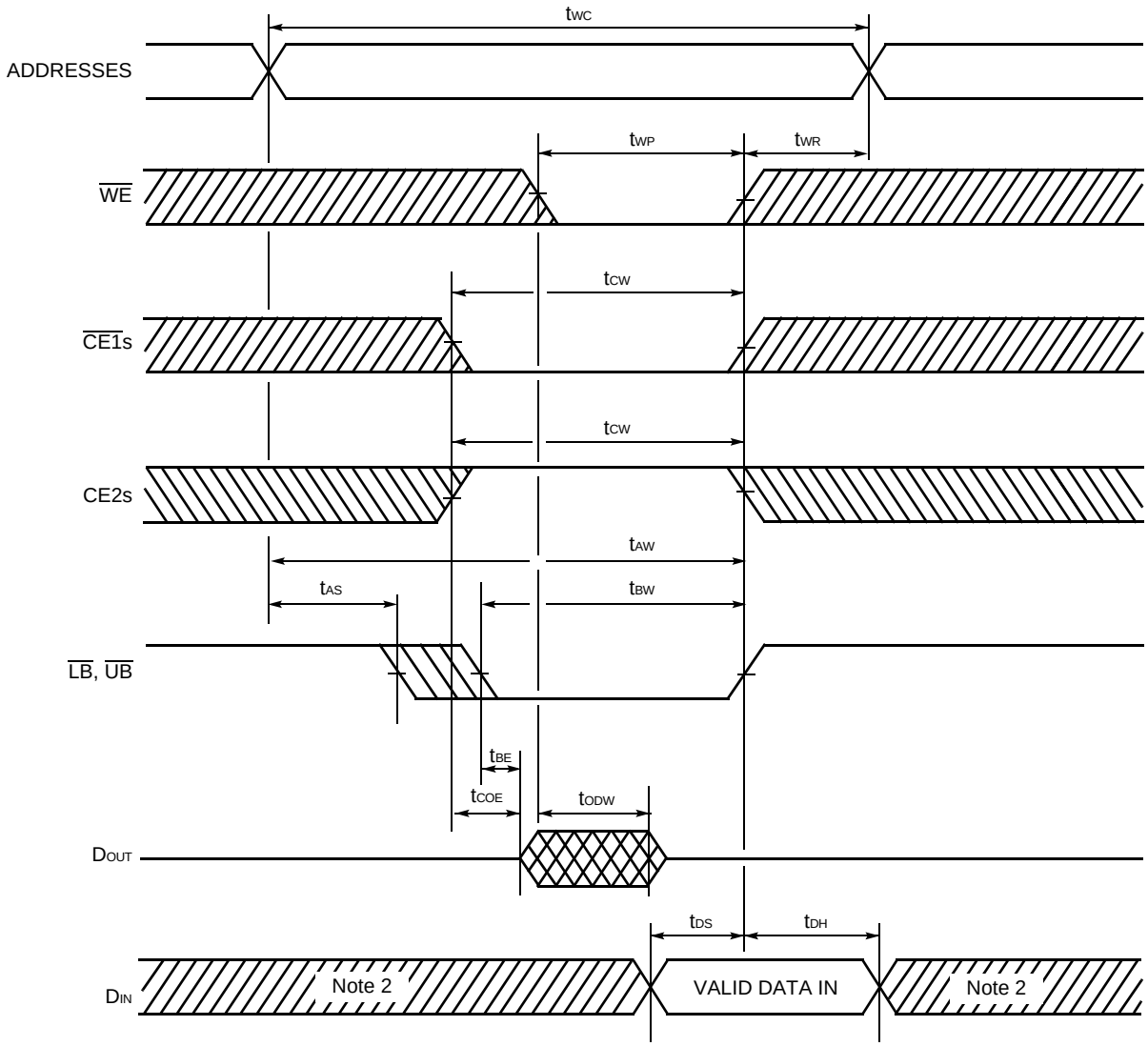
Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) (CE2s Control) (SRAM)**



Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) ($\overline{LB}$, $\overline{UB}$ Control) (SRAM)**



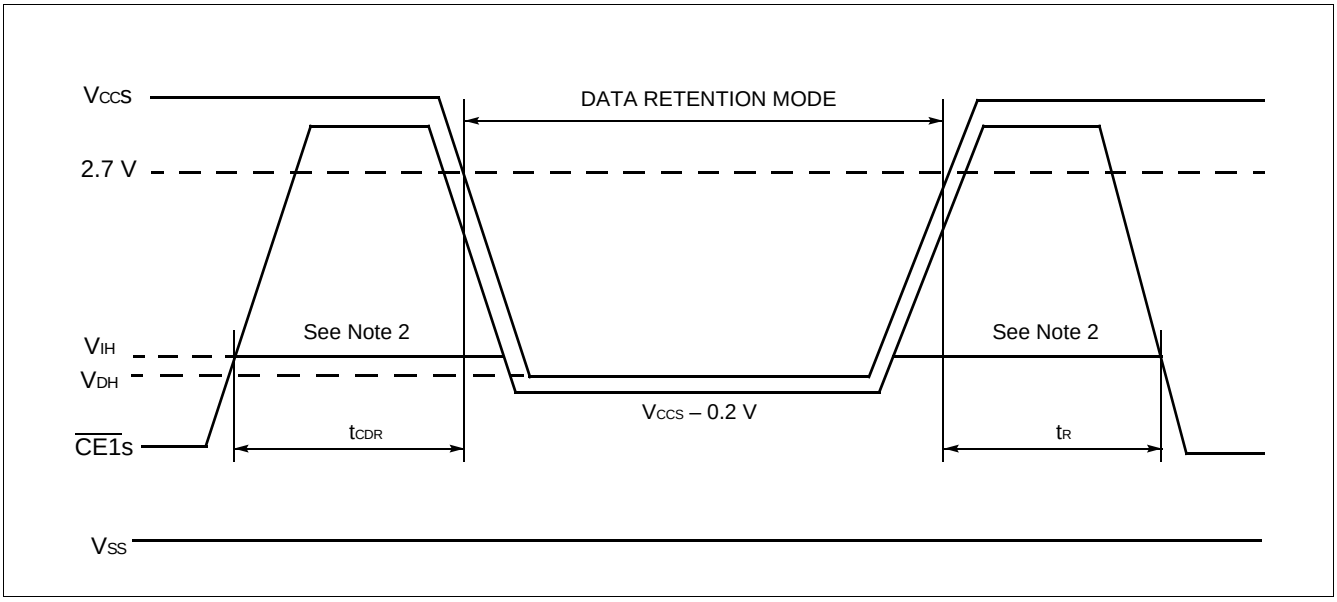
Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

■ DATA RETENTION CHARACTERISTICS (SRAM)

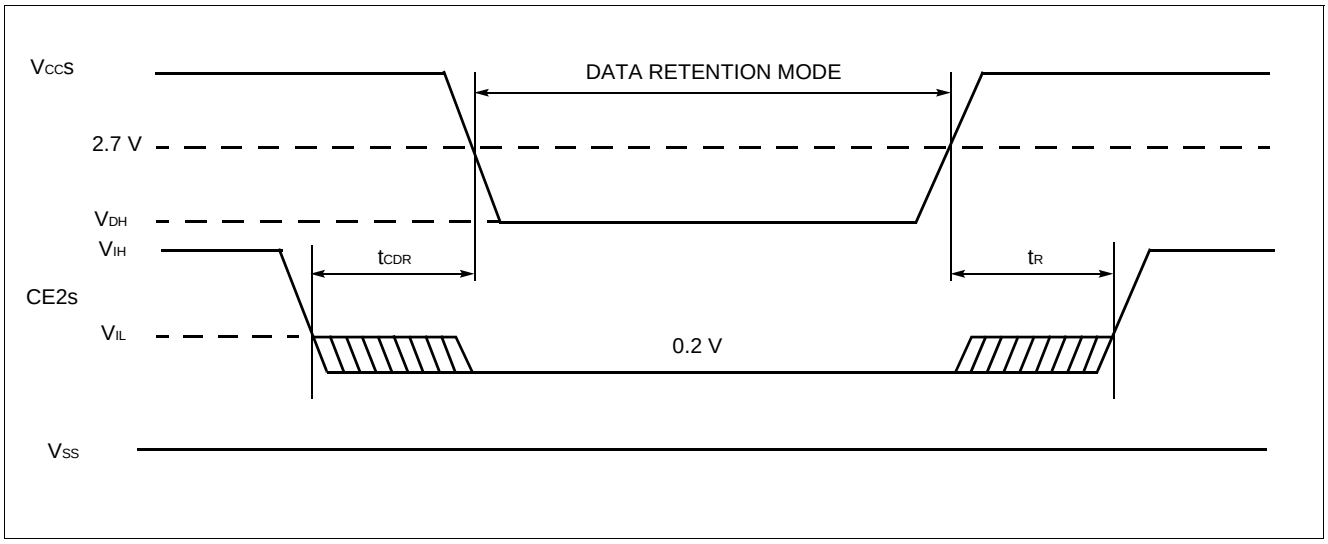
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Data Retention Supply Voltage		V_{DH}	1.5	—	3.1	V
Standby Current	V_{DH} = 3.0 V	I_{DDS2}	—	—	15	µA
Chip Deselect to Data Retention Mode Time		t_{CDR}	0	—	—	ns
Recovery Time		t_R	t_{RC}	—	—	ns

Note t_{RC}: Read cycle time

- **$\overline{CE1}$s Controlled Data Retention Mode (Note 1)**



- **CE2s Controlled Data Retention Mode (Note 3)**



Notes: 1. In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to V_{CC}S–0.2 V or V_{SS} to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to V_{CC}S+0.3 V.

2. When $\overline{CE1}$s is operating at the V_{IH} Min. level, the standby current is given by I_{SB1}s during the transition of V_{CC}s from Vccs MAX to V_{IH} Min. level.
3. In CE2s controlled data retention mode, input and input/output pins can be used between –0.3 V to Vccs+0.3V.

■ PIN CAPACITANCE

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{IN}	V_{IN} = 0	—	—	T.B.D.	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	—	—	T.B.D.	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	—	—	T.B.D.	pF

Note: Test conditions Ta = 25°C, f = 1.0 MHz

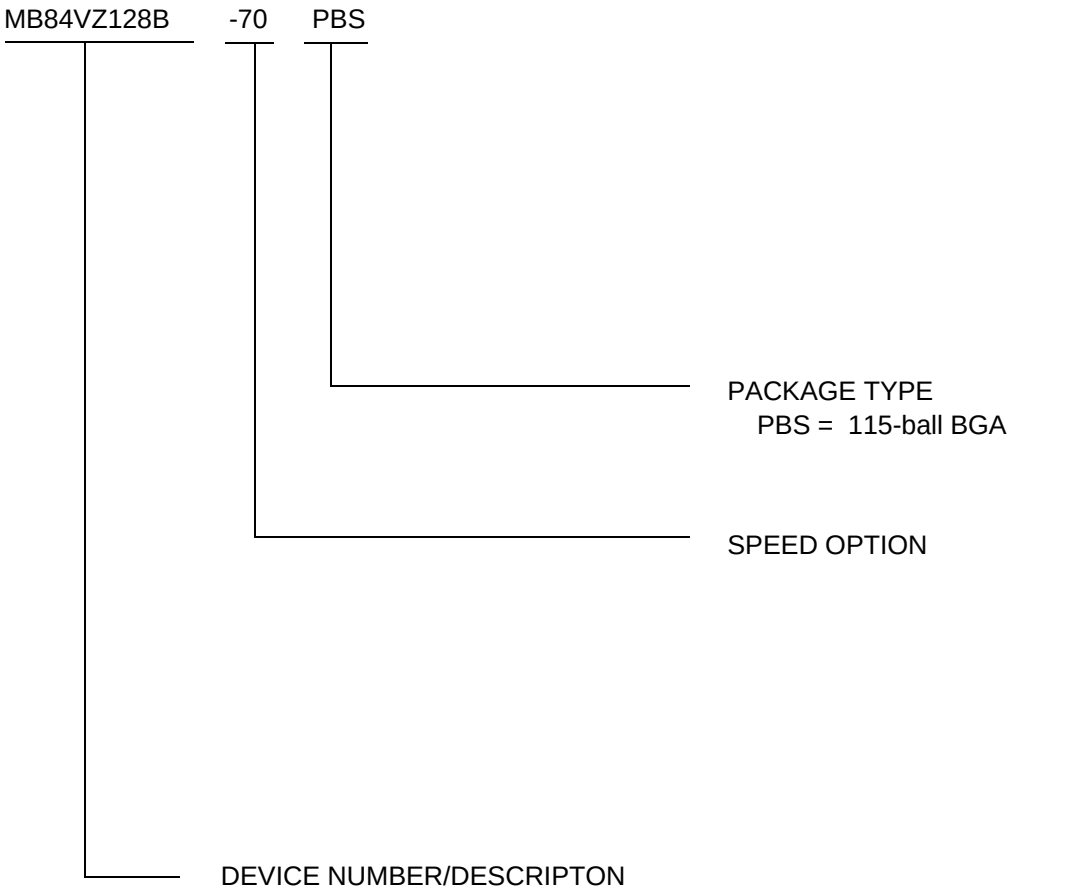
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2. Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2.
- Without the high voltage (V_{ID}) , sector group protection can be achieved by using “Extended Sector Group Protection” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

115-pin plastic FBGA
(BGA-115P-Mxx)

NOW PRINTING

Dimensions in mm (inches).

FUJITSU LIMITED

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