3Stacked MCP (Multi-Chip Package) FLASH & FLASH & FCRAM

CMOS

64M (×16) FLASH MEMORY & 32M (×16) FLASH MEMORY & 64M (×16) Mobile FCRAM ™

MB84VF5F4F5J1-70

■ FEATURES

- **Power supply voltage of 2.7 to 3.1V**
- **High performance**
  70 ns maximum access time (Flash_1: 64Mb Falsh)
  70 ns maximum access time (Flash_2 : 32Mb Falsh)
  65 ns maximum access time (FCRAM : 64Mb FCRAM)
- **Operating Temperature**
  –30 °C to +85 °C
- **Package 107-ball BGA**

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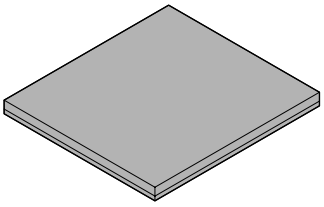
■ PRODUCT LINEUP

	Flash_1	Flash_2	FCRAM
Supply Voltage (V)	V_{ccf}_1* = 2.7V to 3.1V	V_{ccf}_2* = 2.7V to 3.1V	V_{ccr}* = 2.7V to 3.1V
Max. Address Access Time (ns)	70	70	65
Max. $\overline{CE}$ Access Time (ns)	70	70	65
Max. $\overline{OE}$ Access Time (ns)	30	30	40

Note:*1,All of V_{ccf}_1, V_{ccf}_2, and V_{ccr} must be the same level when either part is being accessed.

■ PACKAGE

107-pin plastic FBGA



BGA-107P-M01

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— FLASH MEMORY_1 & _2

- **Simultaneous Read/Write Operations** (**Dual Bank**)
- **Flash_1 FlexBank™**
  Bank A : 8 Mbit (8 KB × 8 and 64 KB × 15)
  Bank B : 24 Mbit (64 KB × 48)
  Bank C : 24 Mbit (64 KB × 48)
  Bank D : 8 Mbit (8 KB × 8 and 64 KB × 15)
- **Flash_2 FlexBank™**
  Bank A : 4 Mbit (8 KB × 8 and 64 KB × 7)
  Bank B : 12 Mbit (64 KB × 24)
  Bank C : 12 Mbit (64 KB × 24)
  Bank D : 4 Mbit (64 KB × 8)
  Two virtual Banks are chosen from the combination of four physical banks.
  Host system can program or erase in one bank, and then read immediately and simultaneously from the other bank with zero latency between read and write operations.
  Read-while-erase
  Read-while-program
- **Minimum 100,000 Program/Erase Cycles**
- **Sector Erase Architecture**
  Sixteen 4 Kword and one hundred twenty-six 32 Kword sectors in word.
  Any combination of sectors can be concurrently erased. It also supports full chip erase.
- **Hidden ROM** (**Hi-ROM**) **Region**
  256 byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC Input Pin**
  At V_{IL}, allows protection of “outermost” 2 × 8 Kbytes on both ends of boot sectors, regardless of sector protection/unprotection status
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, increases program performance
- **Embedded Erase™ Algorithms**
  Automatically preprograms and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready/Busy Output (RY/$\overline{\text{BY}}$_1 or RY/$\overline{\text{BY}}$_2)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, the device automatically switches itself to low power mode.
- **Low V_{CC}f write inhibit ≤ 2.5 V**
- **Program Suspend/Resume**
  Suspends the program operation to allow a read in another byte
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read data and/or program in another sector within the same device
- **Please Refer to “MBM29DL64DF” Datasheet in Detailed Function for Flash_1.**
- **Please Refer to “MBM29DL32BF” Datasheet in Detailed Function for Flash_2.**

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— FCRAM

- **Power Dissipation**
  Operating : 25mA max.
  Standby : 200 µA max.
- **Power Down Mode**
  Sleep : 10 µA max.
  NAP : 65 µA max.
  16M Partial : 85 µA max.
- **Power Down Control by CE2r**
- **Byte Write Control: $\overline{LB}$(DQ_7-DQ_0), $\overline{UB}$(DQ_{15}-DQ_8)**
- **8 words Address Access Capability**

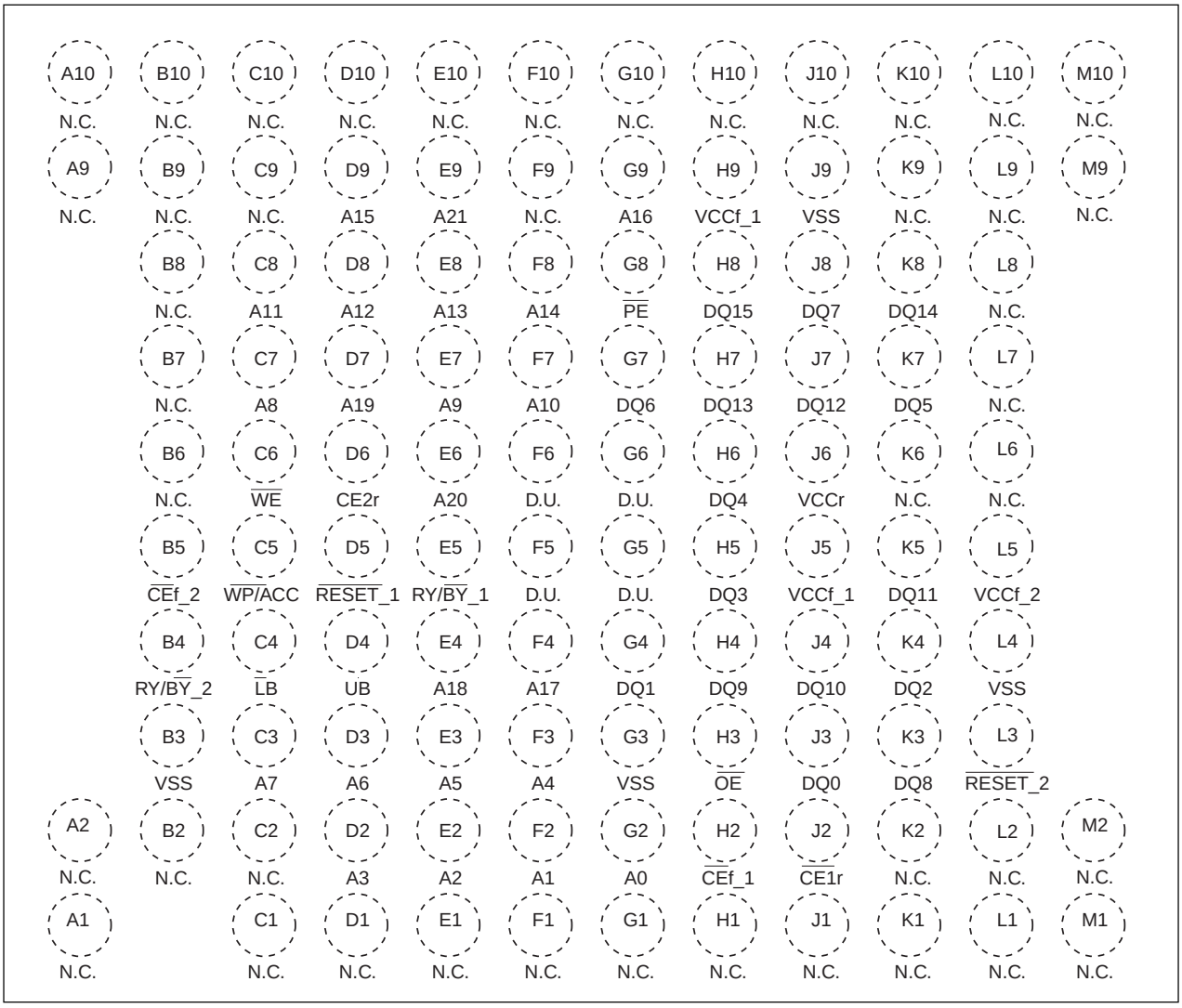
*: FlexBank™ is a trademark of Fujitsu Limited, Japan.

*: Embedded Erase™ and Embedded Program™ are trademarks of Advanced Micro Devices, Inc.

*: Mobile FCRAM™ is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

(Top View)
Marking Side

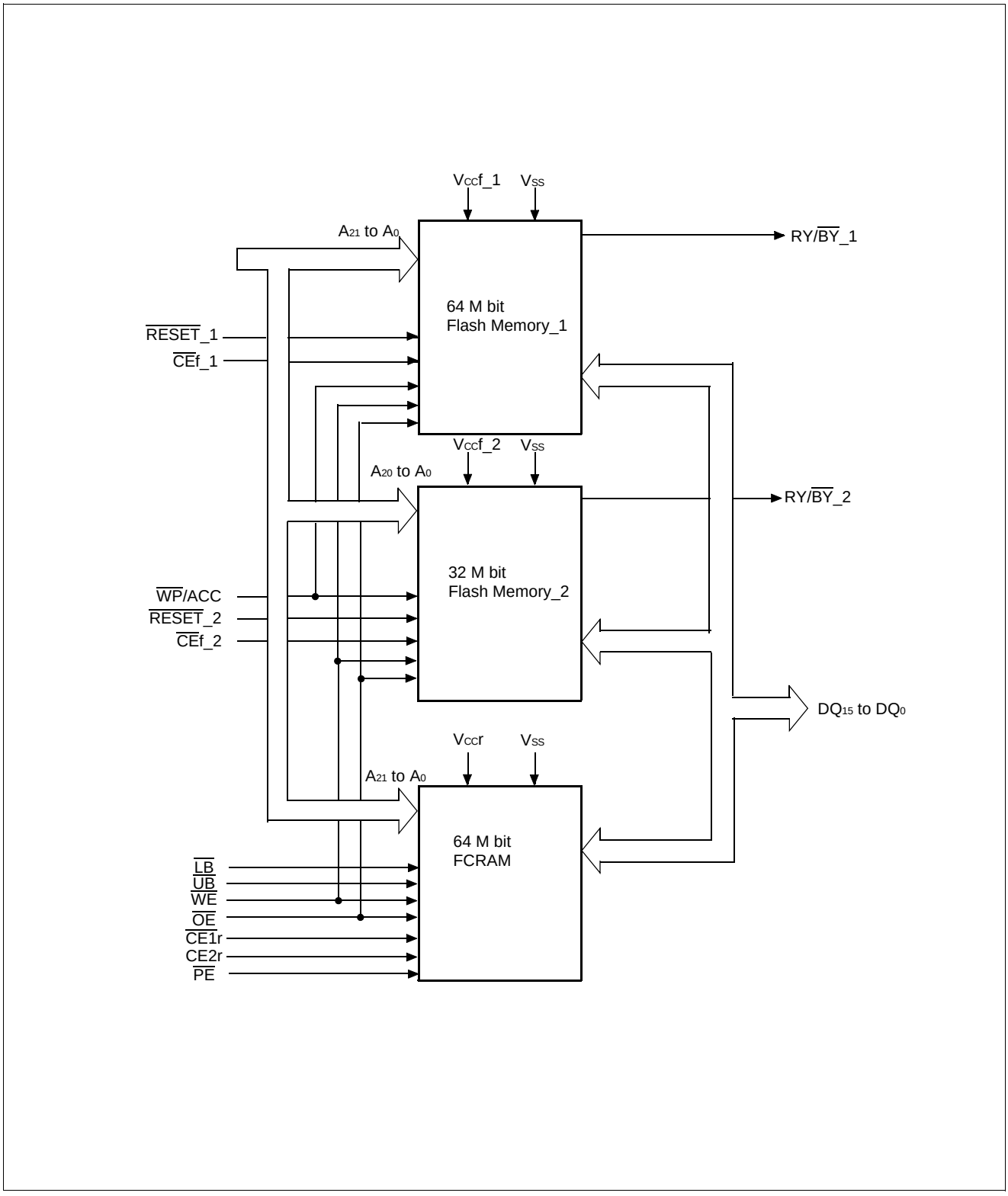


(BGA-107P-M01)

■ PIN DESCRIPTION

Pin name	Input/ Output	Description
A_{20} to A_0	I	Address Inputs (Common)
A_{21}	I	Address Inputs (Flash_1 & FCRAM)
DQ_{15} to DQ_0	I/O	Data Inputs/Outputs (Common)
$\overline{CE}$f_1	I	Chip Enable (Flash_1)
$\overline{CE}$f_2	I	Chip Enable (Flash_2)
$\overline{CE1}$r	I	Chip Enable (FCRAM)
CE2r	I	Chip Enable (FCRAM)
$\overline{OE}$	I	Output Enable (Common)
$\overline{WE}$	I	Write Enable (Common)
RY/$\overline{BY}$_1	O	Ready/Busy Output (Flash_1) Open Drain Output
RY/$\overline{BY}$_2	O	Ready/Busy Output (Flash_2) Open Drain Output
$\overline{UB}$	I	Upper Byte Control (FCRAM)
$\overline{LB}$	I	Lower Byte Control (FCRAM)
$\overline{RESET}$_1	I	Hardware Reset Pin/Sector Protection Unlock (Flash_1)
$\overline{RESET}$_2	I	Hardware Reset Pin/Sector Protection Unlock (Flash_2)
$\overline{WP}$/ACC	I	Write Protect / Acceleration (Flash_1& Flash_2)
$\overline{PE}$	I	Partial Enable (FCRAM)
N.C.	—	No Internal Connection
D.U.	—	Don't Use
V_{SS}	Power	Device Ground (Common)
V_{CC}f_1	Power	Device Power Supply (Flash_1)
V_{CC}f_2	Power	Device Power Supply (Flash_2)
V_{CC}r	Power	Device Power Supply (FCRAM)

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

Operation (1), (2)	$\overline{CE}$f_1	$\overline{CE}$f_2	$\overline{CE1}$r	CE2r	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$\overline{PE}$	A_{20} to A_0	DQ_7 to DQ_0	DQ_{15} to DQ_8	$\overline{RESET}$_1	$\overline{RESET}$_2	$\overline{WP}$/ ACC (12)
Full Standby	H	H	H	H	X	X	X	X	H	X	High-Z	High-Z	H	H	X
Output Disable(3)	H	H	L	H	H	H	X	X	H	X (10)	High-Z	High-Z	H	H	X
	L	H	H		H	H	X	X		X					
	H	L	H												
Read from Flash_1 (4)	L	H	H	H	L	H	X	X	H	Valid	D_{OUT}	D_{OUT}	H	H	X
Read from Flash_2 (4)	H	L	H	H	L	H	X	X	H	Valid	D_{OUT}	D_{OUT}	H	H	X
Write to Flash _1	L	H	H	H	H	L	X	X	H	Valid	D_{IN}	D_{IN}	H	H	X
Write to Flash_2	H	L	H	H	H	L	X	X	H	Valid	D_{IN}	D_{IN}	H	H	X
Read from FCRAM(5)	H	H	L	H	L	H	L (9)	L (9)	H	Valid	D_{OUT}	D_{OUT}	H	H	X
Write to FCRAM	H	H	L	H	H	L	L	L	H	Valid	D_{IN}	D_{IN}	H	H	X
							H	L			High-Z	D_{IN}			
							L	H			D_{IN}	High-Z			
Flash_1 Temporary Sector Group Unprotection(6)	X	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X	X
Flash_ 2 Temporary Sector Group Unprotection(6)	X	X	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash_1 Hardware Reset	X	X	H	H	X	X	X	X	X	X	High-Z	High-Z	L	X	X
Flash_2 Hardware Reset	X	X	H	H	X	X	X	X	X	X	High-Z	High-Z	X	L	X
Flash_1 or 2 Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
FCRAM Power Down Program	H	H	H	H	X	X	X	X	L	Valid	High-Z	High-Z	H	H	X
FCRAM No Read (7)	H	H	L	H	L	H	H	H	H	Valid	High-Z	High-Z	H	H	X
FCRAM Power Down (8)	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

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Notes:
1. Other operations except for indicated this column are inhibited.
2. Do not apply for a following state two or more on the same time;
   1) $\overline{CE}f\_1 = V_{IL}$, 2)$\overline{CE}f\_2 = V_{IL}$, 3) $\overline{CE}1r = V_{IL}$ and $CE2r = V_{IH}$
3. FCRAM Output Disable condition should not be kept longer than 1µs.
4. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
5. FCRAM $\overline{LB}$, $\overline{UB}$ control at Read operation is not supported.
6. It is also used for the extended sector group protections.
7. The FCRAM Power Down Program can be performed one time after compliance of Power-UP timings and it should not be re-programmed after regular Read or Write.
8. FCRAM Power Down mode can be entered from Standby state and all DQ pins are in High-Z state. $I_{PD}r$ current and data retention depends on the selection of Power Down Program.
9. Either or both $\overline{LB}$ and $\overline{UB}$ must be Low for FCRAM Read Operation.
10. Can be either V_{IL} or V_{IH} but must be valid before Read or Write.
11. See “ FCRAM Power Down Program Key Table “ in next page.
12. Protect “ outer most “ 2x8K bytes (4 words) on both ends of the boot block sectors.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–30	+85	°C
Voltage with Respect to Ground All pins except $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2,$\overline{\text{WP}}$/ACC *1	V_{IN}, V_{OUT}	–0.3	V_{CC}f_1 +0.3	V
			V_{CC}f_2 +0.3	V
			V_{CC}r +0.3	V
V_{CC}f_1/V_{CC}f_2/V_{CC}r Supply *1	V_{CC}f_1,V_{CC}f_2, V_{CC}r	–0.3	+3.3	V
$\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 *2	V_{IN}	–0.5	+ 13.0	V
$\overline{\text{WP}}$/ACC *3	V_{IN}	–0.5	+10.5	V

*1 Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –1.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC}f_1 + 0.3 V or V_{CC}f_2 + 0.3 V or V_{CC}r + 0.3 V. During voltage transitions, input or I/O pins may overshoot to V_{CC}f_1 + 2.0 V or V_{CC}f_2 + 2.0 V or V_{CC}r + 1.0 V for periods of up to 20 ns.

*2: Minimum DC input voltage on $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 pin is –0.5 V. During voltage transitions $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns.
Voltage difference between input and supply voltage (VIN-V_{CC}f_1 or V_{CC}f_2) does not exceed +9.0 V.
Maximum DC input voltage on $\overline{\text{RESET}}$_1 or $\overline{\text{RESET}}$_2 pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

*3: Minimum DC input voltage on $\overline{\text{WP}}$/ACC pin is –0.5 V. During voltage transitions, $\overline{\text{WP}}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{\text{WP}}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when V_{CC}f_1 or V_{CC}f_2 is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T_A	–30	+85	°C
V_{CC}f_1/V_{CC}f_2/V_{CC}r Supply Voltages	V_{CC}f_1,V_{CC}f_2,V_{CC}r	+2.7	+3.1	V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter	Sym-bol	Conditions		Value			Unit
				Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to $V_{CC}f\_1, V_{CC}r$		–1.0	—	+1.0	mA
Output Leakage Current	I_{LO}	V_{OUT} = V_{SS} to $V_{CC}f\_1, V_{CC}r$		–1.0	—	+1.0	mA
$\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC}f$ = $V_{CC}f$ Max., $\overline{RESET}$ = 12.5 V		—	—	35	µA
Flash_1 V_{CC} Active Current (Read) *1	$I_{CC1}f\_1$	$\overline{CE}f\_1$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} =5 MHz	—	—	18	mA
			t_{CYCLE} =1 MHz	—	—	4	mA
Flash_1 V_{CC} Active Current (Program/Erase) *2	$I_{CC2}f\_1$	$\overline{CE}f\_1$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	35	mA
Flash_1 V_{CC} Active Current (Read-While-Program) *5	$I_{CC3}f\_1$	$\overline{CE}f\_1$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	53	mA
Flash_1 V_{CC} Active Current (Read-While-Erase) *5	$I_{CC4}f\_1$	$\overline{CE}f\_1$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	53	mA
Flash_1 V_{CC} Active Current (Erase-Suspend-Program)	$I_{CC5}f\_1$	$\overline{CE}f$ _1= V_{IL}, $\overline{OE}$ = V_{IH}		—	—	40	mA
Flash_2 V_{CC} Active Current (Read) *1	$I_{CC1}f\_2$	$\overline{CE}f\_2$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} =5 MHz	—	—	18	mA
			t_{CYCLE} =1 MHz	—	—	4	
Flash_2 V_{CC} Active Current (Program/Erase) *2	$I_{CC2}f\_2$	$\overline{CE}\_2$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	35	mA
Flash_2 V_{CC} Active Current (Read-While-Program) *5	$I_{CC3}f\_2$	$\overline{CE}\_2$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	53	mA
Flash_2 V_{CC} Active Current (Read-While-Erase) *5	$I_{CC4}f\_2$	$\overline{CE}\_2$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	53	mA
Flash_2 V_{CC} Active Current (Erase-Suspend-Program)	$I_{CC5}f\_2$	$\overline{CE}\_2$ = V_{IL}, $\overline{OE}$ = V_{IH}		—	—	35	mA
$\overline{WP}$/ACC Acceleration Program Current	I_{ACC}	$V_{CC}f$ = $V_{CC}f$ Max., $\overline{WP}$/ACC = V_{ACC} Max.		—	—	20	mA
FCRAM V_{CC} Active Current	$I_{CC1}r$	$V_{CC}r$ = $V_{CC}r$ Max., CE1r = V_{IL}, CE2r = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	t_{RC} / t_{WC} =min.	—	—	25	mA
			t_{RC} / t_{WC} =1ms	—	—	3	
Flash V_{CC} Standby Current	$I_{SB1}f$	$V_{CC}f$ = $V_{CC}f$ Max., $\overline{CE}f$ = $V_{CC}f$ ± 0.3 V $\overline{RESET}$ = $V_{CC}f$ ± 0.3 V, $\overline{WP}$/ACC = $V_{CC}f$± 0.3 V		—	1 *7	5 *7	µA
Flash V_{CC} Standby Current ($\overline{RESET}$)	$I_{SB2}f$	$V_{CC}f$ = $V_{CC}f$ Max., $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/ACC = $V_{CC}f$± 0.3 V		—	1 *7	5 *7	µA
Flash V_{CC} Current (Auto-matic Sleep Mode) *3	$I_{SB3}f$	$V_{CC}f$ = $V_{CC}f$ Max., $\overline{CE}f$ = V_{SS} ± 0.3 V $\overline{RESET}$ = $V_{CC}f$ ± 0.3 V, $\overline{WP}$/ACC = $V_{CC}f$± 0.3 V, V_{IN} = $V_{CC}f$± 0.3 V or V_{SS} ± 0.3 V		—	1 *7	5 *7	µA

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Parameter	Sym-bol	Conditions		Value			Unit
				Min.	Typ.	Max.	
FCRAM V_{CC} Standby Current	$I_{SB1}r$	$V_{CC}r$ = $V_{CC}r$ Max., $\overline{CE1}r \geq V_{CC}r - 0.2V$, $CE2r \geq V_{CC}r - 0.2V$, $V_{IN} \leq 0.2$ V or $V_{CC}r - 0.2$ V		—	—	200	µA
FCRAM V_{CC} Power Down Current	$I_{PDS}r$	$\overline{V_{CC}}r$ = $V_{CC}r$ Max., $\overline{CE1}r \geq V_{CC}r - 0.2V$, $CE2r \leq 0.2V$, V_{IN} Cycle time = t_{RC} min.	Sleep	—	—	10	µA
	$I_{PDN}r$		NAP	—	—	65	µA
	$I_{PD8}r$		16M Partial	—	—	85	µA
Input Low Level	V_{IL}	—		–0.3	—	0.5	V
Input High Level	V_{IH}	—		2.2	—	V_{CC}+ 0.3 *6	V
Voltage for Sector Protection, and Temporary Sector Un-protection ($\overline{RESET}$) *4	V_{ID}	—		11.5	—	12.5	V
Voltage for $\overline{WP}$/ACC Sector Protection/Unprotection and Program Acceleration *4	V_{ACC}	—		8.5	9.0	9.5	V
Output Low Voltage Level	$V_{OL}f$	$V_{CC}f$ = $V_{CC}f$ Min., I_{OL}=4.0 mA	Flash	—	—	0.45	V
	$V_{OL}r$	$V_{CC}r$ = $V_{CC}r$ Min., I_{OL} =1.0mA	FCRAM	—	—	0.4	V
Output High Voltage Level	$V_{OH}f$	$V_{CC}f$ = $V_{CC}f$ Min., I_{OH}=–0.1 mA	Flash	$V_{CC}f$– 0.4	—	—	V
	$V_{OH}r$	$V_{CC}r$ = $V_{CC}r$ Min., I_{OH} =–0.5mA	FCRAM	2.2	—	—	V
Flash Low $V_{CC}f$ Lock-Out Voltage	V_{LKO}	—		2.3	2.4	2.5	V

Legend: Flash means Flash_1 or Flash_2, $V_{CC}f$ means $V_{CC}f\_1$ or $V_{CC}f\_2$, $V_{SS}f$ means $V_{SS}f\_1$ or $V_{SS}f\_2$, $\overline{CE}f$ means $\overline{CE}f\_1$ or $\overline{CE}f\_2$, $\overline{RESET}$ means $\overline{RESET}\_1$ or $\overline{RESET}\_2$

*1: The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2: I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3: Automatic sleep mode enables the low power mode when address remains stable for 150 ns.

*4: Applicable for only $V_{CC}f$ applying.

*5: Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

*6: V_{CC} indicates lower of $V_{CC}f\_1$ or $V_{CC}f\_2$ or $V_{CC}r$.

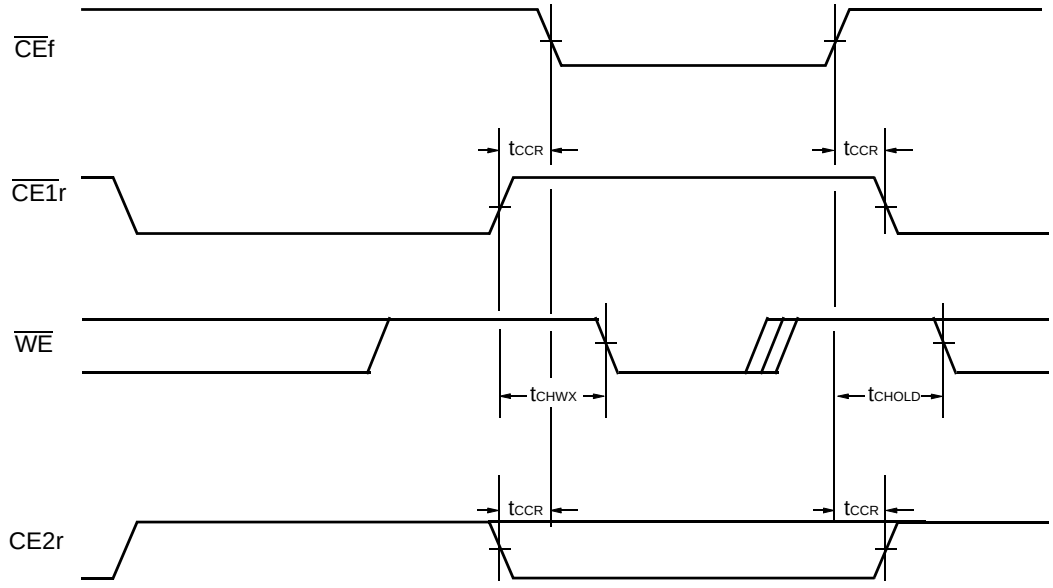
*7: Actual Standby Current is twice of what is indicated in the table, due to two Flash memory chips embedment with one device.

2. AC Characteristics

- **$\overline{CE}$ Timing**

Parameter	Symbol		Condition	Value		Unit
	JEDEC	Standard		Min.	Max.	
$\overline{CE}$ Recover Time	—	t_{CCR}	—	0	—	ns
$\overline{CE}$ Hold Time	—	t_{CHOLD}	—	3	—	ns
$\overline{CE1}$r, High to $\overline{WE}$ Invalid time for Standby Entry	—	t_{CHWX}	—	10	—	ns

- **Timing Diagram for alternating RAM to Flash_1 or Flash_2**



- **Flash_1 Characteristics**
  Please refer to “64M Flash Memory for MCP“ part. In this part, Flash means Flash_1, V_{CC}f means V_{CC}f_1, V_{SS}f means V_{SS}f_1, $\overline{CE}$f means $\overline{CE}$f _1, $\overline{RESET}$ means $\overline{RESET}$_1

- **Flash_2 Characteristics**
  Please refer to “32M Flash Memory for MCP“ part. In this part, Flash means Flash_2, V_{CC}f means V_{CC}f_2, V_{SS}f means V_{SS}f_2, $\overline{CE}$f means $\overline{CE}$f _2, $\overline{RESET}$ means $\overline{RESET}$_2

- **FCRAM Characteristics**
  Please refer to “64M FCRAM for MCP“ part.

■ PIN CAPACITANCE

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Capacitance	C_{IN}	V_{IN} = 0	—	—	20.0	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0	—	—	25.0	pF
Control Pin Capacitance	C_{IN2}	V_{IN} = 0	—	—	25.0	pF

Note: Test conditions Ta = 25°C, f = 1.0 MHz

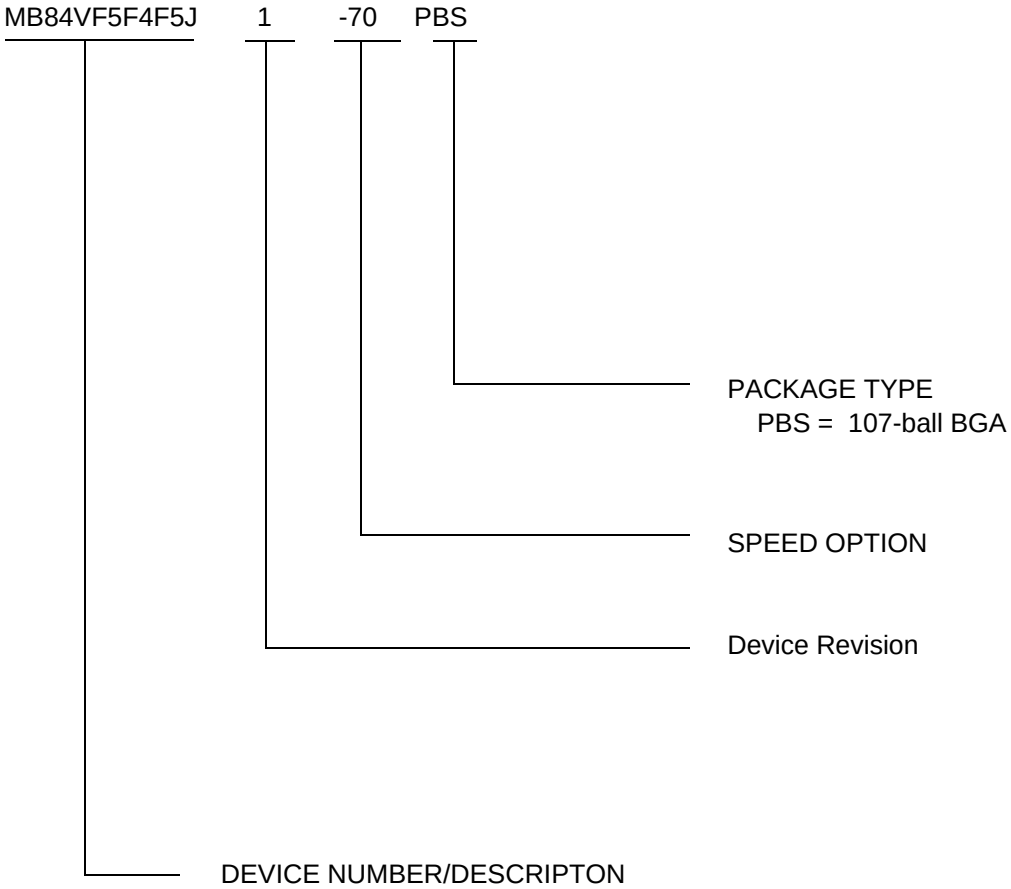
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

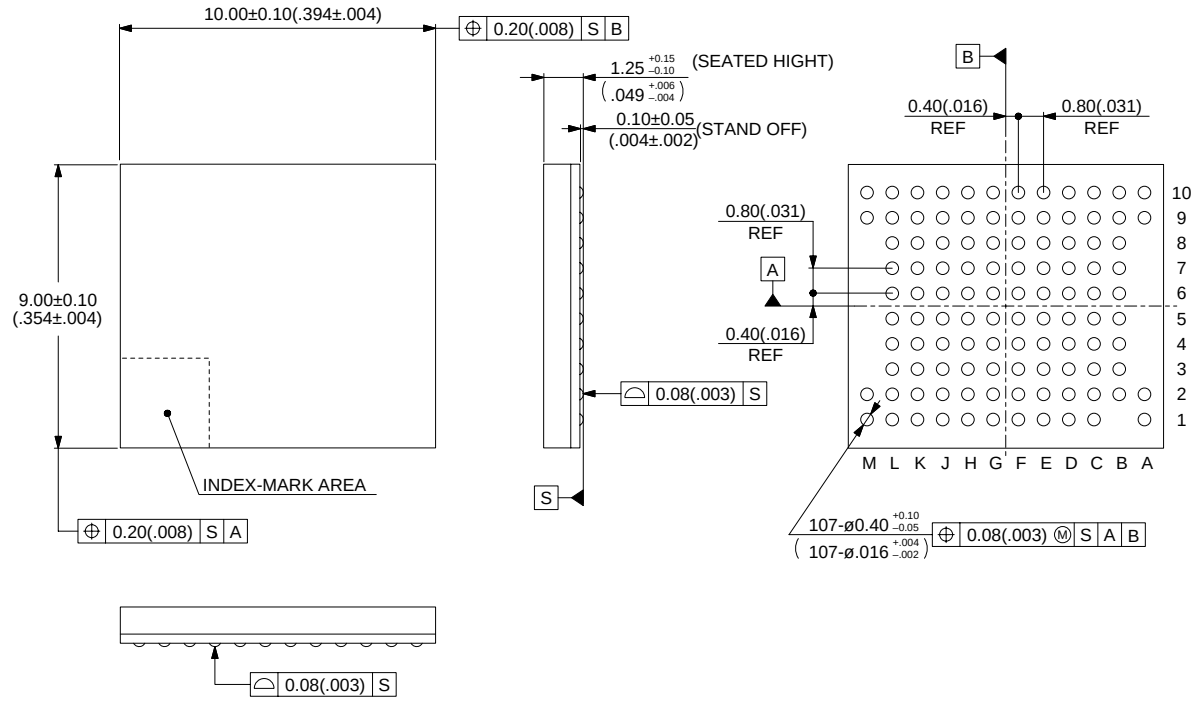
- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{\text{RESET}}$. Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{\text{RESET}}$.
- Without the high voltage (V_{ID}) , sector group protection can be achieved by using “Extended Sector Group Protection” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSION

107-pin plastic FBGA
(BGA-107P-M01)



Dimensions in mm (inches).

FUJITSU LIMITED

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