Stacked MCP (Multi-Chip Package) FLASH MEMORY & SRAM

CMOS

16M (×8/×16) FLASH MEMORY & 4M (×8/×16) STATIC RAM

MB84VD2118XEM-70/MB84VD2119XEM-70

■ FEATURES

- **Power Supply Voltage of 2.7 V to 3.3 V**
- **High Performance**
  70 ns maximum access time (Flash)
  70 ns maximum access time (SRAM)
- **Operating Temperature**
  –40°C to +85°C
- **Package 56-ball BGA**

(Continued)

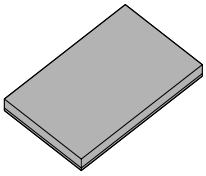
■ PRODUCT LINE UP

Part No.	MB84VD2118XEM/MB84VD2119XEM	
Supply Voltage(V)	$V_{CC}f$= 3.0V $^{+0.3\ V}_{-0.3\ V}$	$V_{CC}s$= 3.0V $^{+0.3V}_{-0.3\ V}$
Max. Address Access Time (ns)	70	70
Max. $\overline{CE}$ Access Time (ns)	70	70
Max. $\overline{OE}$ Access Time (ns)	30	35

Note: Both $V_{CC}f$ and $V_{CC}s$ must be in recommended operation range when either part is being accessed.

■ PACKAGE

56-ball plastic BGA



(BGA-56P-M02)

(Continued)

— FLASH MEMORY

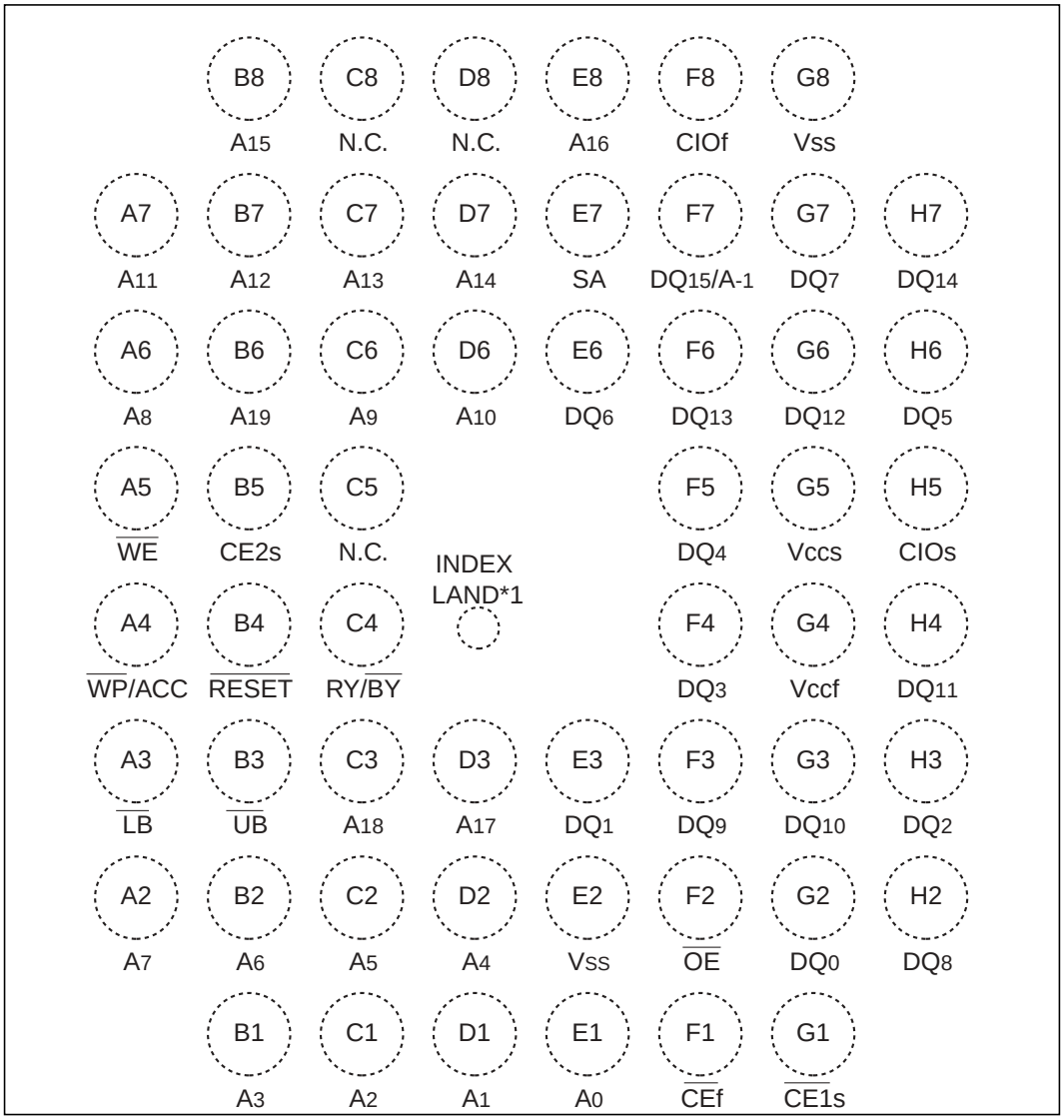
- **Simultaneous Read/Write Operations (Dual Bank)**
  Miltiple devices available with different bank sizes (Please refer to ORDERING INFORMATION)
  Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
  Zero latency between read and write operations
  Read-while-erase
  Read-while-program
- **Minimum 100,000 Write/Erase Cycles**
- **Sector Erase Architecture**
  Eight 4 K words and thirty one 32 K words.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  MB84VD2118XEM: Top sector
  MB84VD2119XEM: Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit Feature for Detection of Program or Erase Cycle Completion**
- **Ready-Busy Output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic Sleep Mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} Write Inhibit ≤ 2.5 V**
- **Hidden ROM (Hi-ROM) Region**
  64K byte of Hi-ROM, accessible through a new “Hi-ROM Enable” command sequence
  Factory serialized and protected to provide a secure electronic serial number (ESN)
- **$\overline{\text{WP}}$/ACC Input Pin**
  At V_{IL}, allows protection of boot sectors, regardless of sector protection/unprotection status
  (MB84VD2118XEM:SA37,SA38 MB84VD2119XEM:SA0,SA1)
  At V_{IH}, allows removal of boot sector protection
  At V_{ACC}, program time will reduse by 40%.
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device
- **Please refer to “MBM29DL16XTE/BE” Datasheet in Detailed Function**

— SRAM

- **Power Dissipation**
  Operating : 40 mA max.
  Standby : 15 µA max.
- **Power Down Features using $\overline{\text{CE1}}$s and CE2s**
- **Data Retention Supply Voltage: 1.5 V to 3.3 V**
- **$\overline{\text{CE1}}$s and CE2s Chip Select**
- **Byte Data Control: $\overline{\text{LB}}$ (DQ_0 to DQ_7), $\overline{\text{UB}}$ (DQ_8 to DQ_{15})**

■ PIN ASSIGNMENT

(Top View)
Marking side



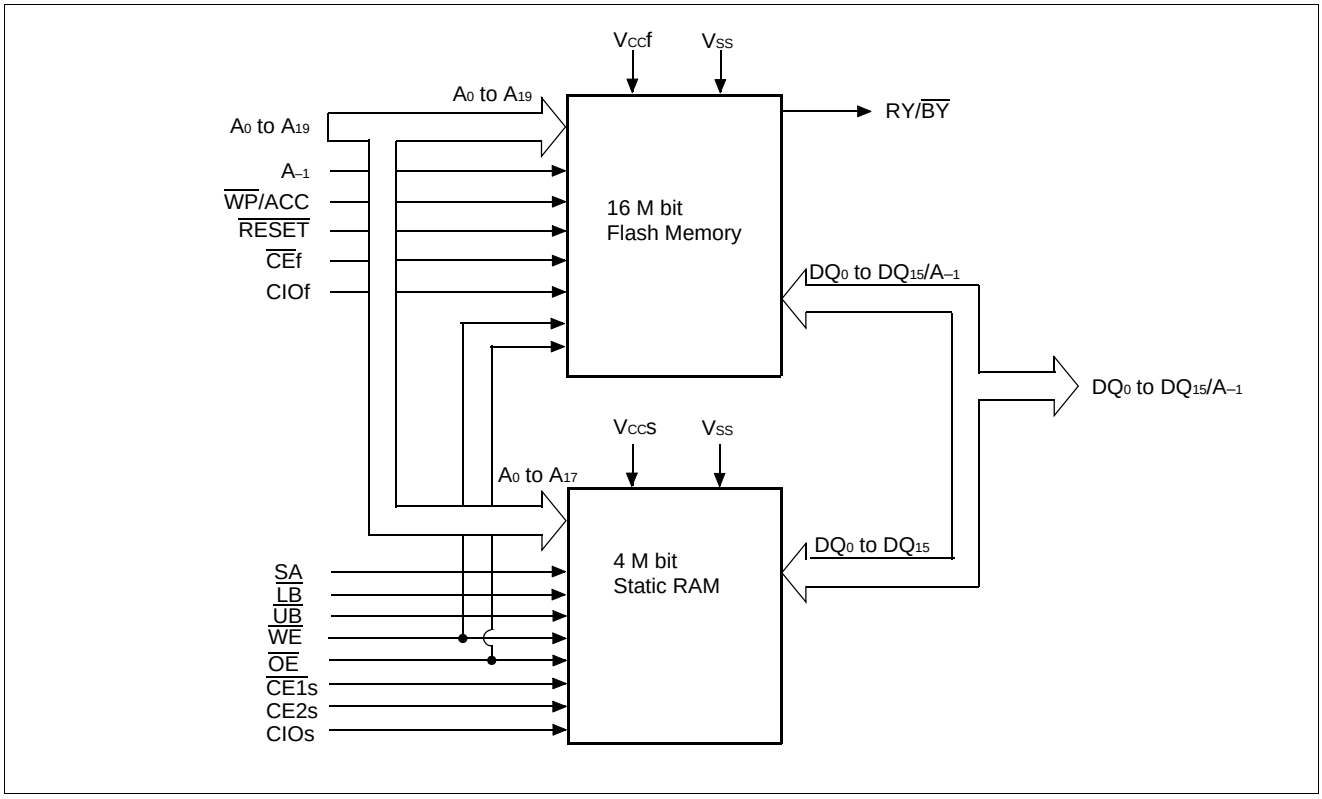
*1) There is no solder ball. This land should be open electrically.

(BGA-56P-M02)

■ PIN DESCRIPTION

Pin Name	Function	Input/Output
A_{17} to A_0	Address Inputs (Common)	I
A_{19} to A_{18}, A_{-1}	Address Input (Flash)	I
SA	Address Input (SRAM)	I
DQ_{15} to DQ_0	Data Inputs / Outputs (Common)	I/O
$\overline{CE}$f	Chip Enable (Flash)	I
$\overline{CE1}$s	Chip Enable (SRAM)	I
CE2s	Chip Enable (SRAM)	I
$\overline{OE}$	Output Enable (Common)	I
$\overline{WE}$	Write Enable (Common)	I
RY/$\overline{BY}$	Ready/Busy Outputs (Flash) Open Drain Output	O
$\overline{UB}$	Upper Byte Control (SRAM)	I
$\overline{LB}$	Lower Byte Control (SRAM)	I
CIOf	I/O Configuration (Flash) CIOf=V_{CC}f is Word mode (×16), CIOf=V_{SS} is Byte mode (× 8)	I
CIOs	I/O Configuration (SRAM) CIOs=V_{CC}s is Word mode (×16), CIOs=V_{SS} is Byte mode (× 8)	I
$\overline{RESET}$	Hardware Reset Pin / Sector Protection Unlock (Flash)	I
$\overline{WP}$/ACC	Write Protect / Acceleration (Flash)	I
N.C.	No Internal Connection	—
V_{SS}	Device Ground (Common)	Power
V_{CC}f	Device Power Supply (Flash)	Power
V_{CC}s	Device Power Supply (SRAM)	Power

■ BLOCK DIAGRAM



■ DEVICE BUS OPERATIONS

Table 1. 1 User Bus Operations (Flash=Word mode; ClOf=V_{CC}f, SRAM=Word mode; ClOs=V_{CC}s)

Operation (1), (3)	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	X	High-Z	High-Z		
		X	L									
Read from Flash (2)	L	H	X	L	H	X	X	X	D_{OUT}	D_{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D_{IN}	D_{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	X	L	L	D_{OUT}	D_{OUT}	H	X
							H	L	High-Z	D_{OUT}		
							L	H	D_{OUT}	High-Z		
Write to SRAM	H	L	H	X	L	X	L	L	D_{IN}	D_{IN}	H	X
							H	L	High-Z	D_{IN}		
							L	H	D_{IN}	High-Z		
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes: 1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
$\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
$\overline{WP}$/ACC = V_{ACC} (9V) ; Program time will reduce by 40%.

Table 1. 2 User Bus Operations (Flash=Word mode; ClOf=V_{CC}f, SRAM=Byte mode; ClOs=V_{SS})

Operation (1), (3)	$\overline{CE}$f	$\overline{CE1}$s	CE2s	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}	$\overline{RESET}$	$\overline{WP}$/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L									
Output Disable	H	L	H	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	H	H	High-Z	High-Z		
	L	H	X	H	H	X	X	X	High-Z	High-Z		
		X	L									
Read from Flash (2)	L	H	X	L	H	X	X	X	D_{OUT}	D_{OUT}	H	X
		X	L									
Write to Flash	L	H	X	H	L	X	X	X	D_{IN}	D_{IN}	H	X
		X	L									
Read from SRAM	H	L	H	L	H	SA	X	X	D_{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	L	SA	X	X	D_{IN}	High-Z	H	X
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L									
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes:
1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
   $\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
   $\overline{WP}$/ACC = V_{ACC} (9V); Program time will reduce by 40%.

Table 1. 3 User Bus Operations (Flash=Byte mode; CIOf=V_{SS}, SRAM=Byte mode; CIOs=V_{SS})

Operation (1), (3)	$\overline{CE}$f	$\overline{CE1}$s	CE2s	DQ_{15}/A_{-1}	$\overline{OE}$	$\overline{WE}$	SA	$\overline{LB}$	$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{14}	$\overline{RESET}$	$\overline{WP}$/ ACC (5)
Full Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	H	X
		X	L										
Output Disable	H	L	H	X	H	H	X	X	X	High-Z	High-Z	H	X
				X	X	X	X	H	H	High-Z	High-Z		
	L	H	X	A_{-1}	H	H	X	X	X	High-Z	High-Z		
		X	L										
Read from Flash (2)	L	H	X	A_{-1}	L	H	X	X	X	D_{OUT}	X	H	X
		X	L										
Write to Flash	L	H	X	A_{-1}	H	L	X	X	X	D_{IN}	X	H	X
		X	L										
Read from SRAM	H	L	H	X	L	H	SA	X	X	D_{OUT}	High-Z	H	X
Write to SRAM	H	L	H	X	X	L	SA	X	X	D_{IN}	High-Z	H	X
Temporary Sector Group Unprotection(4)	X	X	X	X	X	X	X	X	X	X	X	V_{ID}	X
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	High-Z	High-Z	L	X
		X	L										
Boot Block Sector Write Protection	X	X	X	X	X	X	X	X	X	X	X	X	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}. See DC Characteristics for voltage levels.

Notes:
1. Other operations except for indicated this column are inhibited.
2. $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.
3. Do not apply $\overline{CE}$f = V_{IL}, $\overline{CE1}$s = V_{IL} and CE2s = V_{IH} at a time.
4. It is also used for the extended sector group protections.
5. $\overline{WP}$/ACC = V_{IL}; protection of boot sectors.
   $\overline{WP}$/ACC = V_{IH}; removal of boot sectors protection.
   $\overline{WP}$/ACC = V_{ACC} (9V); Program time will reduce by 40%.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with Respect to Ground All pins except $\overline{RESET}$, $\overline{WP}$/ACC (Note 1)	V_{IN}, V_{OUT}	–0.3	$V_{CC}f$ +0.4	V
			$V_{CC}s$ +0.4	V
$V_{CC}f$/$V_{CC}s$ Supply (Note 1)	$V_{CC}f$,$V_{CC}s$	–0.3	+4.0	V
$\overline{RESET}$ (Note 2)	V_{IN}	–0.5	+ 13.0	V
$\overline{WP}$/ACC (Note 3)	V_{IN}	–0.5	+10.5	V

Notes: 1. Minimum DC voltage on input or I/O pins is –0.3 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is $V_{CC}f$ +0.4 V or $V_{CC}s$+0.4 V. During voltage transitions, input or I/O pins may overshoot to $V_{CC}f$+2.0 V or $V_{CC}s$+2.0 V for periods of up to 20 ns.

2. Minimum DC input voltage on $\overline{RESET}$ pin is –0.5 V. During voltage transitions, $\overline{RESET}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (VIN-$V_{CC}f$ or $V_{CC}s$) does not exceed 9.0 V. Maximum DC input voltage on $\overline{RESET}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.
3. Minimum DC input voltage on $\overline{WP}$/ACC pin is –0.5 V. During voltage transitions, $\overline{WP}$/ACC pin may undershoot Vss to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on $\overline{WP}$/ACC pin is +10.5 V which may overshoot to +12.0 V for periods of up to 20 ns, when $V_{CC}f$ is applied.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min.	Max.	
Ambient Temperature	T_A	–40	+85	°C
$V_{CC}f$/$V_{CC}s$ Supply Voltages	Vccf, Vccs	+2.7	+3.3	V

Note: Operating ranges define those limits between which the functionality of the device is guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter Symbol	Parameter Description	Test Conditions			Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CCf}, V_{CCs}			–1.0	—	+1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CCf}, V_{CCs}			–1.0	—	+1.0	µA
I_{LIT}	$\overline{RESET}$ Inputs Leakage Current	V_{CCf} = V_{CCf} Max., V_{CCs} = V_{CCs} Max., $\overline{RESET}$ = 12.5V			—	—	35	µA
I_{CC1f}	Flash V_{CC} Active Current (Read) (Note 1)	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}	t_{CYCLE} = 5 MHz	Byte	—	—	13	mA
			t_{CYCLE} = 5 MHz	Word	—	—	15	
			t_{CYCLE} = 1 MHz	Byte	—	—	7	mA
			t_{CYCLE} = 1 MHz	Word	—	—	7	
I_{CC2f}	Flash V_{CC} Active Current (Program/Erase) (Note 2)	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
I_{CC3f}	Flash V_{CC} Active Current (Read-While-Program) (Note 5)	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}		Byte	—	—	48	mA
				Word	—	—	50	
I_{CC4f}	Flash V_{CC} Active Current (Read-While-Erase) (Note 5)	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}		Byte	—	—	48	mA
				Word	—	—	50	
I_{CC5f}	Flash V_{CC} Active Current (Erase-Suspend-Program)	$\overline{CE}_f$ = V_{IL}, $\overline{OE}$ = V_{IH}			—	—	35	mA
I_{LIA}	ACC Input Leakage Current	V_{CCf} = V_{CCf} Max., V_{CCs} = V_{CCs} Max., $\overline{WP}$/ACC = V_{ACC} Max			—	—	20	mA
I_{CC1s}	SRAM V_{CC} Active Current	V_{CCs} = V_{CCs} Max., $\overline{CE1}_s$ = V_{IL}, CE2s = V_{IH}	t_{CYCLE} =10 MHz		—	—	40	mA
I_{CC2s}	SRAM V_{CC} Active Current	$\overline{CE1}_s$ = 0.2 V, CE2s = V_{CCs} – 0.2 V	t_{CYCLE} = 10 MHz		—	—	40	mA
			t_{CYCLE} = 1 MHz		—	—	8	mA
I_{SB1f}	Flash V_{CC} Standby Current	V_{CCf} = V_{CCf} Max., $\overline{CE}_f$ = V_{CCf} ± 0.3 V $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V			—	1	5	µA
I_{SB2f}	Flash V_{CC} Standby Current ($\overline{RESET}$)	V_{CCf} = V_{CCf} Max., $\overline{RESET}$ = V_{SS} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V			—	1	5	µA
I_{SB3f}	Flash V_{CC} Current (Automatic Sleep Mode) (Note 3)	V_{CCf} = V_{CCf} Max., $\overline{CE}_f$ = V_{SS} ± 0.3 V $\overline{RESET}$ = V_{CCf} ± 0.3 V, $\overline{WP}$/ACC = V_{CCf}± 0.3 V V_{IN} = V_{CCf}± 0.3 V or V_{SS} ± 0.3 V			—	1	5	µA
I_{SB1s}	SRAM V_{CC} Standby Current	$\overline{CE1}_s$ ≥ V_{CCs} – 0.2 V, CE2s ≥ V_{CCs} – 0.2 V $\overline{LB}$ = $\overline{UB}$ ≥ V_{CCs}–0.2 V or ≤ 0.2V			—	—	15	µA
I_{SB2s}	SRAM V_{CC} Standby Current	$\overline{CE1}_s$ ≥ V_{CCs} – 0.2 V or ≤ 0.2V, CE2s ≤ 0.2 V $\overline{LB}$ = $\overline{UB}$ ≥ V_{CCs}–0.2 V or ≤ 0.2V			—	—	15	µA

(Continued)

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Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Level	—	–0.3	—	0.5	V
V_{IH}	Input High Level	—	2.4	—	V_{CC}+0.3*	V
V_{ID}	Voltage for Sector Protection, and Temporary Sector Unprotection ($\overline{RESET}$) (Note 4)	—	11.5	—	12.5	V
V_{ACC}	Voltage for Program Acceleration ($\overline{WP}$/ACC) (Note4)	—	8.5	9.0	9.5	V
V_{OL}	SRAM Output Low Level	$V_{CC}s$ = $V_{CC}s$ Min., I_{OL}=4.0 mA	—	—	0.45	V
V_{OH}	SRAM Output High Level	$V_{CC}s$ = $V_{CC}s$ Min., I_{OH}=–0.5 mA	2.4	—	—	V
V_{OL}	Flash Output Low Level	$V_{CC}f$ = $V_{CC}f$ Min., I_{OL}=4.0 mA	—	—	0.4	V
V_{OH}	Flash Output High Level	$V_{CC}f$ = $V_{CC}f$ Min., I_{OH}=–0.5 mA	2.4	—	—	V
V_{LKO}	Flash Low $V_{CC}f$ Lock-Out Voltage	—	2.3	—	2.5	V

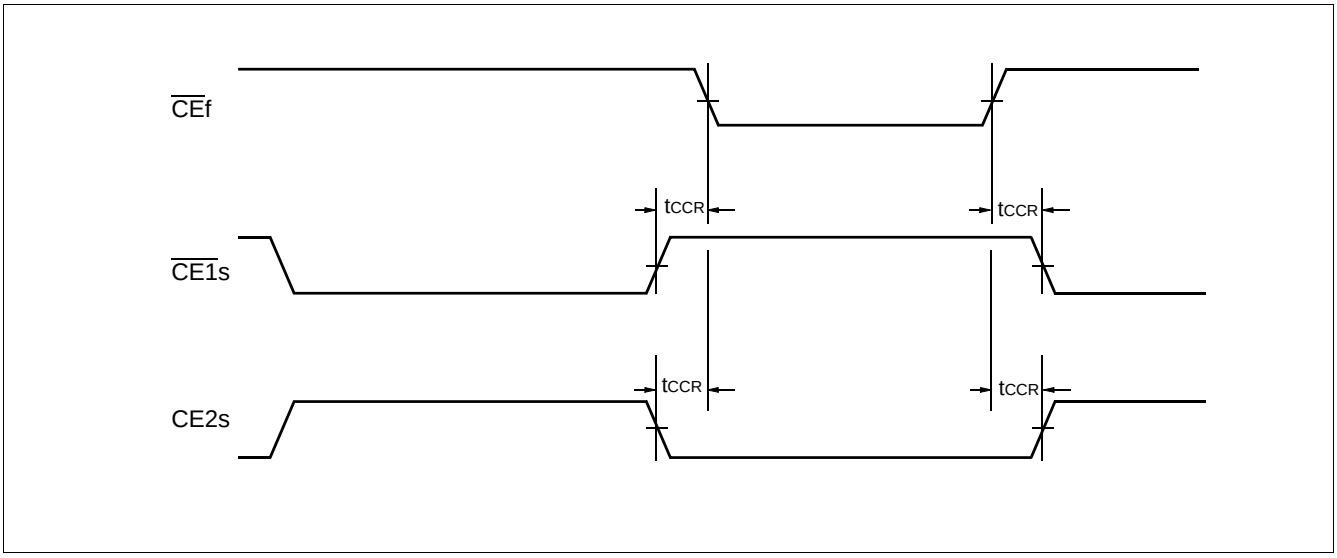
Notes: 1. The I_{CC} current listed includes both the DC operating current and the frequency dependent component.
2. I_{CC} active while Embedded Algorithm (program or erase) is in progress.
3. Automatic sleep mode enables the low power mode when address remain stable for 150 ns.
4. Applicable for only $V_{CC}f$ applying.
5. Embedded Alogorithm (program or erase) is in progress. (@5 MHz)

2. AC Characteristics

- **$\overline{CE}$ Timing**

Parameter Symbols		Description	Test Setup		Value	Unit
JEDEC	Standard					
—	t_{CCR}	$\overline{CE}$ Recover Time	—	Min.	0	ns

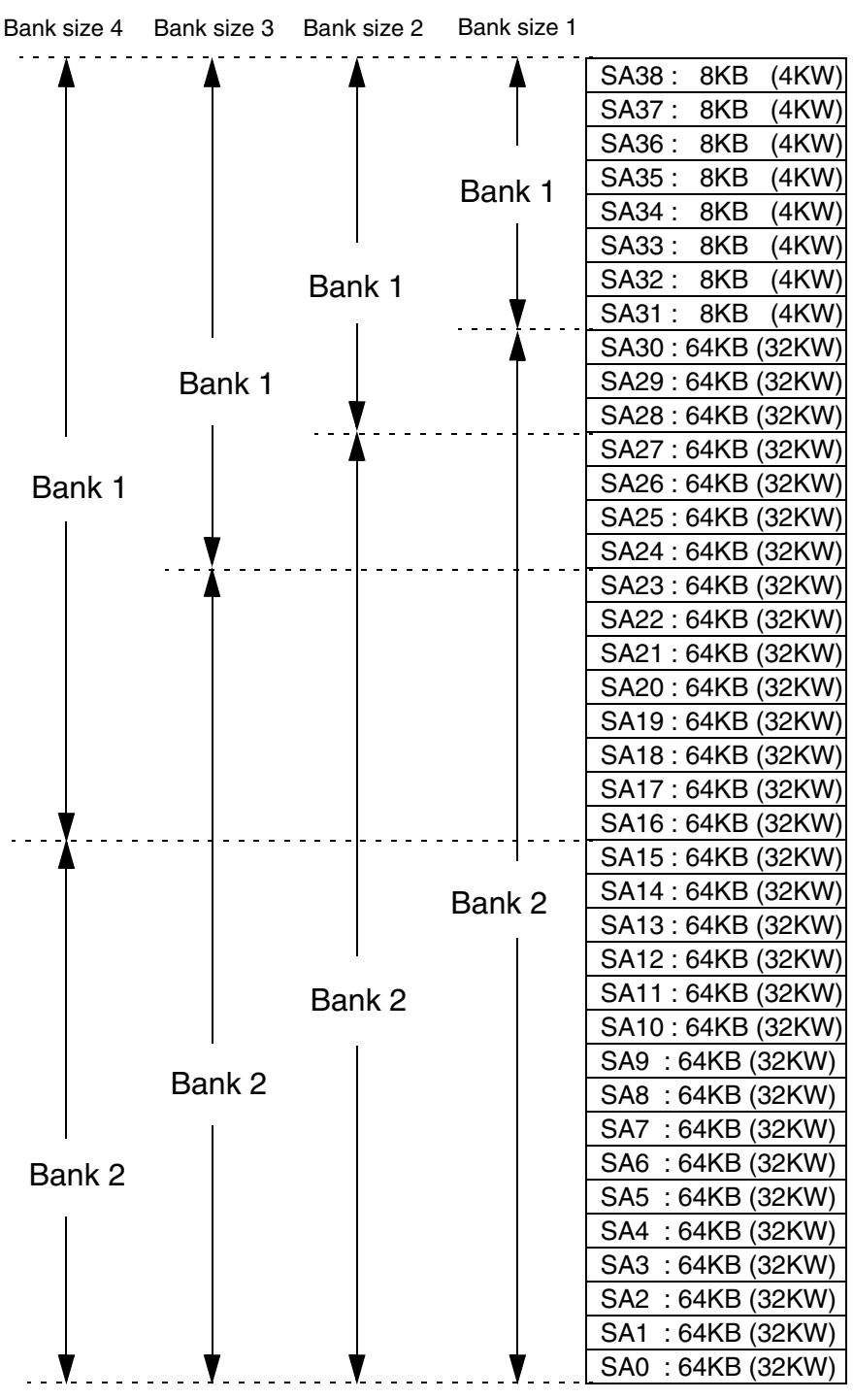
- **Timing Diagram for alternating SRAM to Flash**



- **Flash Characteristics**
  Prease refer to “16M Flash Memory for MCP“ part.
- **SRAM Characteristics,**
  Prease refer to “4M SRAM for MCP“ part.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE on FLASH MEMORY

- Eight 4 K words, and thirty one 32 K words.
- Individual-sector, multiple-sector, or bulk-erase capability.



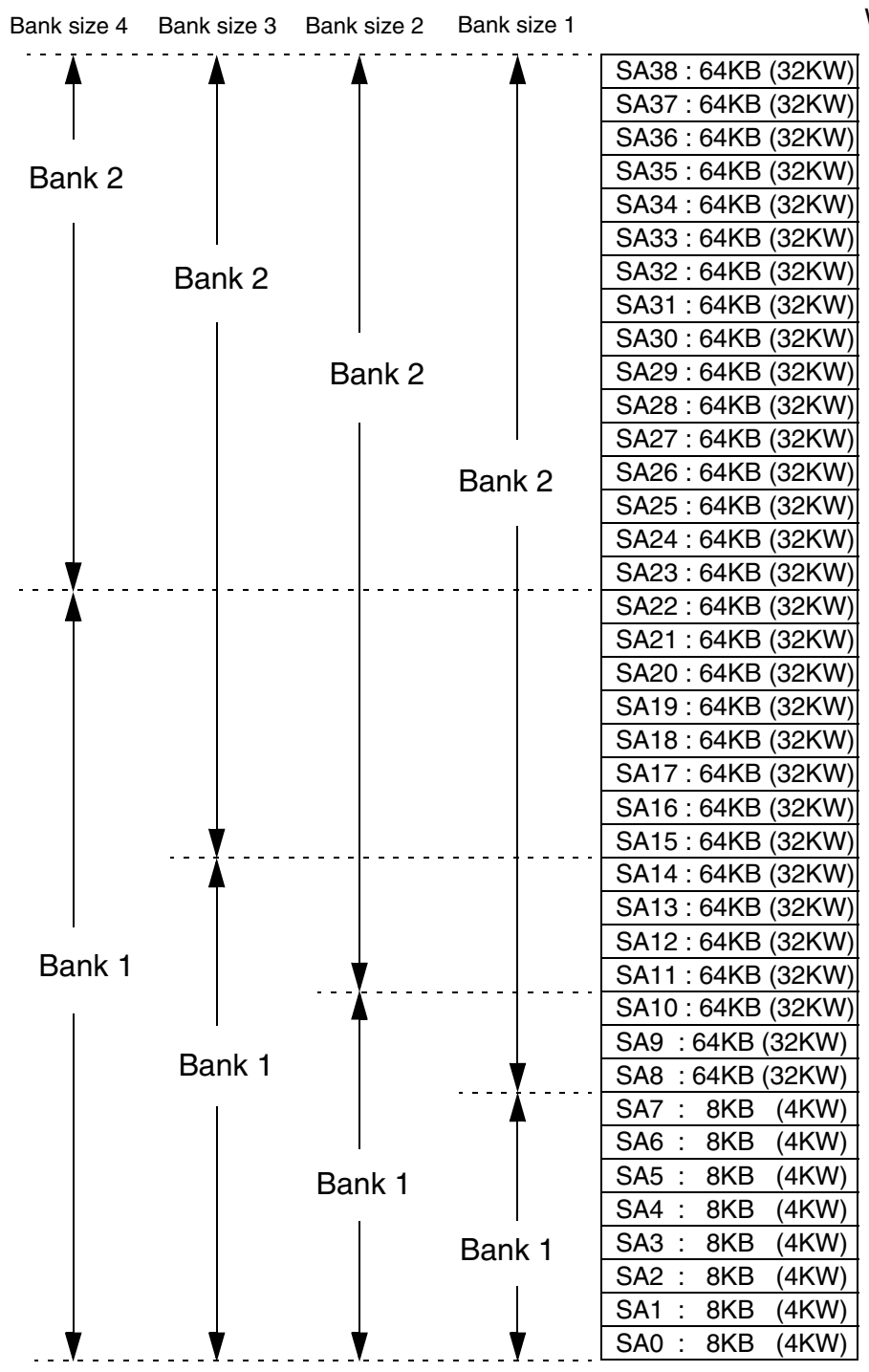
	Word mode	Byte mode
SA38 : 8KB (4KW)	0FFFFFH	1FFFFFH
SA37 : 8KB (4KW)	0FF000H	1FE000H
SA36 : 8KB (4KW)	0FE000H	1FC000H
SA35 : 8KB (4KW)	0FD000H	1FA000H
SA34 : 8KB (4KW)	0FC000H	1F8000H
SA33 : 8KB (4KW)	0FB000H	1F6000H
SA32 : 8KB (4KW)	0FA000H	1F4000H
SA31 : 8KB (4KW)	0F9000H	1F2000H
SA30 : 64KB (32KW)	0F8000H	1F0000H
SA29 : 64KB (32KW)	0F0000H	1E0000H
SA28 : 64KB (32KW)	0E8000H	1D0000H
SA27 : 64KB (32KW)	0E0000H	1C0000H
SA26 : 64KB (32KW)	0D8000H	1B0000H
SA25 : 64KB (32KW)	0D0000H	1A0000H
SA24 : 64KB (32KW)	0C8000H	190000H
SA23 : 64KB (32KW)	0C0000H	180000H
SA22 : 64KB (32KW)	0B8000H	170000H
SA21 : 64KB (32KW)	0B0000H	160000H
SA20 : 64KB (32KW)	0A8000H	150000H
SA19 : 64KB (32KW)	0A0000H	140000H
SA18 : 64KB (32KW)	098000H	130000H
SA17 : 64KB (32KW)	090000H	120000H
SA16 : 64KB (32KW)	088000H	110000H
SA15 : 64KB (32KW)	080000H	100000H
SA14 : 64KB (32KW)	078000H	0F0000H
SA13 : 64KB (32KW)	070000H	0E0000H
SA12 : 64KB (32KW)	068000H	0D0000H
SA11 : 64KB (32KW)	060000H	0C0000H
SA10 : 64KB (32KW)	058000H	0B0000H
SA9 : 64KB (32KW)	050000H	0A0000H
SA8 : 64KB (32KW)	048000H	090000H
SA7 : 64KB (32KW)	040000H	080000H
SA6 : 64KB (32KW)	038000H	070000H
SA5 : 64KB (32KW)	030000H	060000H
SA4 : 64KB (32KW)	028000H	050000H
SA3 : 64KB (32KW)	020000H	040000H
SA2 : 64KB (32KW)	018000H	030000H
SA1 : 64KB (32KW)	010000H	020000H
SA0 : 64KB (32KW)	008000H	010000H
	000000H	000000H

Sector Architecture (Top Boot Block)

(Continued)

16M Flash for MCP

(Continued)



Sector Architecture (Bottom Boot Block)

Sector Address Tables (Top Boot Block, Bank Size=1)

Bank	Sector	Sector Address								Address Range (Byte mode)	Address Range (Word mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
Bank 1	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Sector Address Tables (Bottom Boot Block, Bank Size=1)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFH	000000H to 000FFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFH	001000H to 001FFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFH	002000H to 002FFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFH	003000H to 003FFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFH	004000H to 004FFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFH	005000H to 005FFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFH	006000H to 006FFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFH	007000H to 007FFFH
Bank 2	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFH	0F8000H to 0FFFFFH

Sector Address Tables (Top Boot Block, Bank Size=2)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
Bank 1	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Sector Address Tables (Bottom Boot Block, Bank Size=2)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFH	000000H to 000FFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFH	001000H to 001FFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFH	002000H to 002FFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFH	003000H to 003FFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFH	004000H to 004FFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFH	005000H to 005FFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFH	006000H to 006FFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFH	007000H to 007FFFH
	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
Bank 2	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFH	0F8000H to 0FFFFFH

Sector Address Tables (Top Boot Block, Bank Size=3)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
Bank 1	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Sector Address Tables (Bottom Boot Block, Bank Size=3)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFH	000000H to 000FFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFH	001000H to 001FFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFH	002000H to 002FFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFH	003000H to 003FFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFH	004000H to 004FFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFH	005000H to 005FFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFH	006000H to 006FFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFH	007000H to 007FFFH
	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
Bank 2	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFH	0F8000H to 0FFFFFH

Sector Address Tables (Top Boot Block, Bank Size=4)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 2	SA0	0	0	0	0	0	X	X	X	000000H to 00FFFFH	000000H to 007FFFH
	SA1	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA2	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA3	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA4	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA5	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA6	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA7	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA8	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA9	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA10	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA11	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA12	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA13	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA14	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA15	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
Bank 1	SA16	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA17	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA18	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA19	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA20	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA21	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA22	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA23	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA24	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA25	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA26	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA27	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA28	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA29	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA30	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA31	1	1	1	1	1	0	0	0	1F0000H to 1F1FFFH	0F8000H to 0F8FFFH
	SA32	1	1	1	1	1	0	0	1	1F2000H to 1F3FFFH	0F9000H to 0F9FFFH
	SA33	1	1	1	1	1	0	1	0	1F4000H to 1F5FFFH	0FA000H to 0FAFFFH
	SA34	1	1	1	1	1	0	1	1	1F6000H to 1F7FFFH	0FB000H to 0FBFFFH
	SA35	1	1	1	1	1	1	0	0	1F8000H to 1F9FFFH	0FC000H to 0FCFFFH
	SA36	1	1	1	1	1	1	0	1	1FA000H to 1FBFFFH	0FD000H to 0FDFFFH
	SA37	1	1	1	1	1	1	1	0	1FC000H to 1FDFFFH	0FE000H to 0FEFFFH
	SA38	1	1	1	1	1	1	1	1	1FE000H to 1FFFFFH	0FF000H to 0FFFFFH

Sector Address Tables (Bottom Boot Block, Bank Size=4)

Bank	Sector	Sector Address								Address Range (BYTE mode)	Address Range (WORD mode)
		Bank Address									
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}		
Bank 1	SA0	0	0	0	0	0	0	0	0	000000H to 001FFFH	000000H to 000FFFH
	SA1	0	0	0	0	0	0	0	1	002000H to 003FFFH	001000H to 001FFFH
	SA2	0	0	0	0	0	0	1	0	004000H to 005FFFH	002000H to 002FFFH
	SA3	0	0	0	0	0	0	1	1	006000H to 007FFFH	003000H to 003FFFH
	SA4	0	0	0	0	0	1	0	0	008000H to 009FFFH	004000H to 004FFFH
	SA5	0	0	0	0	0	1	0	1	00A000H to 00BFFFH	005000H to 005FFFH
	SA6	0	0	0	0	0	1	1	0	00C000H to 00DFFFH	006000H to 006FFFH
	SA7	0	0	0	0	0	1	1	1	00E000H to 00FFFFH	007000H to 007FFFH
	SA8	0	0	0	0	1	X	X	X	010000H to 01FFFFH	008000H to 00FFFFH
	SA9	0	0	0	1	0	X	X	X	020000H to 02FFFFH	010000H to 017FFFH
	SA10	0	0	0	1	1	X	X	X	030000H to 03FFFFH	018000H to 01FFFFH
	SA11	0	0	1	0	0	X	X	X	040000H to 04FFFFH	020000H to 027FFFH
	SA12	0	0	1	0	1	X	X	X	050000H to 05FFFFH	028000H to 02FFFFH
	SA13	0	0	1	1	0	X	X	X	060000H to 06FFFFH	030000H to 037FFFH
	SA14	0	0	1	1	1	X	X	X	070000H to 07FFFFH	038000H to 03FFFFH
	SA15	0	1	0	0	0	X	X	X	080000H to 08FFFFH	040000H to 047FFFH
	SA16	0	1	0	0	1	X	X	X	090000H to 09FFFFH	048000H to 04FFFFH
	SA17	0	1	0	1	0	X	X	X	0A0000H to 0AFFFFH	050000H to 057FFFH
	SA18	0	1	0	1	1	X	X	X	0B0000H to 0BFFFFH	058000H to 05FFFFH
	SA19	0	1	1	0	0	X	X	X	0C0000H to 0CFFFFH	060000H to 067FFFH
	SA20	0	1	1	0	1	X	X	X	0D0000H to 0DFFFFH	068000H to 06FFFFH
	SA21	0	1	1	1	0	X	X	X	0E0000H to 0EFFFFH	070000H to 077FFFH
	SA22	0	1	1	1	1	X	X	X	0F0000H to 0FFFFFH	078000H to 07FFFFH
Bank 2	SA23	1	0	0	0	0	X	X	X	100000H to 10FFFFH	080000H to 087FFFH
	SA24	1	0	0	0	1	X	X	X	110000H to 11FFFFH	088000H to 08FFFFH
	SA25	1	0	0	1	0	X	X	X	120000H to 12FFFFH	090000H to 097FFFH
	SA26	1	0	0	1	1	X	X	X	130000H to 13FFFFH	098000H to 09FFFFH
	SA27	1	0	1	0	0	X	X	X	140000H to 14FFFFH	0A0000H to 0A7FFFH
	SA28	1	0	1	0	1	X	X	X	150000H to 15FFFFH	0A8000H to 0AFFFFH
	SA29	1	0	1	1	0	X	X	X	160000H to 16FFFFH	0B0000H to 0B7FFFH
	SA30	1	0	1	1	1	X	X	X	170000H to 17FFFFH	0B8000H to 0BFFFFH
	SA31	1	1	0	0	0	X	X	X	180000H to 18FFFFH	0C0000H to 0C7FFFH
	SA32	1	1	0	0	1	X	X	X	190000H to 19FFFFH	0C8000H to 0CFFFFH
	SA33	1	1	0	1	0	X	X	X	1A0000H to 1AFFFFH	0D0000H to 0D7FFFH
	SA34	1	1	0	1	1	X	X	X	1B0000H to 1BFFFFH	0D8000H to 0DFFFFH
	SA35	1	1	1	0	0	X	X	X	1C0000H to 1CFFFFH	0E0000H to 0E7FFFH
	SA36	1	1	1	0	1	X	X	X	1D0000H to 1DFFFFH	0E8000H to 0EFFFFH
	SA37	1	1	1	1	0	X	X	X	1E0000H to 1EFFFFH	0F0000H to 0F7FFFH
	SA38	1	1	1	1	1	X	X	X	1F0000H to 1FFFFFH	0F8000H to 0FFFFFH

Sector Group Addresses (Top Boot Block)

Sector Group	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	X	X	X	SA0
SGA1	0	0	0	0	1	X	X	X	SA1 to SA3
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA2	0	0	1	X	X	X	X	X	SA4 to SA7
SGA3	0	1	0	X	X	X	X	X	SA8 to SA11
SGA4	0	1	1	X	X	X	X	X	SA12 to SA15
SGA5	1	0	0	X	X	X	X	X	SA16 to SA19
SGA6	1	0	1	X	X	X	X	X	SA20 to SA23
SGA7	1	1	0	X	X	X	X	X	SA24 to SA27
SGA8	1	1	1	0	0	X	X	X	SA28 to SA30
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA9	1	1	1	1	1	0	0	0	SA31
SGA10	1	1	1	1	1	0	0	1	SA32
SGA11	1	1	1	1	1	0	1	0	SA33
SGA12	1	1	1	1	1	0	1	1	SA34
SGA13	1	1	1	1	1	1	0	0	SA35
SGA14	1	1	1	1	1	1	0	1	SA36
SGA15	1	1	1	1	1	1	1	0	SA37
SGA16	1	1	1	1	1	1	1	1	SA38

Sector Group Addresses (Bottom Boot Block)

Sector Group	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sectors
SGA0	0	0	0	0	0	0	0	0	SA0
SGA1	0	0	0	0	0	0	0	1	SA1
SGA2	0	0	0	0	0	0	1	0	SA2
SGA3	0	0	0	0	0	0	1	1	SA3
SGA4	0	0	0	0	0	1	0	0	SA4
SGA5	0	0	0	0	0	1	0	1	SA5
SGA6	0	0	0	0	0	1	1	0	SA6
SGA7	0	0	0	0	0	1	1	1	SA7
SGA8	0	0	0	0	1	X	X	X	SA8 to SA10
	0	0	0	1	0	X	X	X	
	0	0	0	1	1	X	X	X	
SGA9	0	0	1	X	X	X	X	X	SA11 to SA14
SGA10	0	1	0	X	X	X	X	X	SA15 to SA18
SGA11	0	1	1	X	X	X	X	X	SA19 to SA22
SGA12	1	0	0	X	X	X	X	X	SA23 to SA26
SGA13	1	0	1	X	X	X	X	X	SA27 to SA30
SGA14	1	1	0	X	X	X	X	X	SA31 to SA34
SGA15	1	1	1	0	0	X	X	X	SA35 to SA37
	1	1	1	0	1	X	X	X	
	1	1	1	1	0	X	X	X	
SGA16	1	1	1	1	1	X	X	X	SA38

Flash Memory Autoselect Codes

Type			A_{12} to A_{19}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacturer's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04H
Device Code	Top Boot Block Bank Size=1	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	36H
		Word					X	2236H
	Bottom Boot Block Bank Size=1	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	39
		Word					X	2239H
	Top Boot Block Bank Size=2	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	2D
		Word					X	222DH
	Bottom Boot Block Bank Size=2	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	2E
		Word					X	222EH
	Top Boot Block Bank Size=3	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	28H
		Word					X	2228H
	Bottom Boot Block Bank Size=3	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	2BH
		Word					X	222BH
	Top Boot Block Bank Size=4	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	33H
		Word					X	2233H
	Bottom Boot Block Bank Size=4	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	35
		Word					X	2235H
Sector Group protect			Sector Group Address	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01H*2

*1: A_{-1} is for Byte mode.
*2: Output 01H at protected sector address and output 00H at unprotected sector address.

Flash Memory Command Definitions

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset (Note 1)		1	XXXH	F0H	—	—	—	—	—	—	—	—	—	—
Read/Reset (Note 1)	Word	3	555H	AAH	2AAH	55H	555H	F0H	RA	RD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Autoselect	Word	3	555H	AAH	2AAH	55H	(BA) 555H	90H	—	—	—	—	—	—
	Byte		AAAH		555H		(BA) AAAH							
Program	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Chip Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
	Byte		AAAH		555H		AAAH		AAAH		555H		AAAH	
Sector Erase	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Sector Erase Suspend		1	BA	B0H	—	—	—	—	—	—	—	—	—	—
Sector Erase Resume		1	BA	30H	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555H	AAH	2AAH	55H	555H	20H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Fast Program (Note 2)	Word	2	XXXH	A0H	PA	PD	—	—	—	—	—	—	—	—
	Byte													
Reset from Fast Mode (Note 2)	Word	2	BA	90H	XXXH	F0H (Note6)	—	—	—	—	—	—	—	—
	Byte													
Extended Sector Group Protection (Note 3)	Word	4	XXXH	60H	SPA	60H	SPA	40H	SPA	SD	—	—	—	—
	Byte													
Query (Note 4)	Word	1	55H	98H	—	—	—	—	—	—	—	—	—	—
	Byte		AAH											
Hi-ROM Entry	Word	3	555H	AAH	2AAH	55H	555H	88H	—	—	—	—	—	—
	Byte		AAAH		555H		AAAH							
Hi-ROM Program (Note 5)	Word	4	555H	AAH	2AAH	55H	555H	A0H	PA	PD	—	—	—	—
	Byte		AAAH		555H		AAAH							
Hi-ROM Erase (Note 5)	Word	6	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	HRA	30H
	Byte		AAAH		555H		AAAH		AAAH		555H			
Hi-ROM Exit (Note 5)	Word	4	555H	AAH	2AAH	55H	(HRBA) 555H	90H	XXXH	00H	—	—	—	—
	Byte		AAAH		555H		(HRBA) AAAH							

1: Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
2: This command is valid while Fast Mode.
3: This command is valid while $\overline{RESET}=V_{ID}$.
4: The valid Address is A_6 to A_0.
5: This command is valid while Hi-ROM mode.

6: The data "00H" is also acceptable.

Address bits A_{12} to A_{19} = X = “H” or “L” for all address commands except for Program Address (PA), Sector Address (SA),and Bank Address (BA).
Bus operations are defined in Table 2 "User Bus Operations".
RA = Address of the memory location to be read.
PA = Address of the memory location to be programmed.
Addresses are latched on the falling edge of the write pulse.

SA = Address of the sector to be erased. The combination of A_{19}, A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
BA = Bank address (A_{15} to A_{19})
SPA = Sector group address to be protected. Set sector group address (SGA) and (A_6, A_1, A_0) = (0, 1, 0).
HRA= Address of the Hidden-ROM area.

Top Boot Block	Word mode:	0F8000H to 0FFFFFH
	Byte mode:	1F0000H to 1FFFFFH
Bottom Boot Block	Word mode:	000000H to 007FFFH
	Byte mode:	000000H to 00FFFFH

HRBA = Bank address of the Hidden-ROM area.
Top Boot Block : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 1$
Bottom Boot Block : $A_{15} = A_{16} = A_{17} = A_{18} = A_{19} = A_{20} = 0$
RD = Data read from location RA during read operation.
PD = Data to be programmed at location PA.
SD = Sector protection verify data. Output 01H at protected sector addresses and output 00H at unprotectedsector addresses.

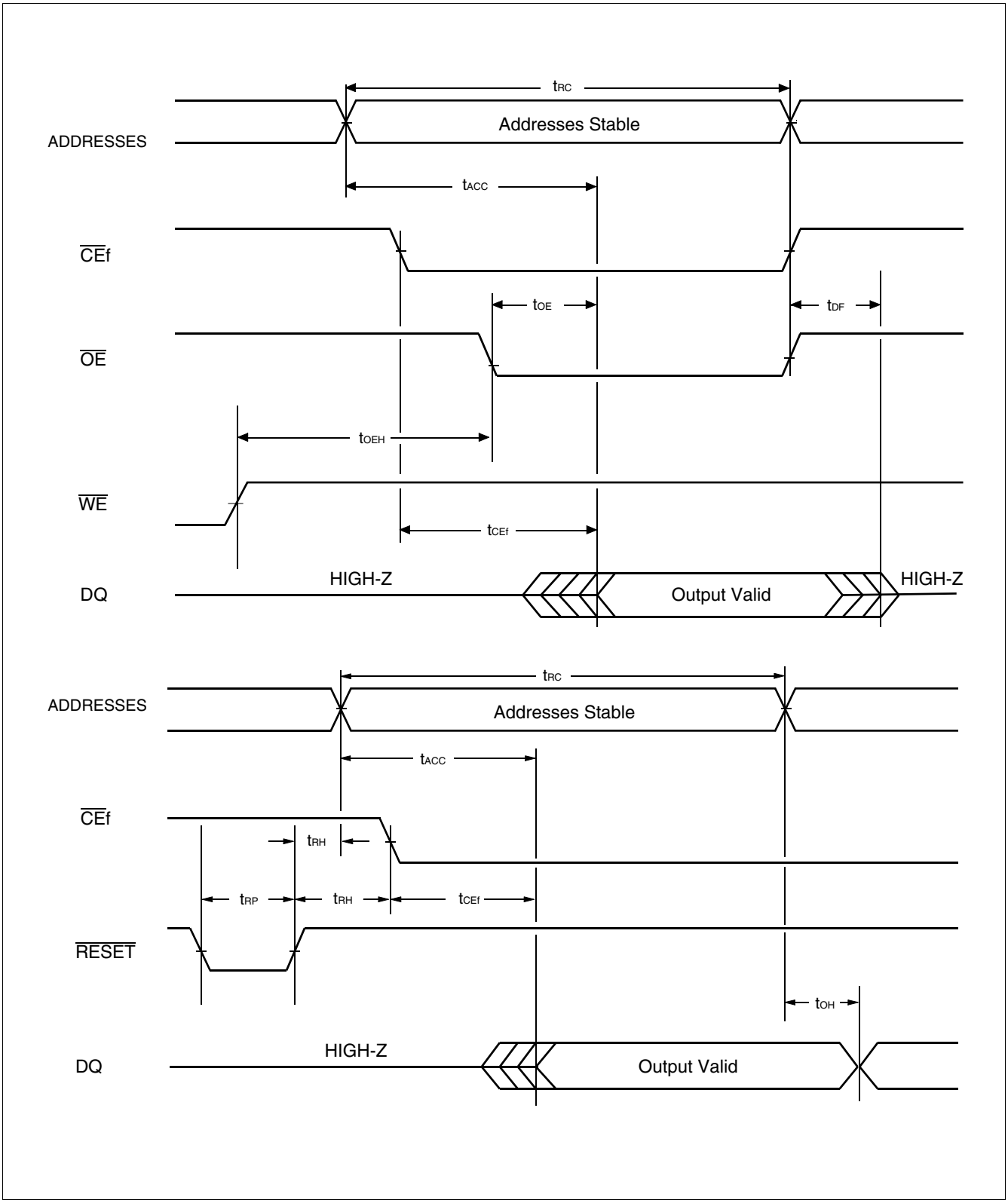
The system should generate the following address patterns;
Word mode: 555H or 2AAH to addresses A_{10} to A_0
Byte mode : AAAH or 555H to addresses A_{10} to A_0 and A_{-1}

- **Read Only Operations Characteristics (Flash)**

Parameter Symbols		Description	Test Setup	Value (Note)		Unit
JEDEC	Standard			Min.	Max.	
t_{AVAV}	t_{RC}	Read Cycle Time	—	70	—	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}f = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	ns
t_{ELQV}	$t_{CE}f$	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	—	70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	—	—	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z	—	—	25	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z	—	—	25	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}f$ or $\overline{OE}$, Whichever Occurs First	—	0	—	ns
—	t_{READY}	$\overline{RESET}$ Pin Low to Read Mode	—	—	20	µs

Note: Test Conditions–Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to 3.0 V
Timing measurement reference level
Input: 1.5 V
Output: 1.5 V

- **Read Cycle (Flash)**

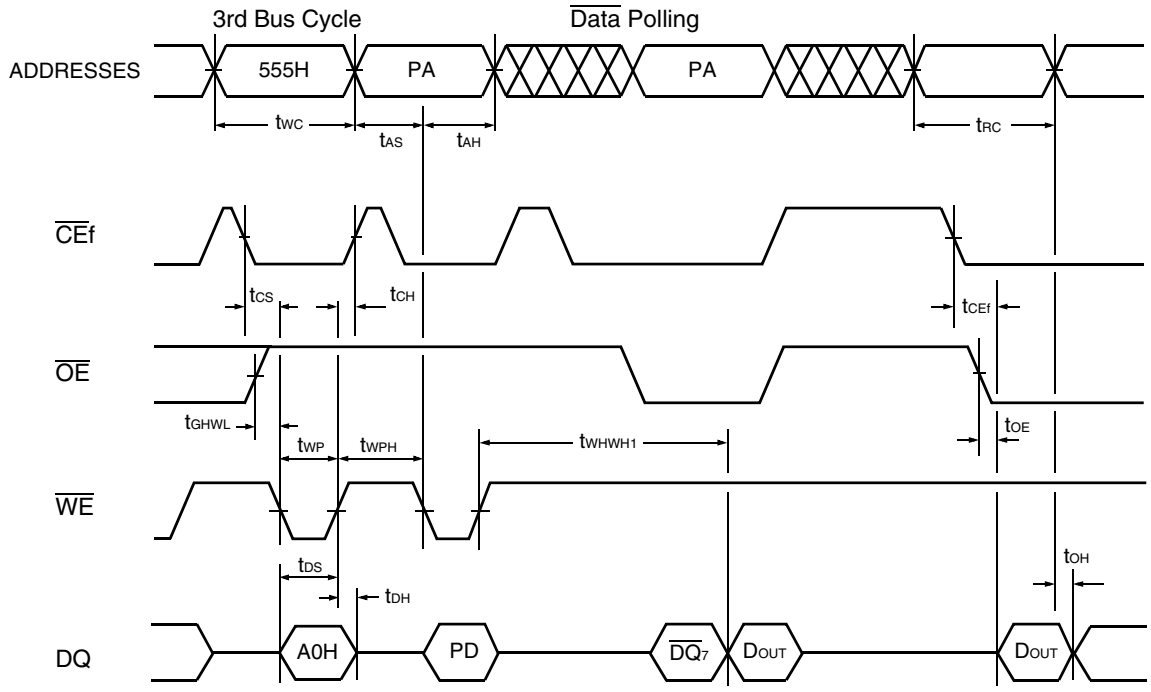


• **Erase/Program Operations (Flash)**

Parameter Symbols		Description		Value			Unit
JEDEC	Standard			Min.	Typ.	Max.	
t_{AVAV}	t_{WC}	Write Cycle Time		70	—	—	ns
t_{AVWL}	t_{AS}	Address Setup Time ($\overline{WE}$ to Addr.)		0	—	—	ns
—	t_{ASO}	Address Setup Time to $\overline{CE}$f Low During Toggle Bit Polling		12	—	—	ns
t_{WLAX}	t_{AH}	Address Hold Time ($\overline{WE}$ to Addr.)		45	—	—	ns
—	t_{AHT}	Address Hold Time from $\overline{CE}$f or $\overline{OE}$ High During Toggle Bit Polling		0	—	—	ns
t_{DVWH}	t_{DS}	Data Setup Time		30	—	—	ns
t_{WHDX}	t_{DH}	Data Hold Time		0	—	—	ns
—	t_{OES}	Output Enable Setup Time		0	—	—	ns
—	t_{OEH}	Output Enable Hold Time	Read	0	—	—	ns
			Toggle and $\overline{Data}$ Polling	10	—	—	ns
—	t_{CEPH}	$\overline{CE}$f High During Toggle Bit Polling		20	—	—	ns
—	t_{OEPH}	$\overline{OE}$ High During Toggle Bit Polling		20	—	—	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{CE}$f)		0	—	—	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write ($\overline{OE}$ to $\overline{WE}$)		0	—	—	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{ELWL}	t_{CS}	$\overline{CE}$f Setup Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time ($\overline{CE}$f to $\overline{WE}$)		0	—	—	ns
t_{WHEH}	t_{CH}	$\overline{CE}$f Hold Time ($\overline{WE}$ to $\overline{CE}$f)		0	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width		35	—	—	ns
t_{ELEH}	t_{CP}	$\overline{CE}$f Pulse Width		35	—	—	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		25	—	—	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$f Pulse Width High		25	—	—	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		—	8	—	µs
		Word Programming Operation		—	16	—	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 1)		—	1	—	sec
—	t_{VCS}	V_{CC}f Setup Time		50	—	—	µs
—	t_{VLHT}	Voltage Transition Time (Note 2)		4	—	—	µs
—	t_{VIDR}	Rise Time to V_{ID} (Note 2)		500	—	—	ns
—	t_{VACCR}	Rise Time to V_{ACC}		500	—	—	ns
—	t_{RB}	Recover Time from RY/$\overline{BY}$		0	—	—	ns
—	t_{RP}	$\overline{RESET}$ Pulse Width		500	—	—	ns
—	t_{EOE}	Delay Time from Embedded Output Enable		—	—	70	ns
—	t_{RH}	$\overline{RESET}$ Hold Time Before Read		200	—	—	ns
—	t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay		—	—	90	ns
—	t_{TOW}	Erase Time-out Time (Note 3)		50	—	—	µs
—	t_{SPD}	Erase Suspend Transition Time (Note 4)		—	—	20	µs

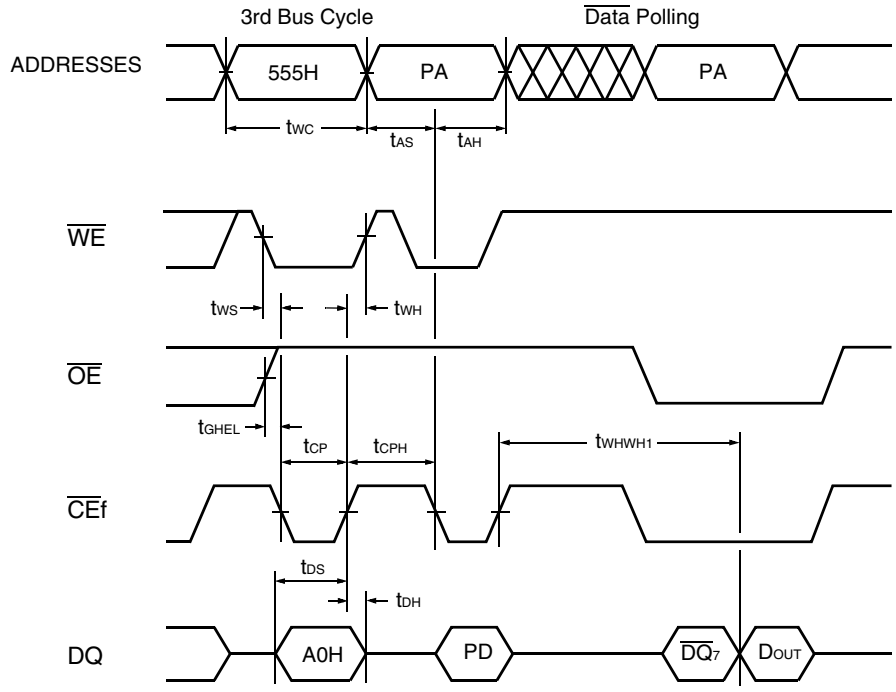
Notes: 1. This does not include the preprogramming time.
2. This timing is for Sector Protection Operation.
3. The time between writes must be less than "t_{TOW}" otherwise that command will not be accepted and erasure will start. A time-out or "t_{TOW}" from the rising edge of last $\overline{CE}$f or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s).
4. When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of "t_{SPD}" to suspend the erase operation.

- **Write Cycle ($\overline{WE}$ control) (Flash)**



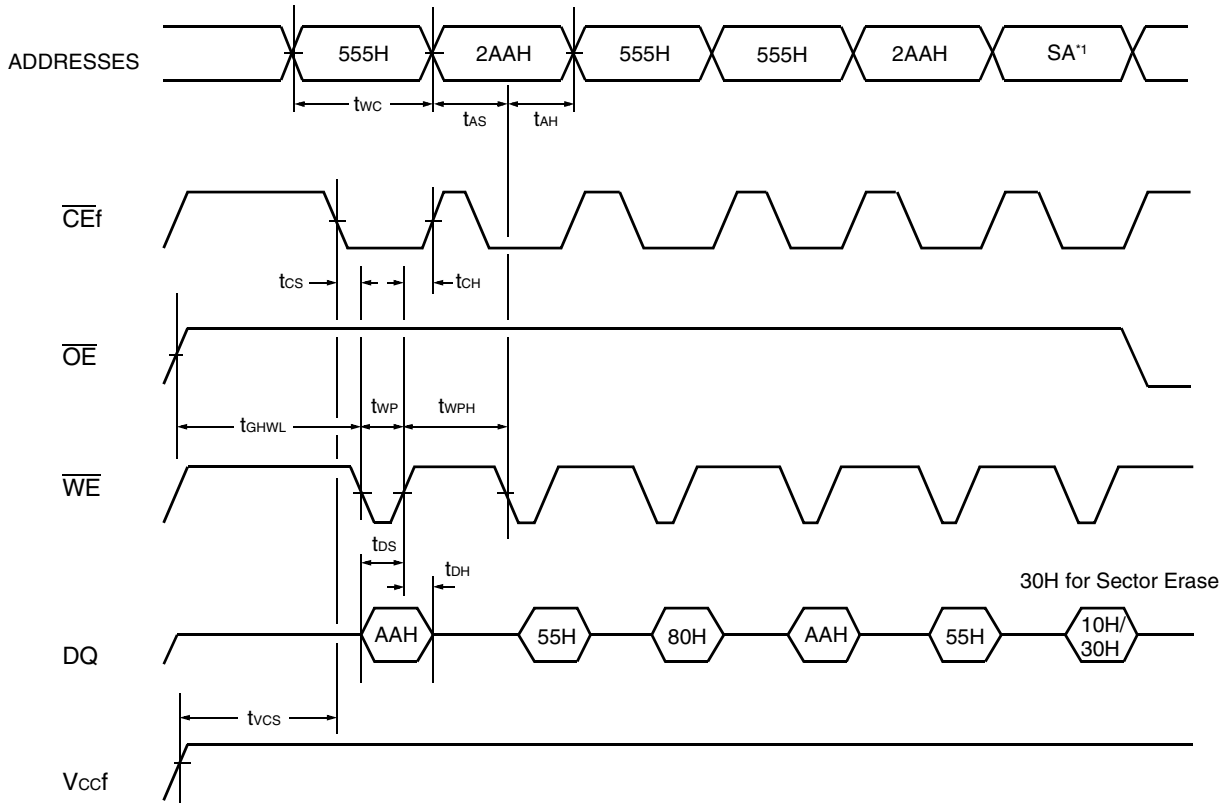
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ_7}$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

- **Write Cycle ($\overline{CE}$f control) (Flash)**



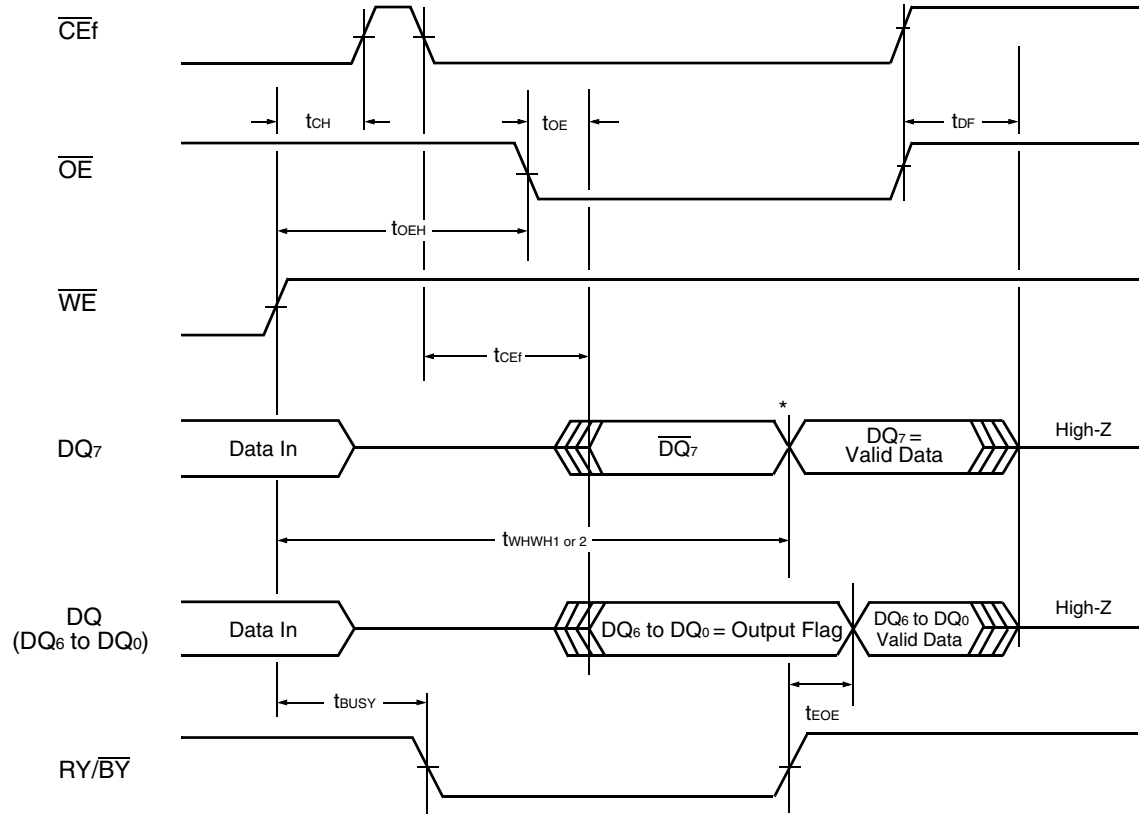
Notes: 1. PA is address of the memory location to be programmed.
2. PD is data to be programmed at byte address.
3. $\overline{DQ}_7$ is the output of the complement of the data written to the device.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles out of four bus cycle sequence.
6. These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

- **AC Waveforms Chip/Sector Erase Operations (Flash)**



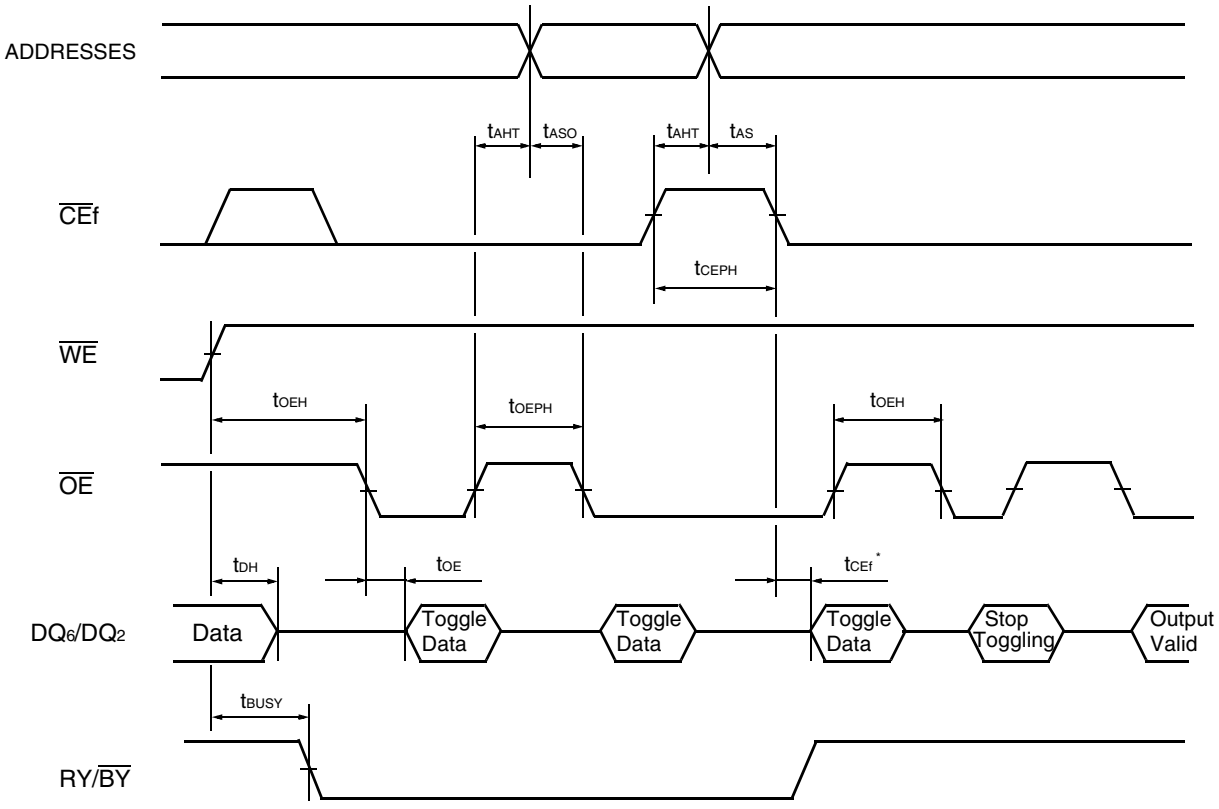
Notes: 1. SA is the sector address for Sector Erase. Addresses = 555H for Chip Erase.
2. These waveform are for the ×16 mode. (The addresses differ from ×8 mode.)

- **AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations (Flash)**



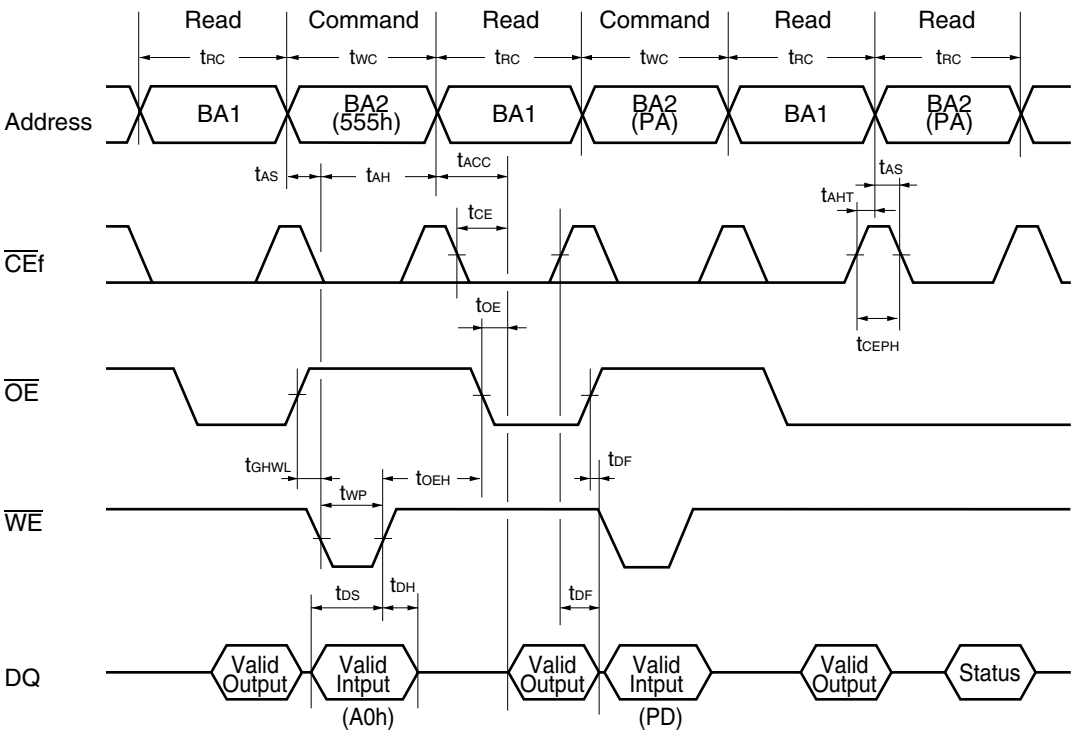
*DQ_7 = Valid Data (The device has completed the Embedded operation.)

- **AC Waveforms for Toggle Bit during Embedded Algorithm Operations (Flash)**



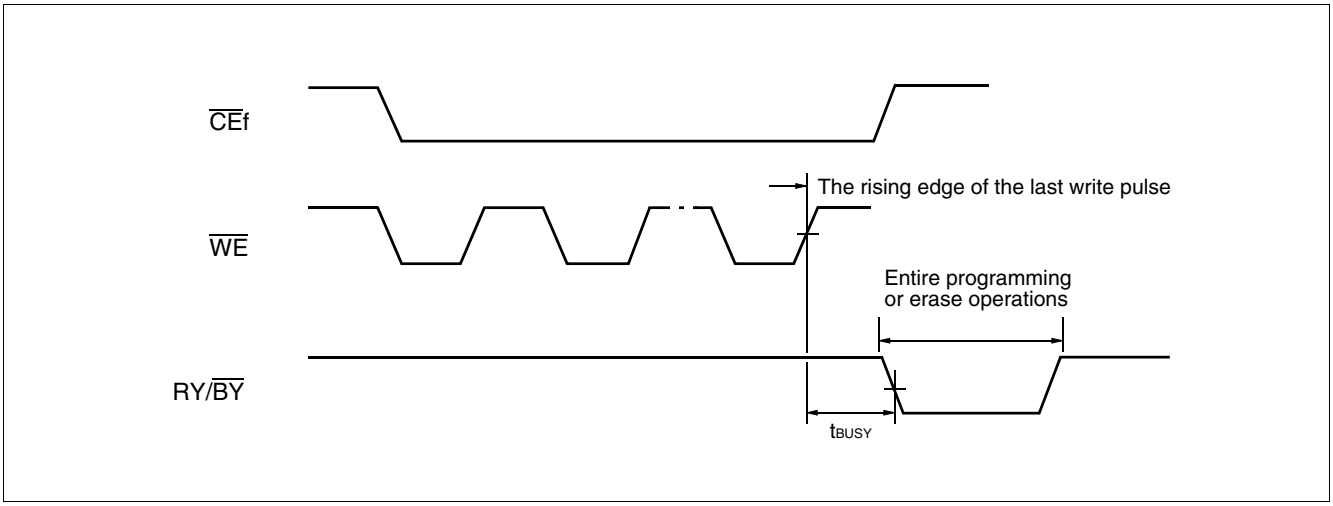
* : DQ_6 stops toggling (The device has completed the Embedded operation).

- **Back-to-back Read/Write Timing Diagram (Flash)**

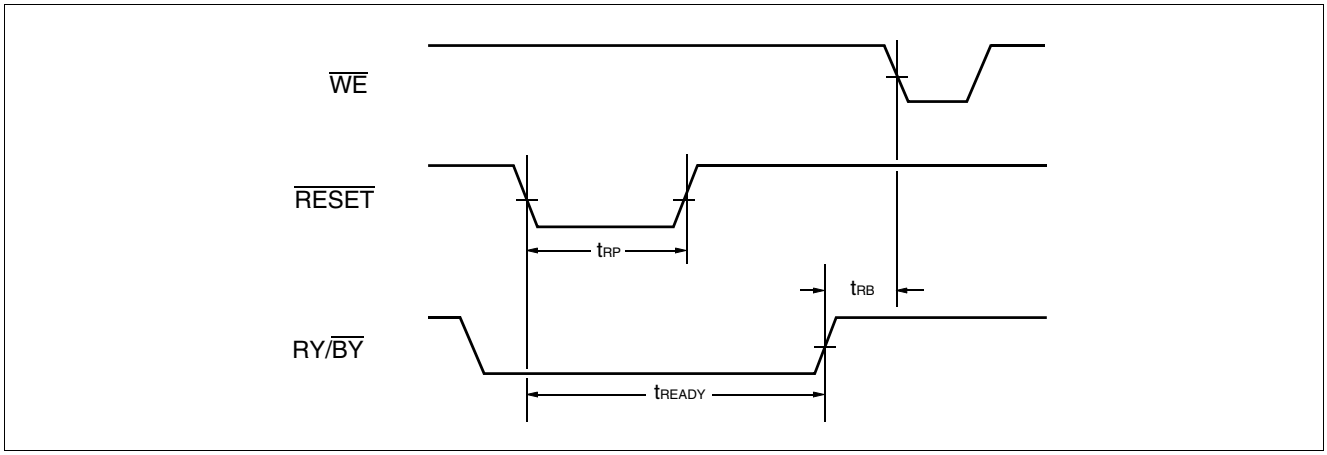


Note: This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address of Bank 1.
BA2: Address of Bank 2.

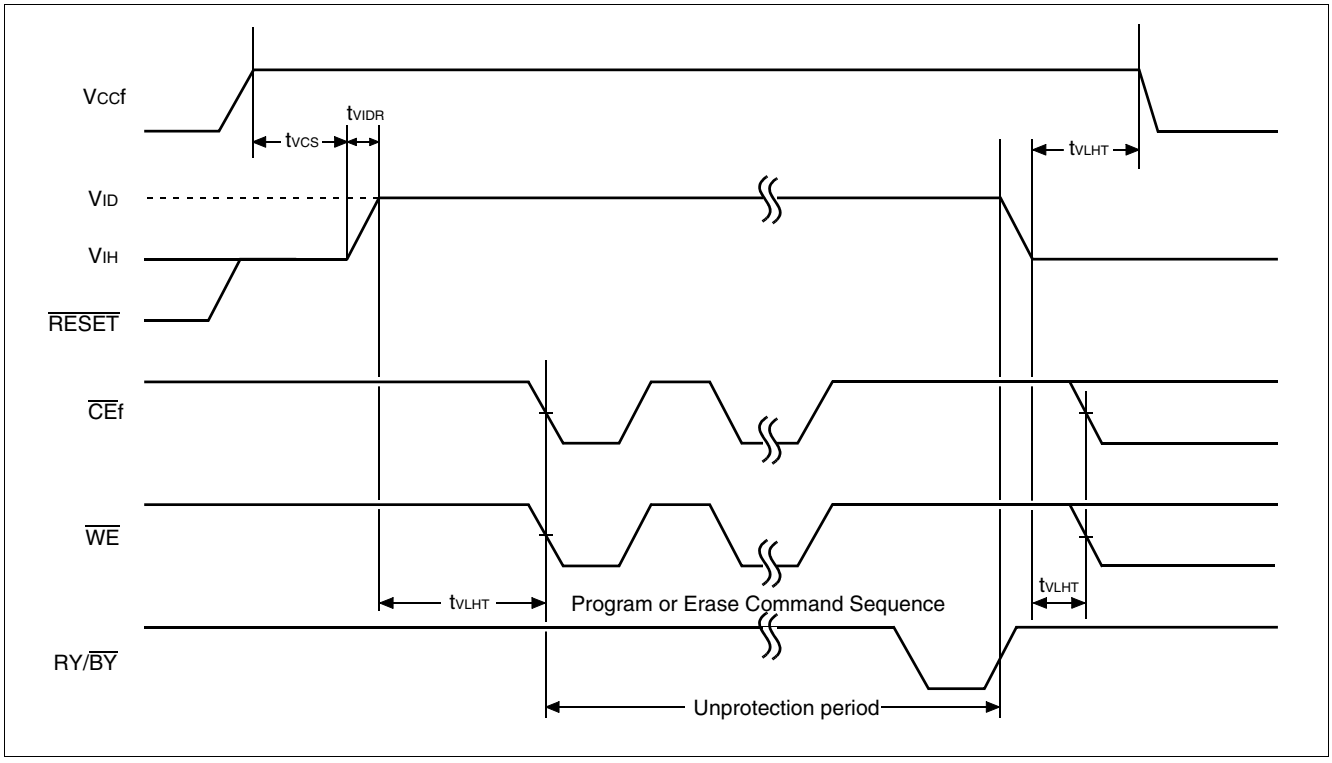
- **RY/$\overline{BY}$ Timing Diagram during Write/Erase Operations (Flash)**



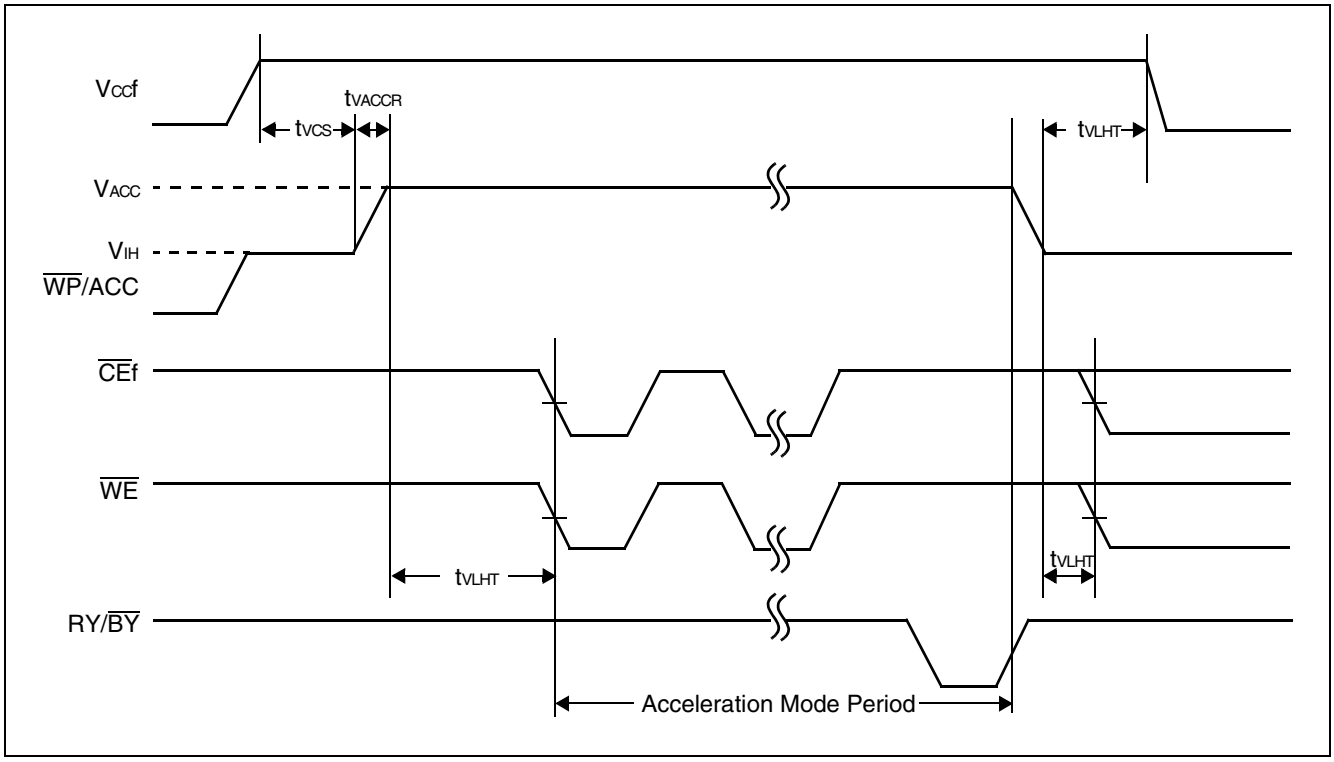
- **$\overline{RESET}$, RY/$\overline{BY}$ Timing Diagram (Flash)**



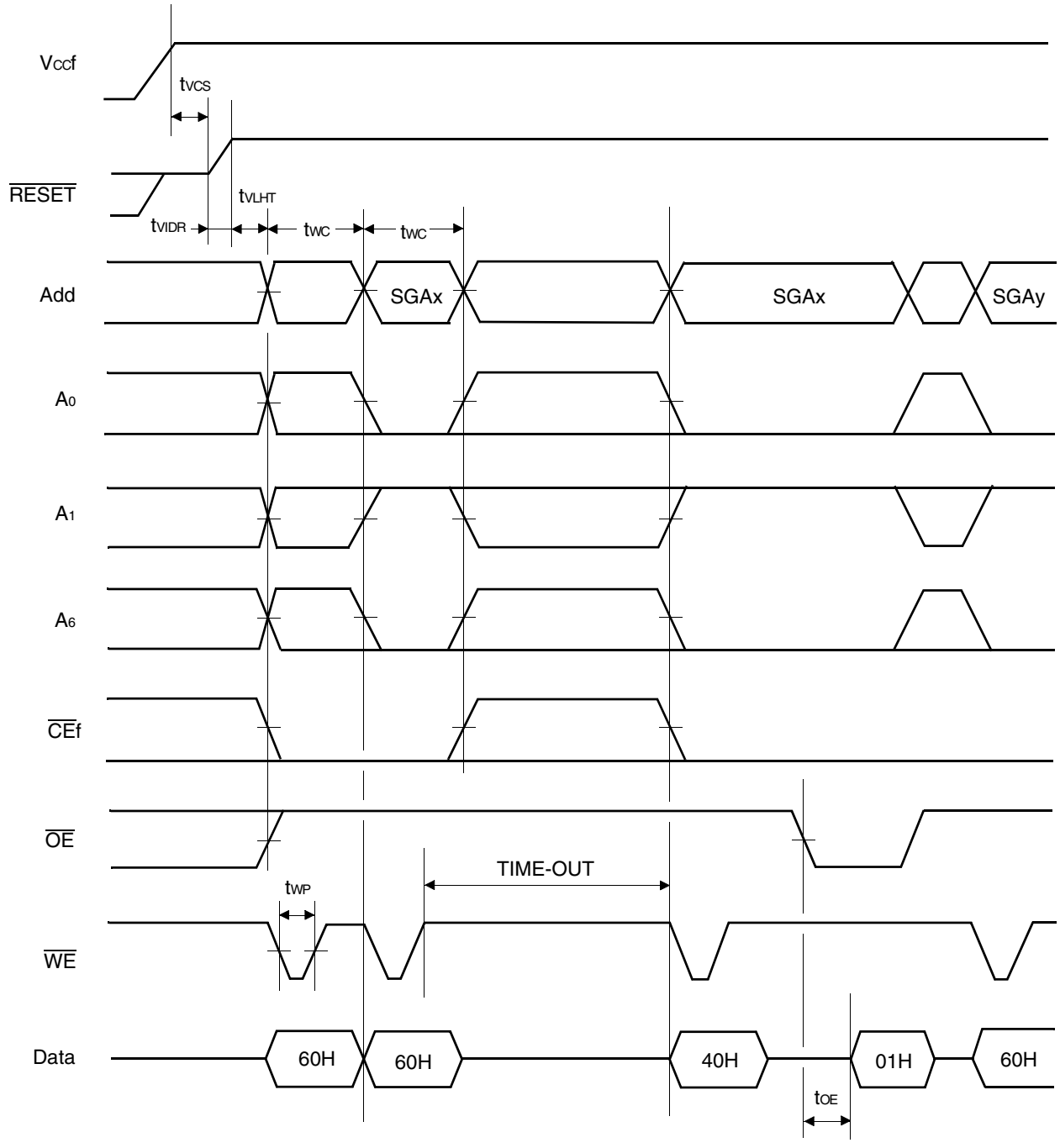
- **Temporary Sector Unprotection (Flash)**



- **Acceleration Mode Timing Diagram (Flash)**



- **Extended Sector Protection (Flash)**



SGAx : Sector Group Address to be protected
SGAy : Next Group Sector Address to be protected
TIME-OUT : Time-Out window = 250 μs (min)

■ ERASE AND PROGRAMMING PERFORMANCE (Flash)

Parameter	Limits			Unit	Comment
	Min.	Typ.	Max.		
Sector Erase Time	—	1	10	sec	Excludes programming time prior to erasure
Byte Programming Time	—	8	300	µs	Excludes system-level overhead
Word Programming Time	—	16	360	µs	Excludes system-level overhead
Chip Programming Time	—	—	50	sec	Excludes system-level overhead
Erase/Program Cycle	100,000	—	—	cycles	

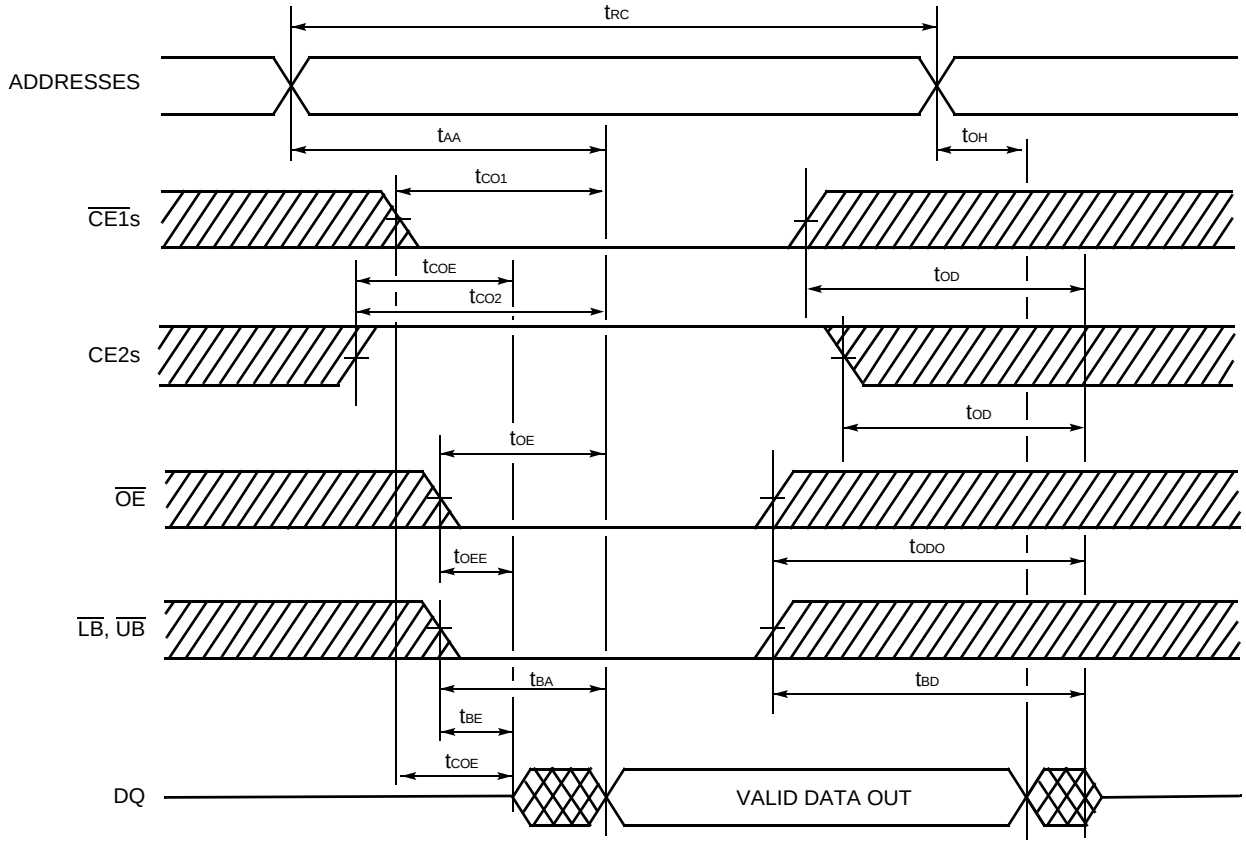
- **Read Cycle (SRAM)**

Parameter	Symbol	Value		Unit
		Min.	Max.	
Read Cycle Time	t_{RC}	70	—	ns
Address Access Time	t_{AA}	—	70	ns
Chip Enable ($\overline{CE1}$s) Access Time	t_{CO1}	—	70	ns
Chip Enable (CE2s) Access Time	t_{CO2}	—	70	ns
Output Enable Access Time	t_{OE}	—	35	ns
$\overline{LB}$, $\overline{UB}$ to Output Valid	t_{BA}	—	70	ns
Chip Enable ($\overline{CE1}$s Low and CE2s High) to Output Active	t_{COE}	5	—	ns
Output Enable Low to Output Active	t_{OEE}	0	—	ns
$\overline{UB}$, $\overline{LB}$ Enable Low to Output Active	t_{BE}	0	—	ns
Chip Enable ($\overline{CE1}$s High or CE2s Low) to Output High-Z	t_{OD}	—	25	ns
Output Enable High to Output High-Z	t_{ODO}	—	25	ns
$\overline{UB}$, $\overline{LB}$ Output Enable to Output High-Z	t_{BD}	—	25	ns
Output Data Hold Time	t_{OH}	10	—	ns

Note: Test Conditions– Output Load:1 TTL gate and 30 pF
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V to V_{CC}s
Timing measurement reference level
Input: 0.5×V_{CC}s
Output: 0.5×V_{CC}s

4M SRAM for MCP

- **Read Cycle (SRAM)**

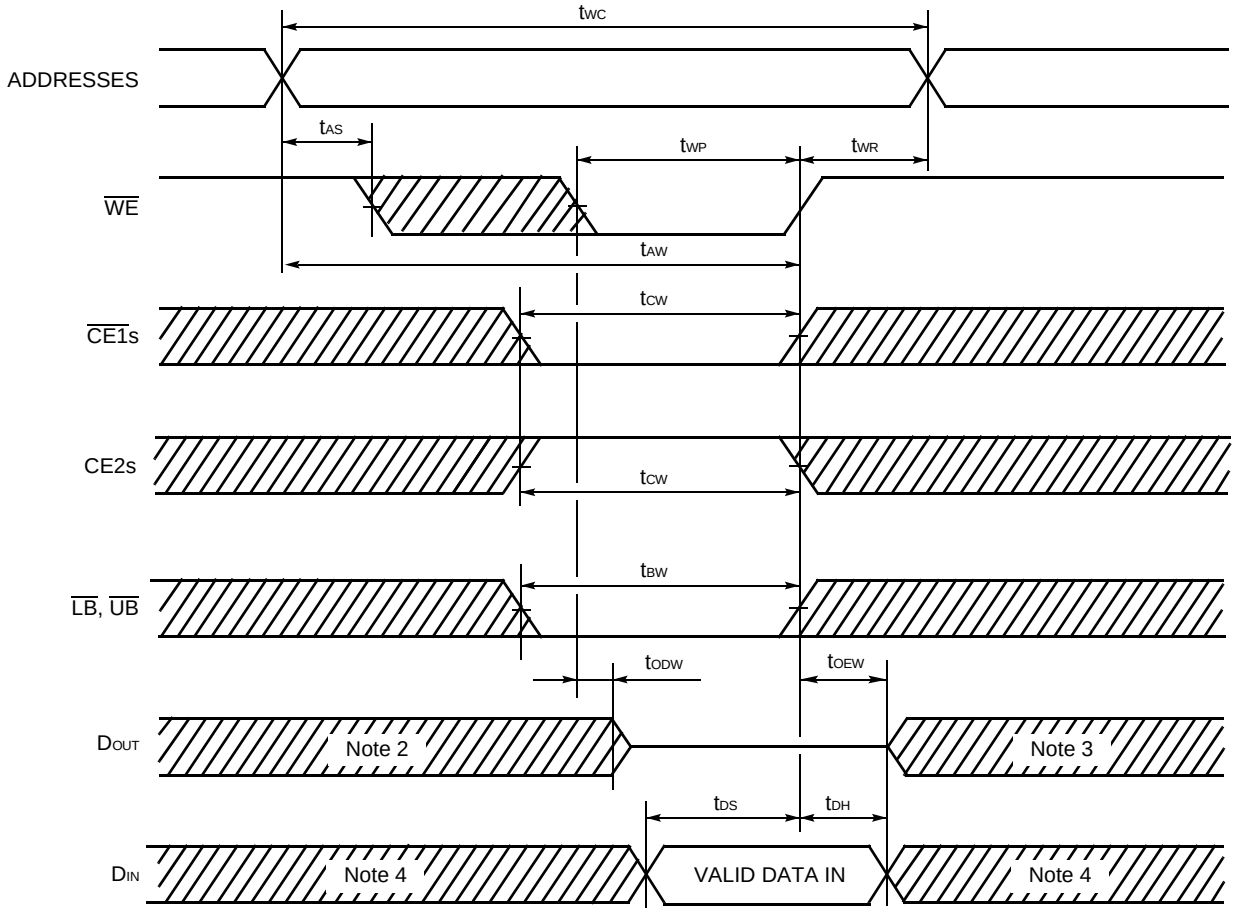


Note: $\overline{WE}$ remains HIGH for the read cycle.

- **Write Cycle (SRAM)**

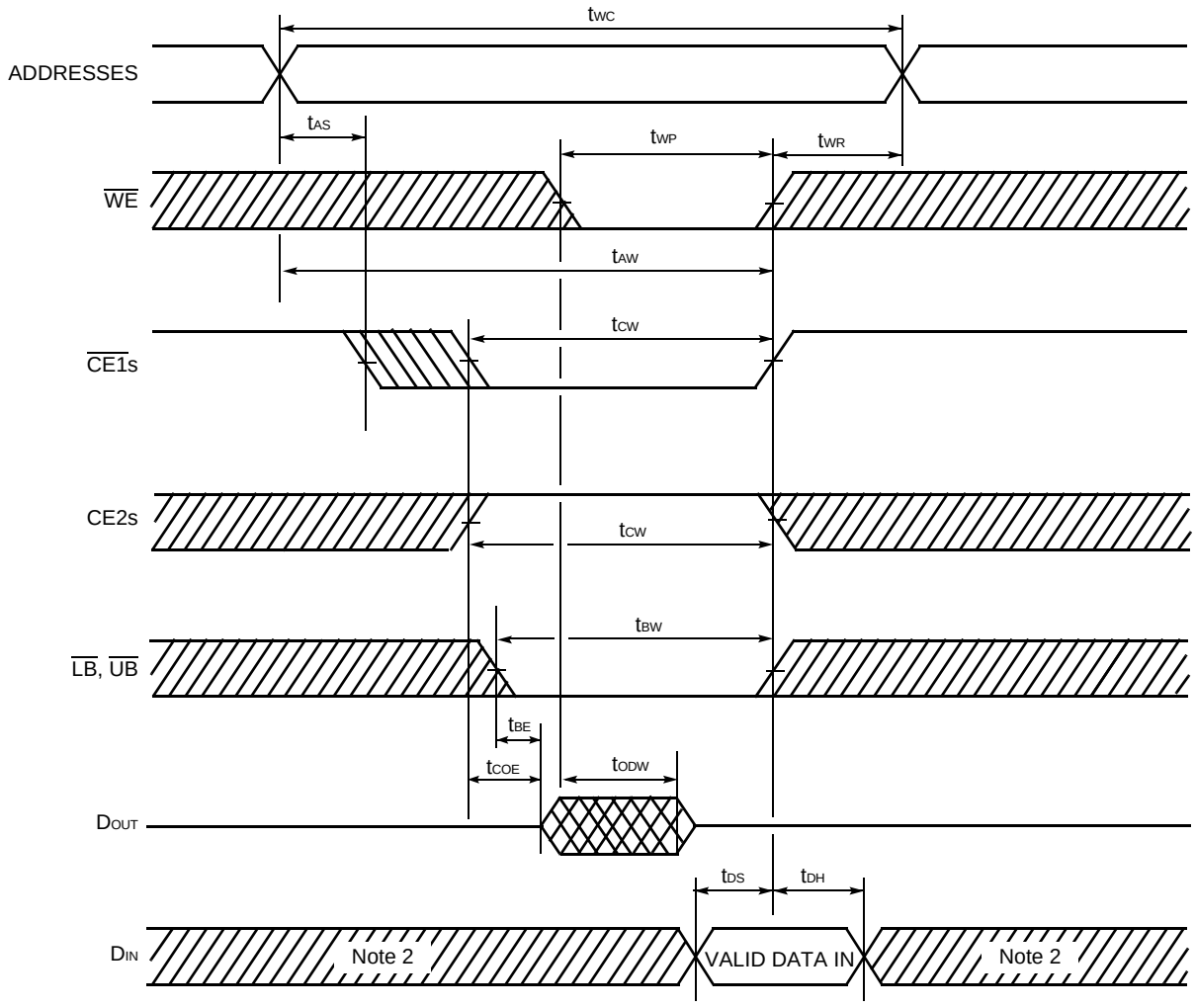
Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	70	—	ns
Write Pulse Width	t_{WP}	50	—	ns
Chip Enable to End of Write	t_{CW}	55	—	ns
Address valid to End of Write	t_{AW}	55	—	ns
$\overline{UB}$, $\overline{LB}$ to End of Write	t_{BW}	55	—	ns
Address Setup Time	t_{AS}	0	—	ns
Write Recovery Time	t_{WR}	0	—	ns
$\overline{WE}$ Low to Output High-Z	t_{ODW}	—	25	ns
$\overline{WE}$ High to Output Active	t_{OEW}	0	—	ns
Data Setup Time	t_{DS}	30	—	ns
Data Hold Time	t_{DH}	0	—	ns

- **Write Cycle (Note 1) ($\overline{WE}$ control) (SRAM)**



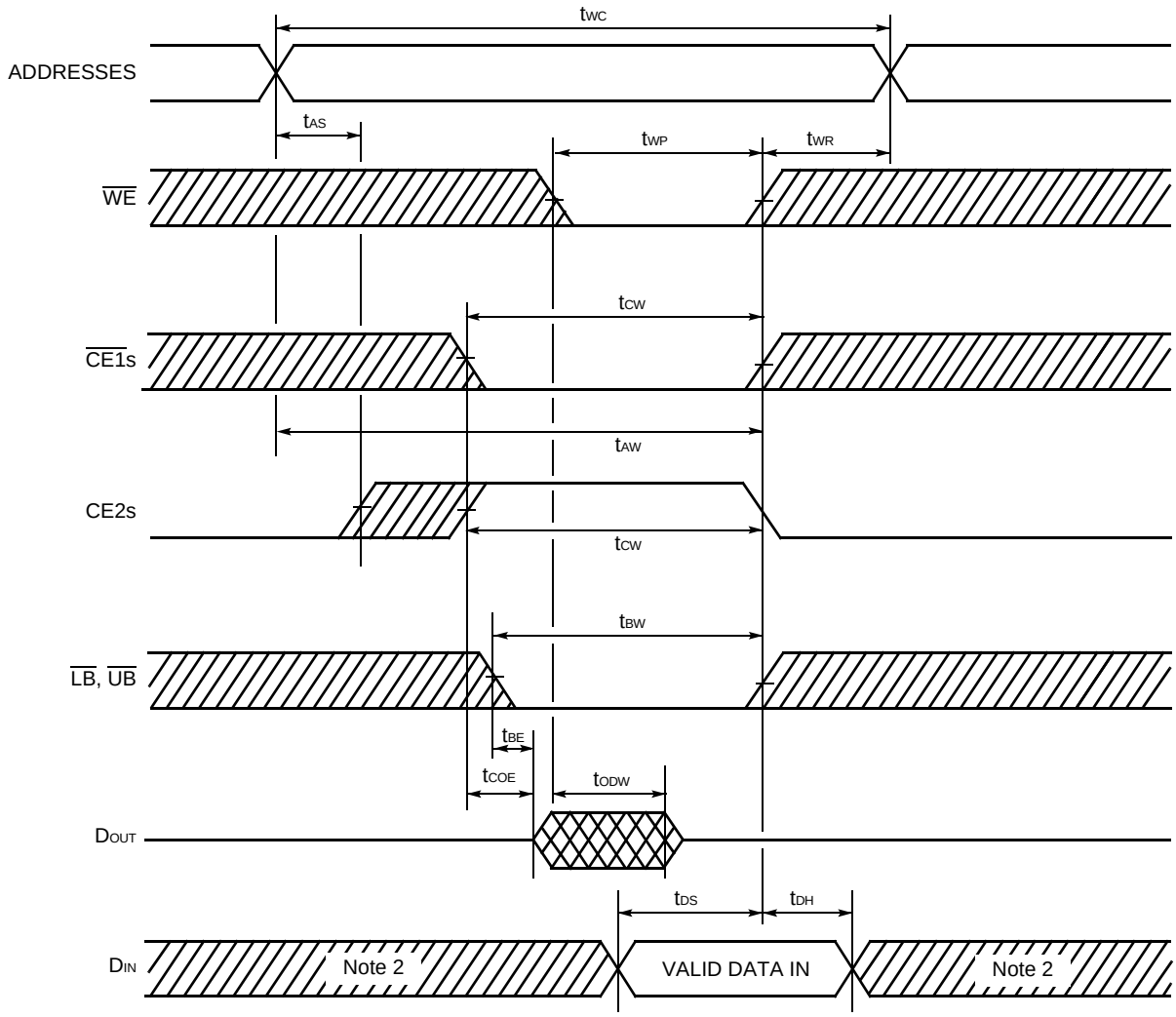
Note 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. If $\overline{CE1}$s goes LOW (or CE2s goes HIGH) coincident with or after $\overline{WE}$ goes LOW, the output will remain at high impedance.
3. If $\overline{CE1}$s goes HIGH (or CE2s goes LOW) coincident with or before $\overline{WE}$ goes HIGH, the output will remain at high impedance.
4. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) ($\overline{CE1}$s control) (SRAM)**



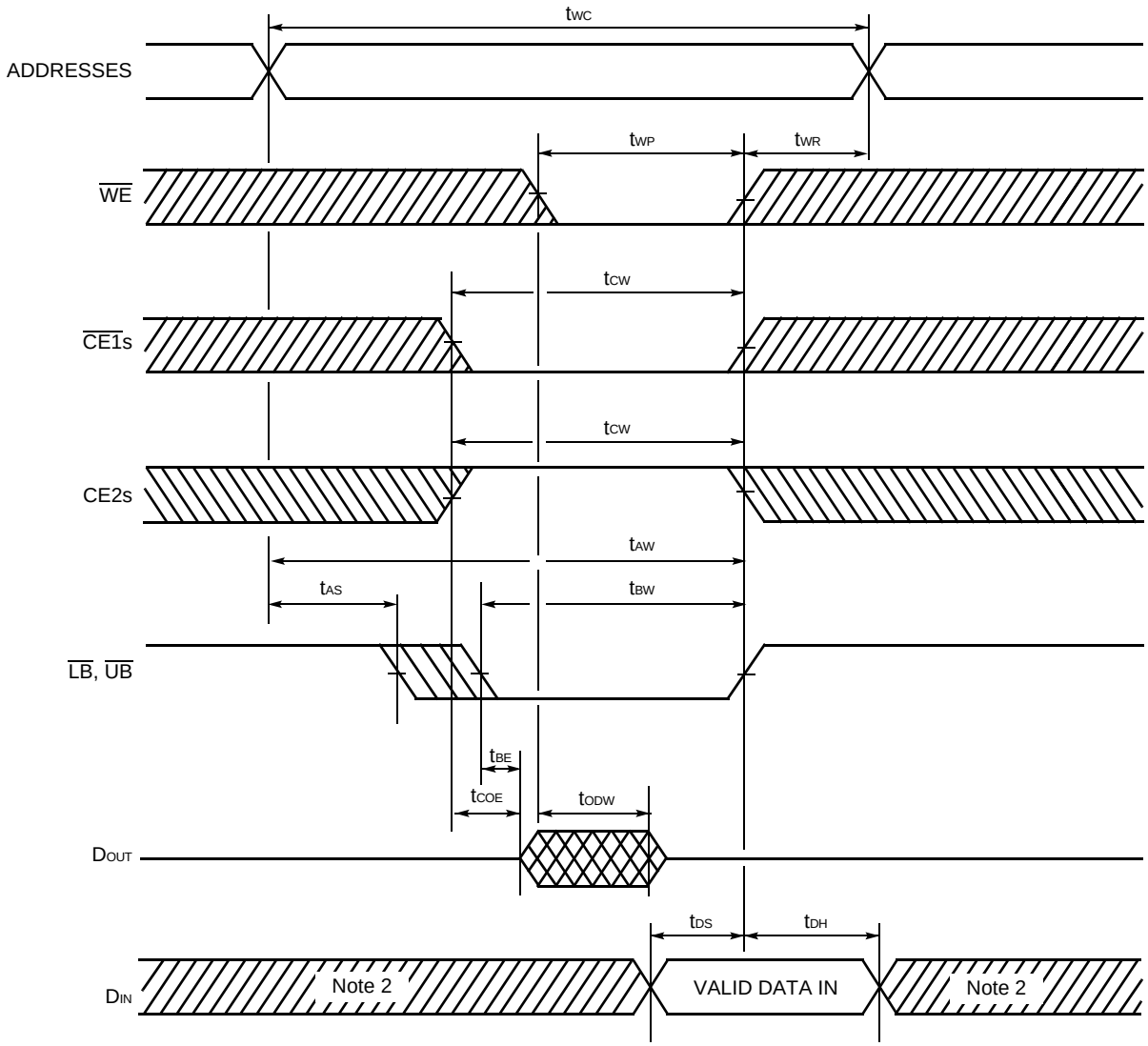
Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) (CE2s Control) (SRAM)**



Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

- **Write Cycle (Note 1) ($\overline{LB}$, $\overline{UB}$ Control) (SRAM)**



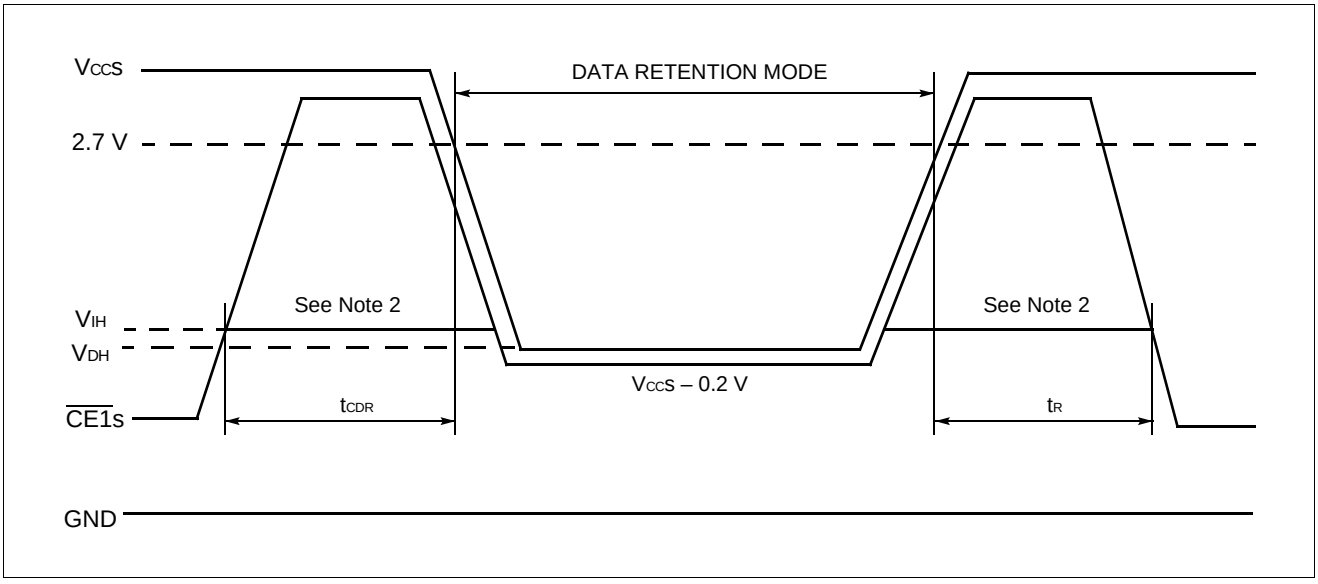
Notes: 1. If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.
2. Because I/O signals may be in the output state at this Time, input signals of reverse polarity must not be applied.

■ DATA RETENTION CHARACTERISTICS (SRAM)

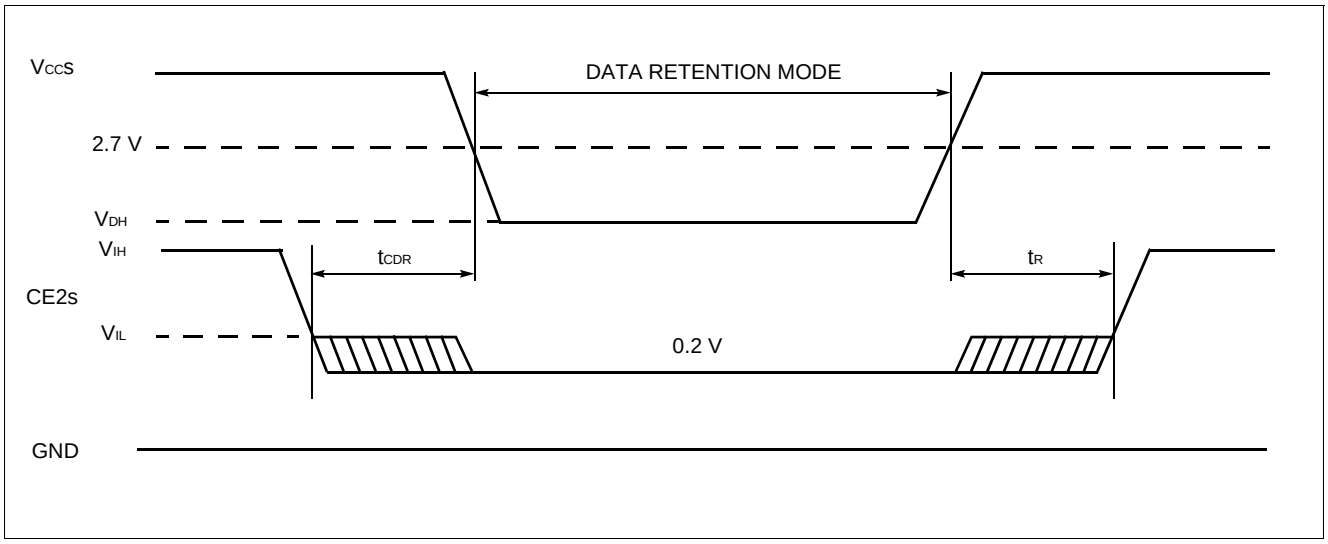
Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Data Retention Supply Voltage		V_{DH}	1.5	—	3.1	V
Standby Current	V_{DH} = 3.0 V	I_{DDS2}	—	—	15	µA
Chip Deselect to Data Retention Mode Time		t_{CDR}	0	—	—	ns
Recovery Time		t_R	t_{RC}	—	—	ns

Note t_{RC}: Read cycle time

- **$\overline{CE1}$s Controlled Data Retention Mode (Note 1)**



- **CE2s Controlled Data Retention Mode (Note 3)**



Notes: 1. In $\overline{CE1}$s controlled data retention mode, input level of CE2s should be fixed Vccs to Vccs–0.2 V or Vss to 0.2 V during data retention mode. Other input and input/output pins can be used between –0.3 V to Vccs+0.3 V.

2. When $\overline{CE1}$s is operating at the V_{IH} Min. level, the standby current is given by I_{SB1}s during the transition of V_{CC}s from V_{CC}s MAX to V_{IH} Min. level.
3. In CE2s controlled data retention mode, input and input/output pins can be used between –0.3 V to Vccs+0.3V.

■ PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	11	14	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	12	16	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	14	16	pF
C_{IN3}	$\overline{WP}$/ACC Pin Capacitance	V_{IN} = 0	17	20	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

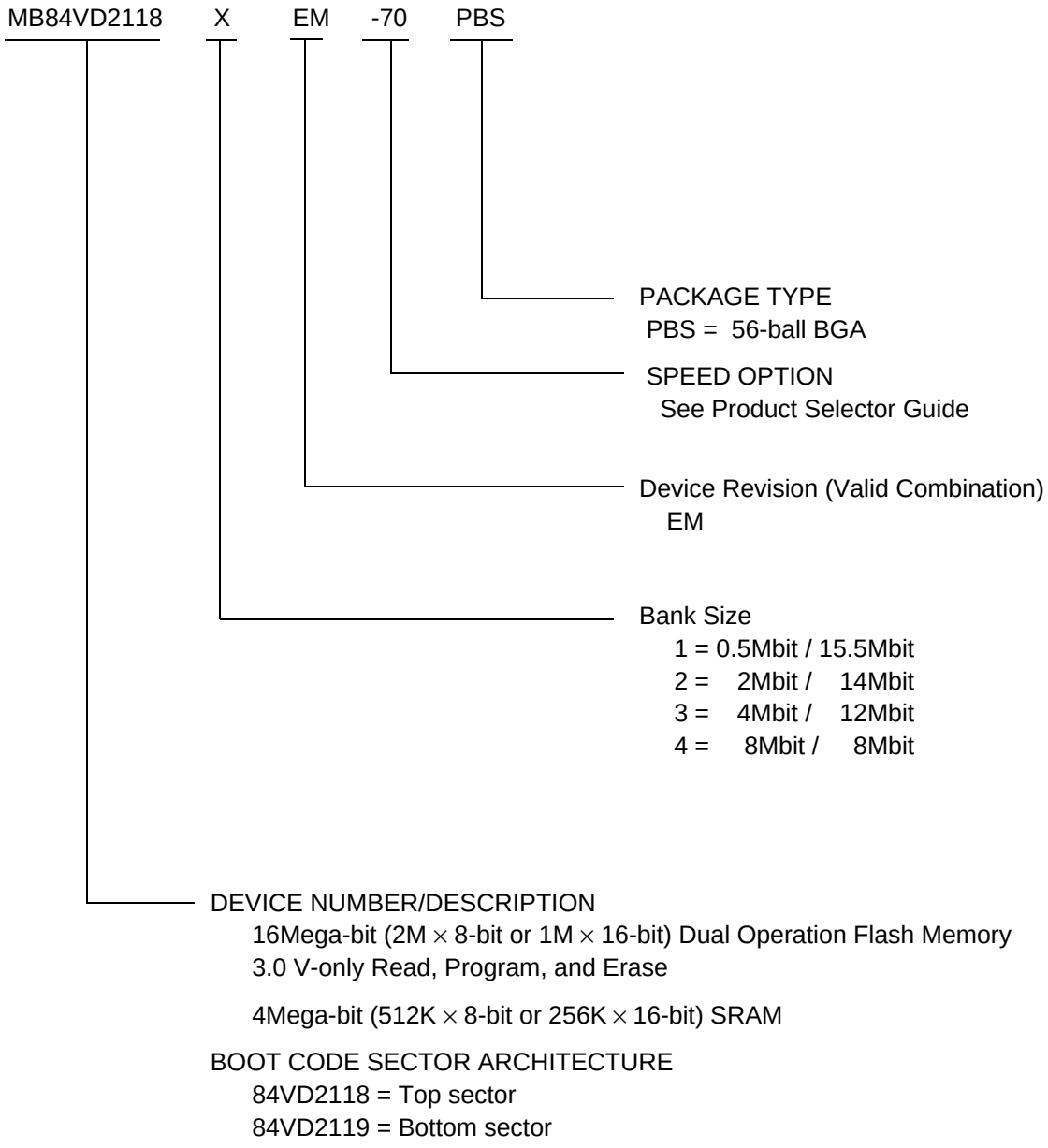
■ HANDLING OF PACKAGE

Please handle this package carefully since the sides of package create acute angles.

■ CAUTION

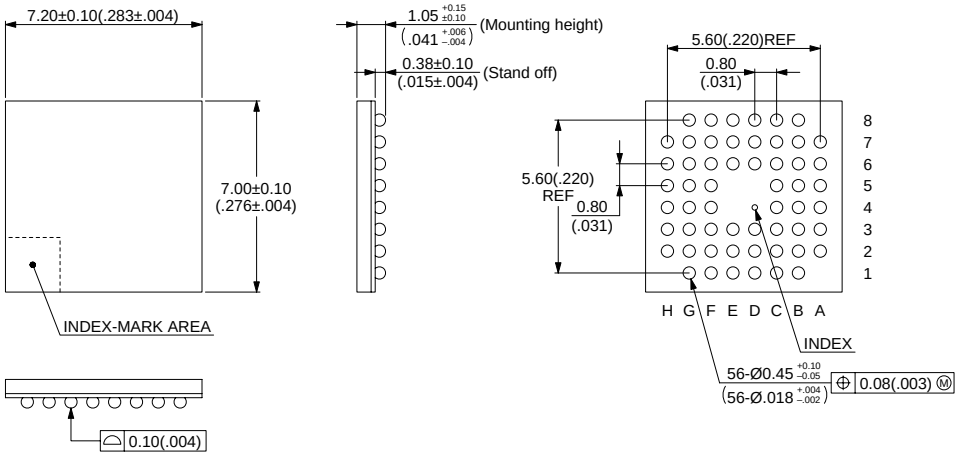
- The high voltage (V_{ID}) cannot apply to address pins and control pins except $\overline{RESET}$.
  Exception is when autoselect and sector group protect function are used, then the high voltage (V_{ID}) can be applied to $\overline{RESET}$.
- Without the high voltage (V_{ID}) , sector group protection can be achieved by using “Extended Sector Group Protection” command.

■ ORDERING INFORMATION



■ PACKAGE DIMENSIONS

56-pin plastic FBGA
(BGA-56P-M02)



Dimension in mm.

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F0206

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