

## Monolithic Quad SPST CMOS Analog Switches

### Features

- $\pm 15\text{-V}$  Input Range
- Low Off Leakage— $I_{D(on)}$ : 0.1 nA
- Low On-Resistance— $r_{DS(on)}$ : 115  $\Omega$
- 44-V Maximum Supply Ratings
- TTL and CMOS Compatible

### Benefits

- Wide Input Range
- Low Distortion Switching
- Can Be Driven from Comparators or Op Amps Without Limiting Resistors

### Applications

- Disk Drives
- Radar Systems
- Communications Systems
- Sample-and-Hold

### Description

The DG201A and DG202 are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. When combining a low on-resistance and a wide signal range ( $\pm 15\text{ V}$ ) with low charge-transfer these devices are well suited for industrial and military applications.

Built on Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch

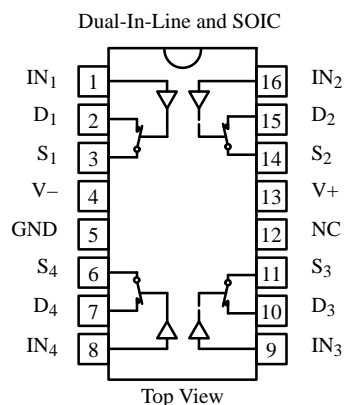
conducts equally well in both directions when on. When off these switches will block up to 30 V peak-to-peak and have a 44-V absolute maximum power supply rating.

These two devices are differentiated by the type of switch actions (See Truth Table).

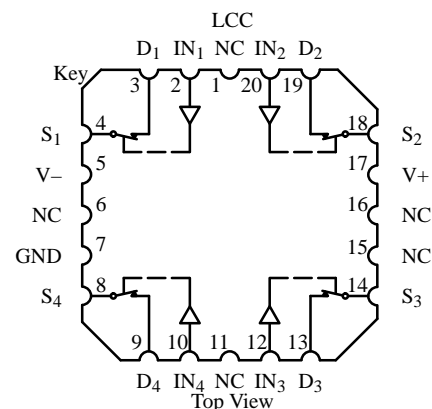
The DG201B/DG202B upgrades are recommended for new designs.

### Functional Block Diagram and Pin Configuration

#### DG201A



#### DG201A



#### Truth Table

Logic	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0"  $\leq 0.8\text{ V}$   
 Logic "1"  $\geq 2.4\text{ V}$

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70036.

## Ordering Information

Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG201ACJ
		DG202CJ
-25 to 85°C	16-Pin CerDIP	DG201ABK
-40 to 85°C	16-Pin Narrow SOIC	DG201ADY
-55 to 125°C	16-Pin CerDIP	DG201AAK
		DG201AAK/883, JM38510/12302BEA
		7705301EA
		DG202AK
		DG202AK/883
-55 to 125°C	16-Pin Sidebrazed	JM38510/12302BEC
		7705301EC
	LCC-20	77053012A

## Absolute Maximum Ratings

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs<sup>a</sup> V<sub>S</sub>, V<sub>D</sub> ..... (V-) -2 V to (V+) +2 V  
or 20 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D  
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (K, Z Suffix) ..... -65 to 150°C  
(J, Y Suffix) ..... -65 to 125°C

Power Dissipation (Package)<sup>b</sup>

16-Pin Plastic DIP<sup>c</sup> ..... 470 mW

16-Pin SOIC<sup>d</sup> ..... 640 mW

16-Pin CerDIP and Sidebrazed<sup>e</sup> ..... 900 mW

LCC-20<sup>f</sup> ..... 750 mW

Notes:

- Signals on S<sub>X</sub>, D<sub>X</sub>, or IN<sub>X</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 25°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C
- Derate 10 mW/°C above 75°C

## Schematic Diagram (Typical Channel)

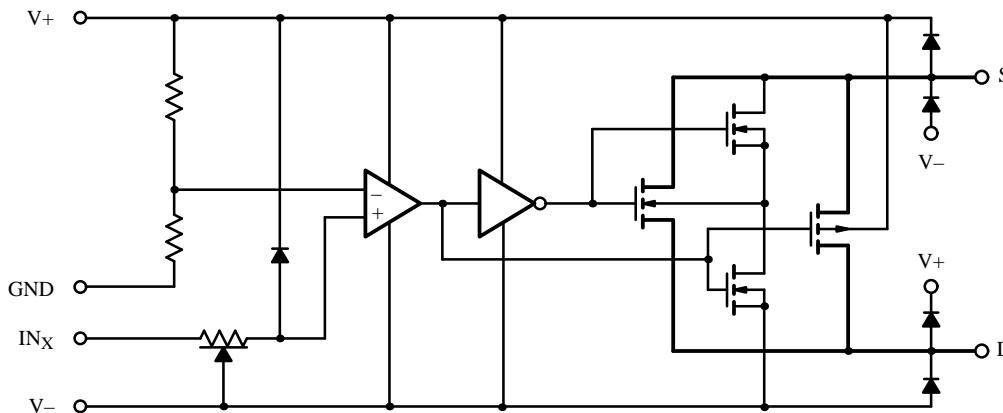


Figure 1.

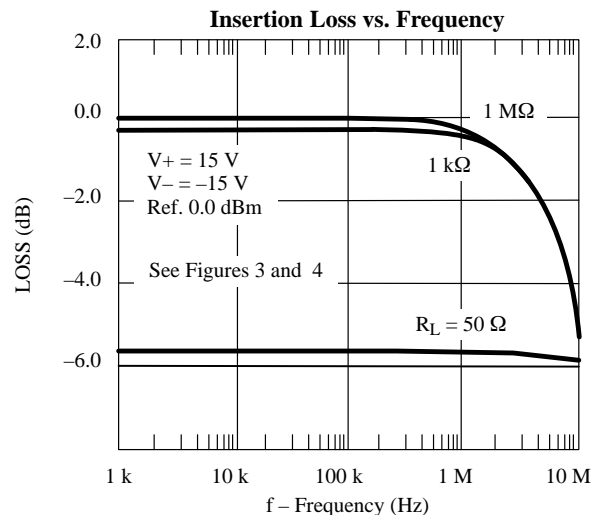
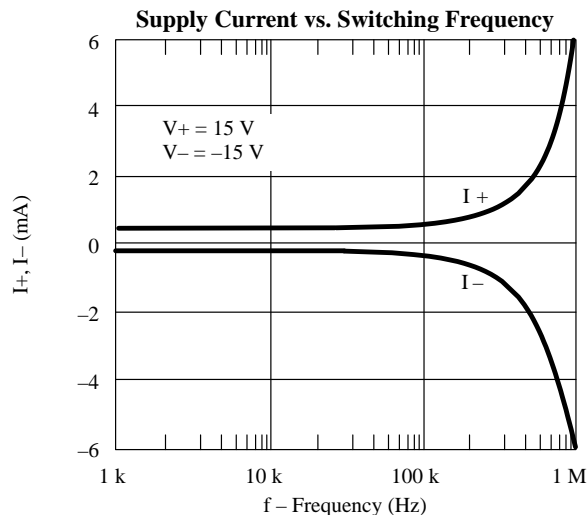
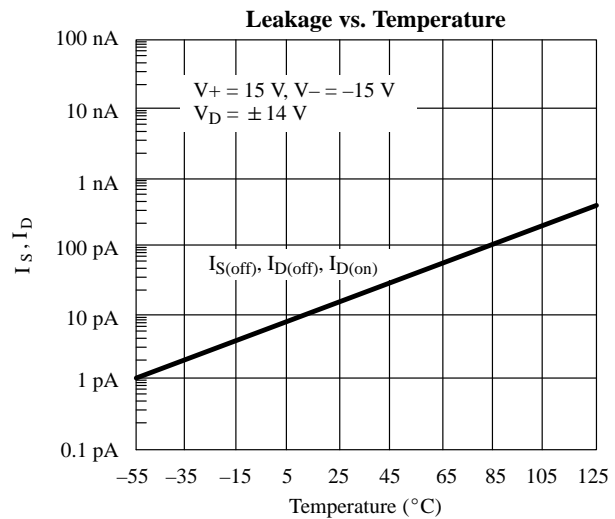
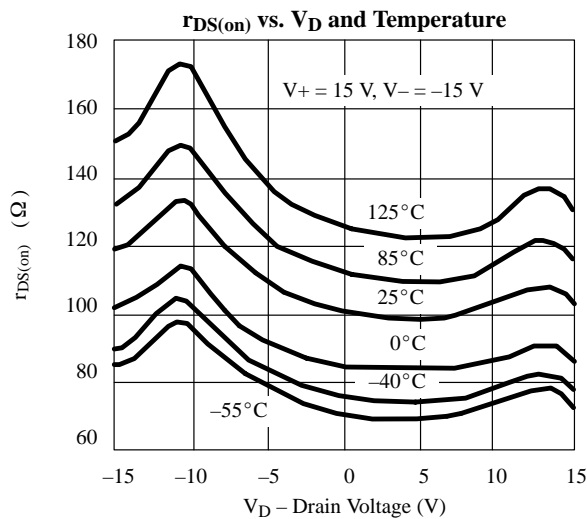
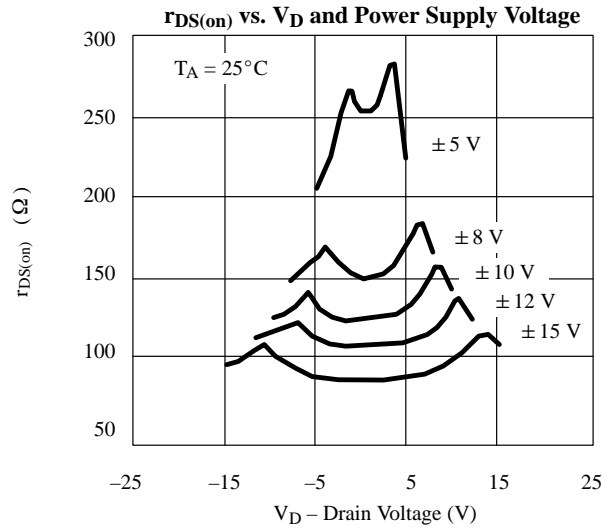
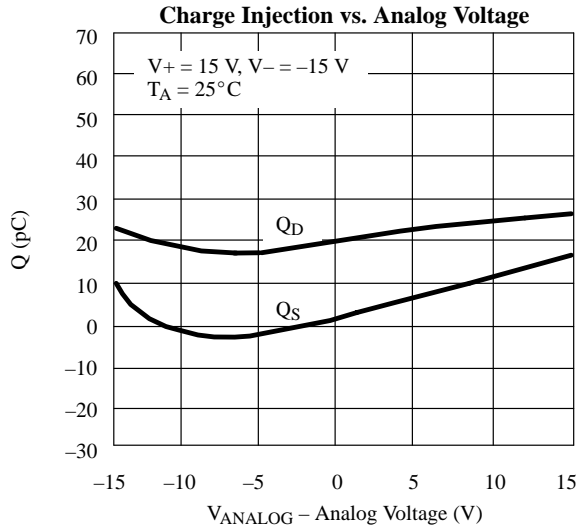
## Specifications<sup>a</sup>

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{IN} = 2.4\text{ V}$ , $0.8\text{ V}^f$	Temp <sup>b</sup>	Typ <sup>c</sup>	A Suffix -55 to 125°C		B, C, D Suffix		Unit
					Min <sup>d</sup>	Max <sup>d</sup>	Min <sup>d</sup>	Max <sup>d</sup>	
<b>Analog Switch</b>									
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		-15	15	-15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = 1\text{ mA}$	Room	115		175		175	$\Omega$
			Full			250		250	
Source Off Leakage Current	$I_{S(off)}$	$V_S = \pm 14\text{ V}$ , $V_D = \mp 14\text{ V}$	Room Full	$\pm 0.02$	-1 -100	1 100	-5 -100	5 100	nA
Drain Off Leakage Current	$I_{D(off)}$	$V_D = \pm 14\text{ V}$ , $V_S = \mp 14\text{ V}$	Room Full	$\pm 0.02$	-1 -100	1 100	-5 -100	5 100	
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \pm 14\text{ V}$	Room Full	$\pm 0.15$	-1 -200	1 200	-5 -200	5 200	
<b>Digital Control</b>									
Input Current with Input Voltage High	$I_{INH}$	$V_{IN} = 2.4\text{ V}$	Room Full	-0.0004	-1 -1		-1 -10		$\mu\text{A}$
		$V_{IN} = 15\text{ V}$	Room Full	0.003		1 10		1 10	
Input Current with Input Voltage Low	$I_{INL}$	$V_{IN} = 0\text{ V}$	Room Full	-0.0004	-1 -10		-1 -10		
<b>Dynamic Characteristics</b>									
Turn-On Time	$t_{ON}$	See Switching Time Test Circuit	Room	480		600		600	ns
Turn-Off Time	$t_{OFF}$		Room	370		450		450	
Charge Injection	Q	$C_L = 1000\text{ pF}$ , $V_g = 0\text{ V}$ $R_g = 0\ \Omega$	Room	20					pC
Source-Off Capacitance	$C_{S(off)}$	$V_S = 0\text{ V}$ , $V_{IN} = 5\text{ V}$ , $f = 1\text{ MHz}$	Room	5					pF
Drain-Off Capacitance	$C_{D(off)}$		Room	5					
Channel On Capacitance	$C_{D(on)} + C_{S(on)}$	$V_D = V_S = 0\text{ V}$ , $V_{IN} = 0\text{ V}$ $f = 1\text{ MHz}$	Room	16					
Off Isolation	OIRR	$V_{IN} = 5\text{ V}$ , $R_L = 75\ \Omega$ $V_S = 2\text{ V}$ , $f = 100\text{ kHz}$	Room	70					dB
Channel-to-Channel Crosstalk	$X_{TALK}$		Room	90					
<b>Power Supply</b>									
Positive Supply Current	I+	All Channels On or Off	Room	0.9		2		2	mA
Negative Supply Current	I-		Room	-0.3	-1		-1		

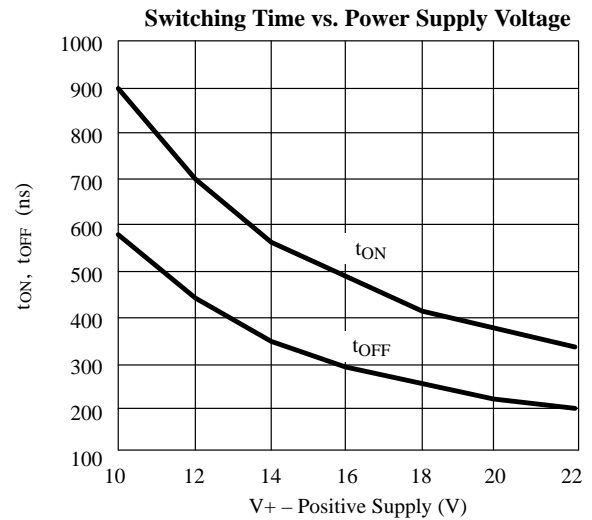
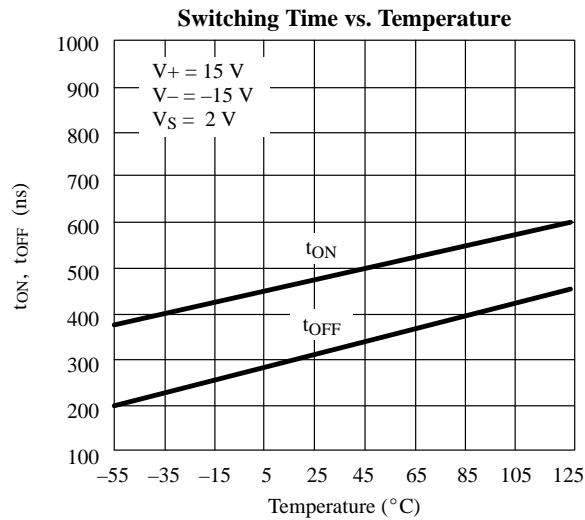
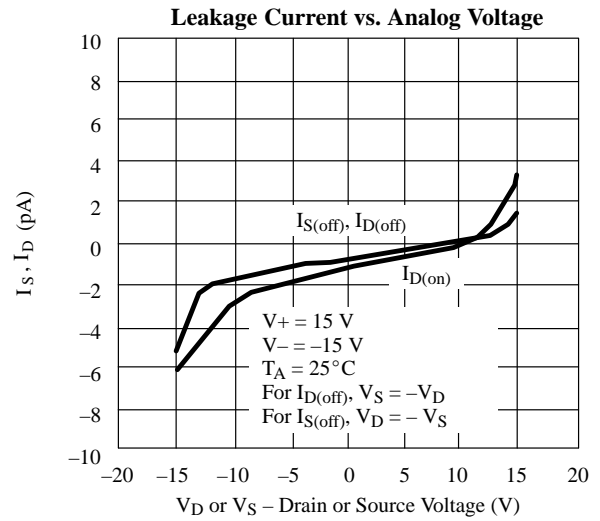
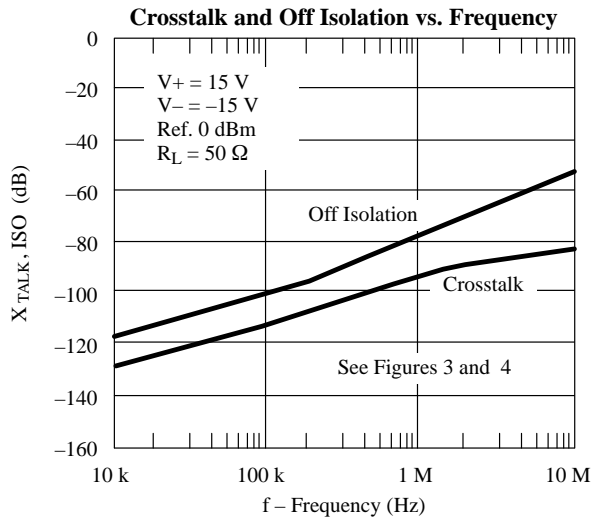
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- $V_{IN}$  = input voltage to perform proper function.

## Typical Characteristics

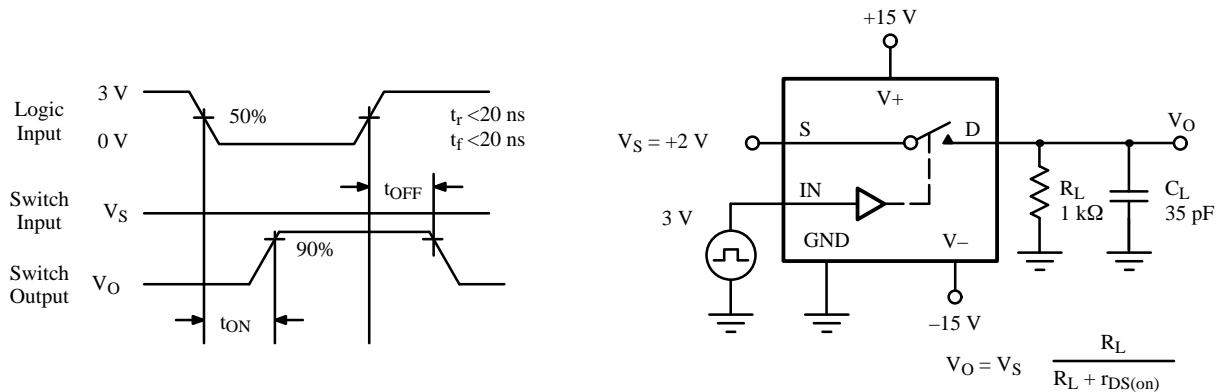


## Typical Characteristics (Cont'd)

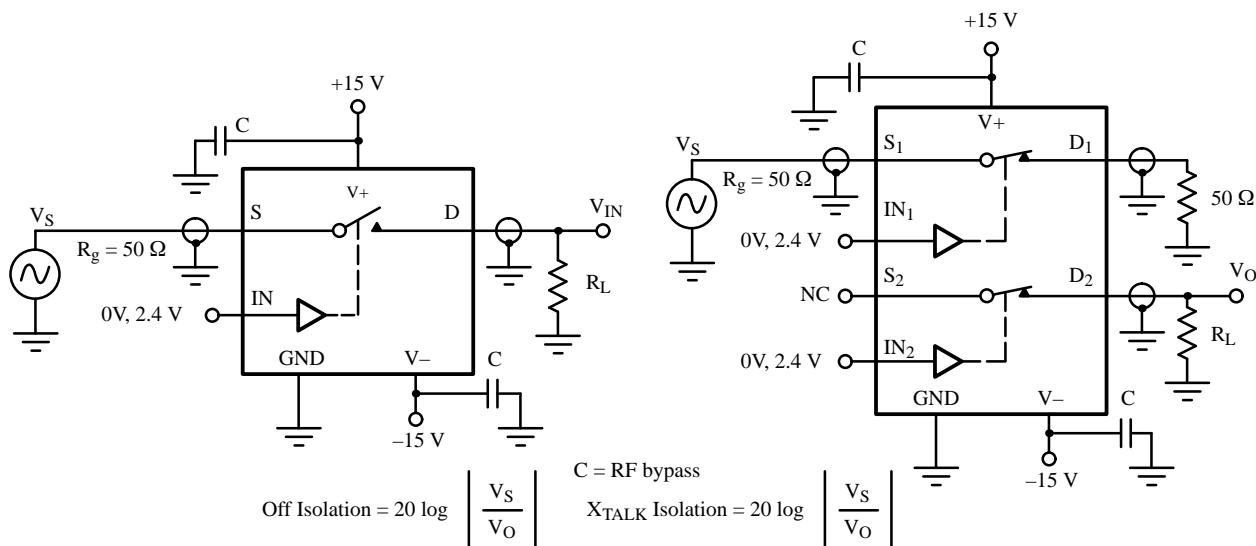


## Test Circuits

$V_O$  is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

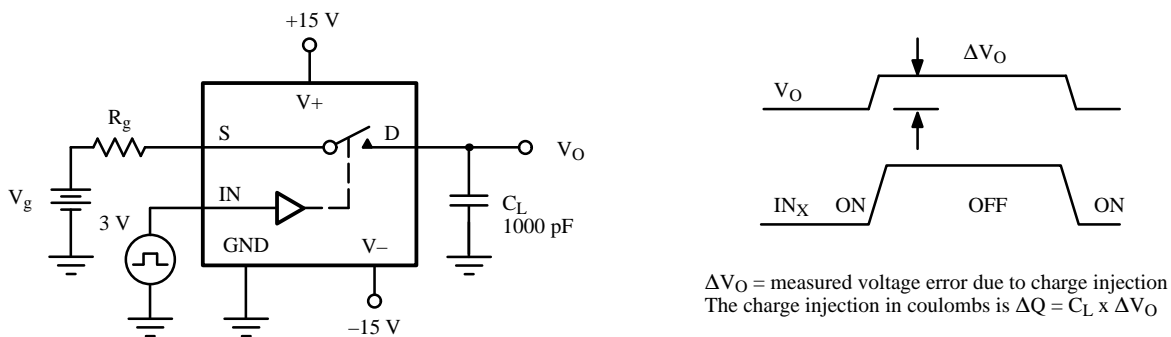


**Figure 2.** Switching Time



**Figure 3.** Off Isolation

**Figure 4.** Channel-to-Channel Crosstalk



**Figure 5.** Charge Injection

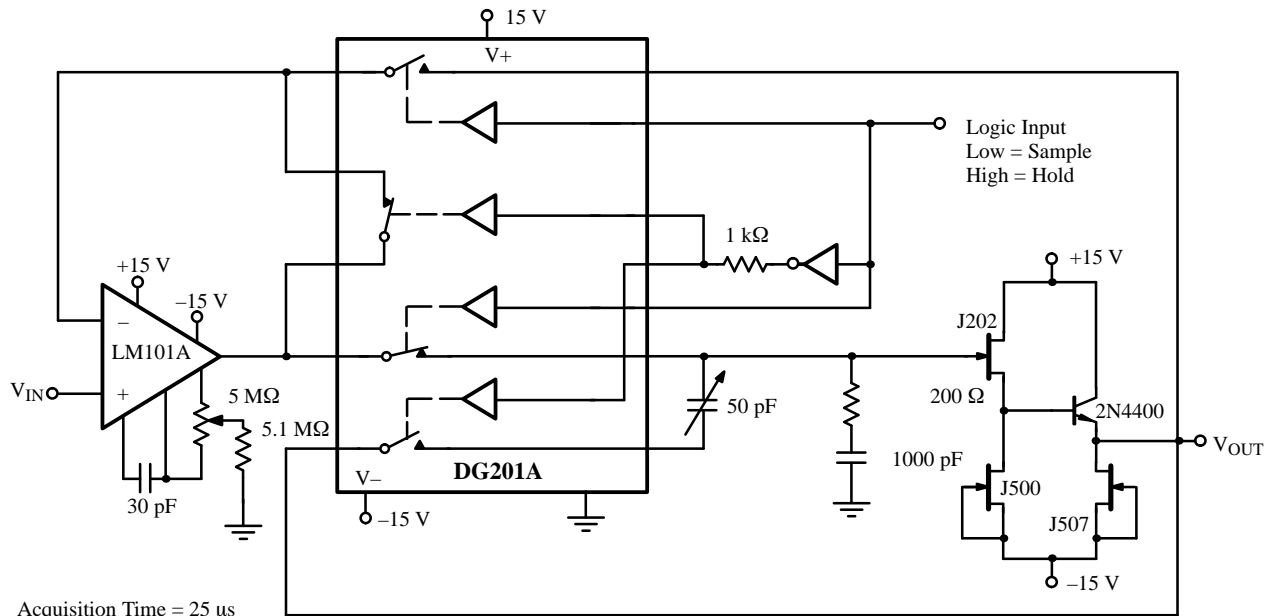
**Application Hints<sup>a</sup>**

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V <sub>IN</sub> Logic Input Voltage V <sub>INH(min)</sub> /V <sub>INL(max)</sub> (V)	V <sub>S</sub> or V <sub>D</sub> Analog Voltage Range (V)
15	-15	2.4/0.8	-15 to 15
10	-12	2.4/0.8	-12 to 12
12	-10	2.2/0.6	-10 to 10
8 <sup>b</sup>	-8	2.0/0.5	-8 to 8

Notes:

- a. Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
- b. Operation below ± 8 V is not recommended.

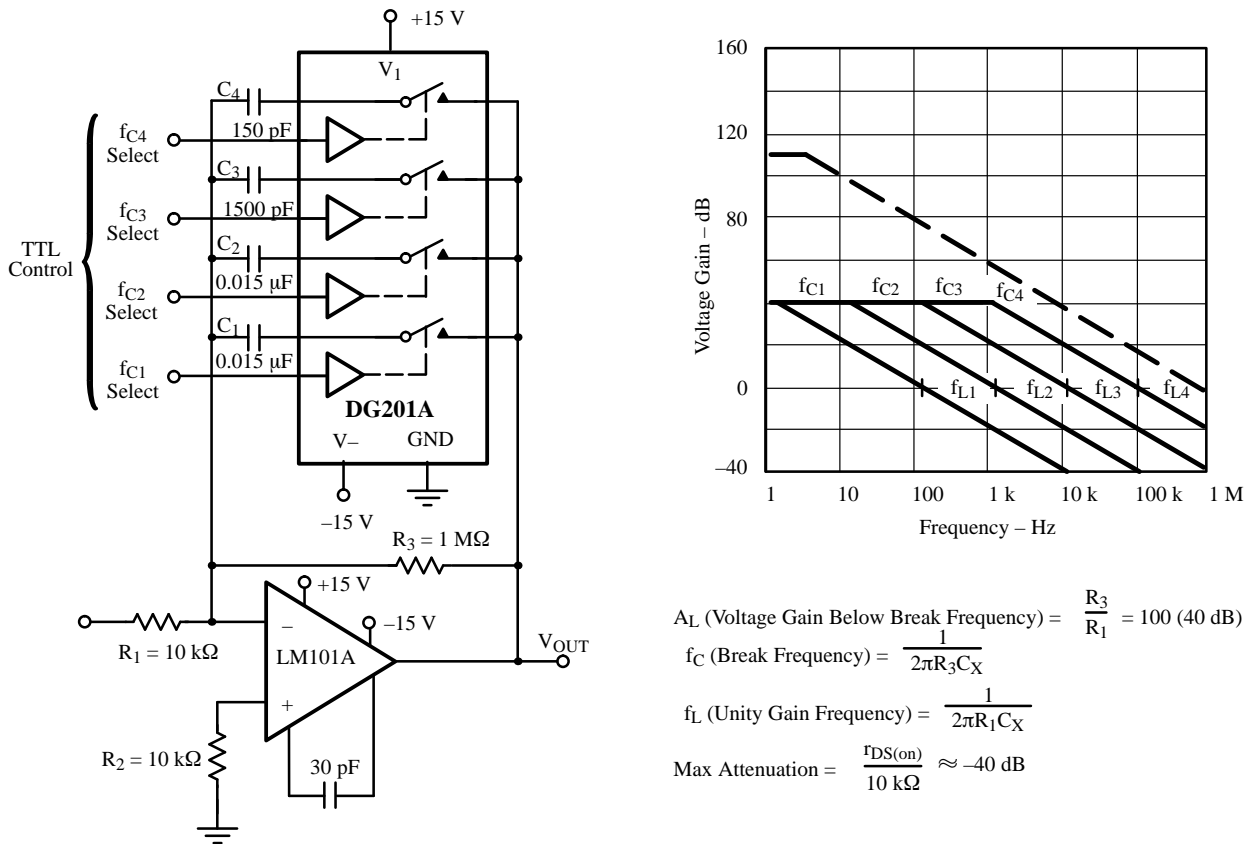
**Applications**



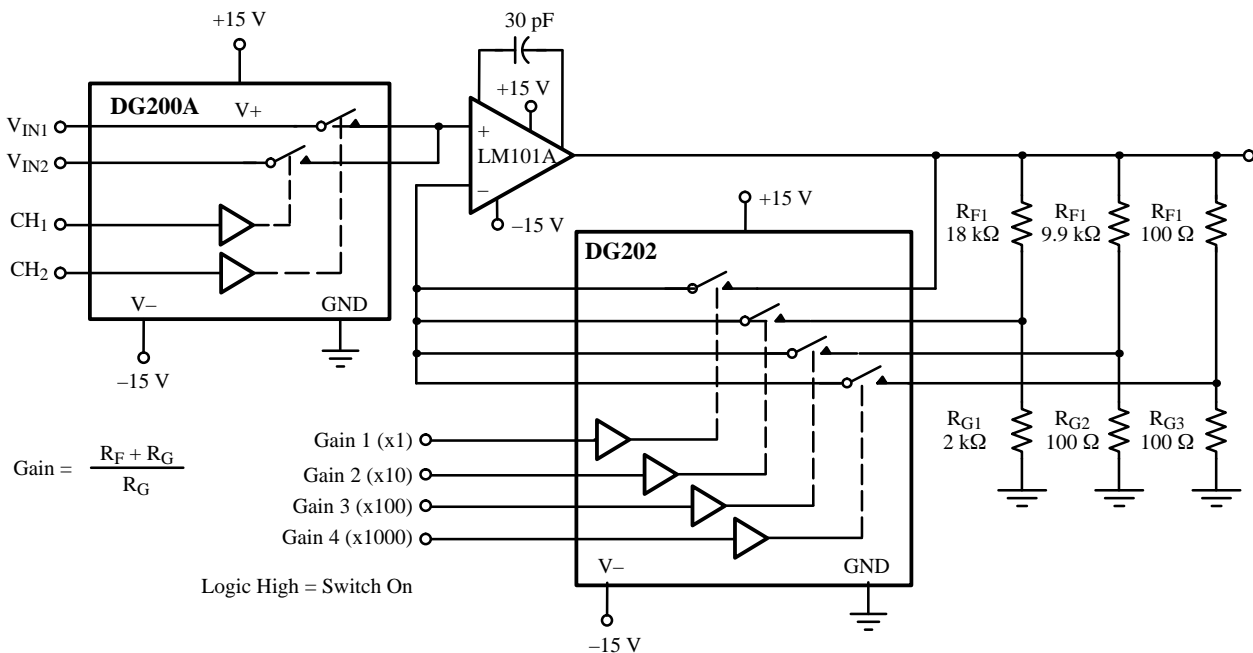
Acquisition Time = 25  $\mu$ s  
 Aperature Time = 1  $\mu$ s  
 Sample to Hold Offset = 5 mV  
 Droop Rate = 5 mV/s

**Figure 6.** Sample-and-Hold

## Applications (Cont'd)



**Figure 7.** Active Low Pass Filter with Digitally Selected Break Frequency



**Figure 8.** A Precision Amplifier with Digitally Programmable Input and Gains