PLL Basics—Loop Filter Design

Introduction

With the rapid expansion of the wireless/RF marketplace, there has been a proliferation of companies entering the fray to design the next winning wireless connectivity product. For many, it is their first attempt to design a PLL synthesized wireless communication transceiver.

The major basic requirements in the design of a PLL frequency synthesizer are to achieve the performance goals of low phase noise, low spurious output and to step, or hop, from one frequency to another in a specified amount of time.

Unfortunately, most of the articles and books written about designing the Loop Filter for PLL synthesizers dwell in the theoretical and try to cover the subject for all cases of PLL synthesizer design. This article will consider the design of a simple passive three-pole Loop Filter typically used in low voltage, low operating bandwidth synthesizer applications. This approach will simplify and demystify the Loop Filter design procedure.

Thanks to current levels of semiconductor integration, the components that make up the total synthesizer solution consist of a PLL IC for the control portion of the synthesizer, a Reference Oscillator and a hybrid VCO. The only external components needed are the DC decoupling elements, RF by-pass elements, and the passive Loop Filter components.

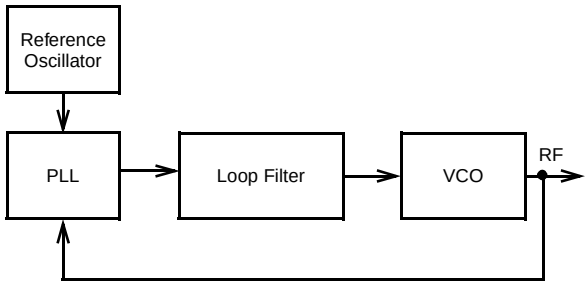


Figure 1. Basic PLL Layout

Presented here are the design calculations that have been used to develop Loop Filter solutions for many PLL applications. These calculations have been found to achieve the expected performance goals.

If the information used in the calculations is accurate, the PLL synthesizer will perform as designed. Experience has shown if the PLL synthesizer does not perform as expected, some component part or device specification is in error.

The simplified Loop Filter design formulas, found in Fujitsu's *Super PLL Application Guide*, are detailed below. The formulas are based upon the use of a basic passive two-pole Loop Filter along with a single-pole spur filter as shown in Figure 2.

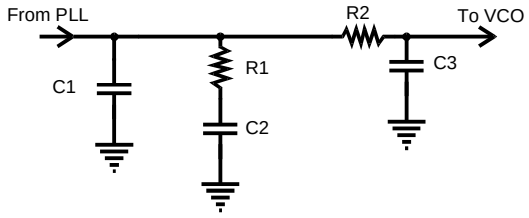


Figure 2. Loop Filter Configuration

Terms

fstep – Maximum frequency change during a step or hop, from one frequency to another.

ts – The desired time for the carrier to step to a new frequency.

fa – The frequency of the carrier, within the desired time (ts), after a step or hop. This is normally 1000 Hz.

ξ – Damping Factor - 0.707 is the typical choice

fn – Natural frequency

Icp – Charge Pump Current

Kvco – VCO sensitivity

ln – Natural LOG

Basic Calculations

1. Determine the maximum dividing ratio, N.

$$N = \frac{Maximum\ VCO\ Frequency}{Channel\ Spacing}$$

2. Calculate fn (natural frequency).

$$fn = \frac{-1}{2\pi \times ts \times \xi} \times ln\left(\frac{fa}{fstep}\right)$$

3. Calculate capacitor C2.

$$C2 = \frac{Icp \times Kvco}{N \times (2\pi \times fn)^2}$$

4. Calculate resistor R1.

$$R1 = 2 \times \xi \times \sqrt{\frac{N}{Icp \times Kvco \times C2}}$$

5. Calculate capacitor C1.

$$C1 = \frac{C2}{10}$$

6. Calculate R2 and C3 – the spur filter.

R2 and C3 are used to reduce any "spurs" caused by the reference frequency. The product of R2 and C3 should be at least 1/10 the product of C2 and R1.

Design Example

First you must define the basic synthesizer requirements for your application. Then define the active component's specifications.

For this example, a hypothetical application with arbitrary low-side injection is specified. It will use the Fujitsu MB15F08SL PLL IC and a VCO with a 25 volt/MHz sensitivity.

Application Requirements

Frequency Range:	1675 to 1735 MHz
Channel Spacing:	200 KHz
Maximum Frequency Hop:	60 MHz
Frequency Hop time:	500 microseconds
Frequency Accuracy after the specified Hop time:	1000 Hz

Identify the Active Component Specifications

VCO sensitivity:	25 MHz/V
PLL IC Charge Pump current:	6 mA

Step by Step Example Calculations

1. Determine N

$$N = \frac{1735\ MHz}{200\ KHz}$$

$$N = 8675$$

2. Determine fn

$$fn = \frac{-1}{6.28 \times 0.5e^{-3} \times 0.707} \times ln\frac{1000}{60e^{6}}$$

$$fn = 4,955.95\ Hz$$

3. Calculate C2

$$C2 = \frac{.006 \times 25e^{6}}{8675 \times (6.28 \times 4955.95)^2}$$

$$C2 = 0.01785\mu F$$

4. Calculate R1

$$R1 = 2 \times 0.707 \times \sqrt{\frac{8675}{.006 \times 25e^{6} \times 0.01785e^{-6}}}$$

$$R1 = 2545\Omega$$

5. Calculate C1

$$C1 = \frac{.01785\mu F}{10}$$

$$C1 = .001785\mu F$$

6. Determine R2 and C3 – the spur filter

The product of R2 and C3 should be about 1/10 the product of R1 and C2.

$$R2 = 2545\Omega$$

$$C3 = \frac{.01785\mu F}{10} = .001785\mu F$$

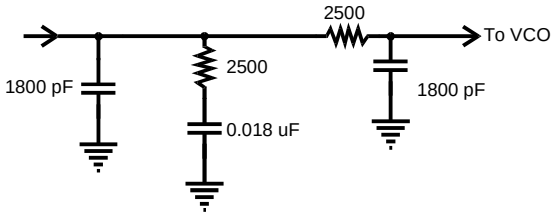


Figure 3. Loop Filter Components to the Nearest Standard Values

After the Loop filter values have been calculated, the Loop Bandwidth can be calculated.

Knowing the Loop Bandwidth will help determine if the PLL is operating correctly when the Phase Noise is displayed on a Spectrum Analyzer.

Loop Bandwidth Calculation

$$Loop\ Bandwidth\ =\ \frac{(2\pi)\times fn}{2}\times\left(\xi+\frac{1}{4\xi}\right)Hz$$

Loop Bandwidth Calculation for this Example

$$Loop\ Bandwidth\ =\ \frac{6.28\times 4955}{2}\times\left(.707+\frac{1}{2.828}\right)$$

$$Loop\ Bandwidth\ =\ 16,500\ Hz$$

The following graphs show the performance of the PLL synthesizer using the calculated values.

The graphs confirm that the calculations work well for designing Loop Filters to be used in many of today's PLL applications.

Figure 4 shows the excellent Phase Noise performance of the RF PLL of Fujitsu's new MB15F08SL dual 2.5/1.1 GHz PLL using the calculated Loop Filter values.

Marker "0" shows the Phase Noise inside the loop is –80.5 dBc/Hz. Marker "1" shows the loop bandwidth is 16000 Hz.

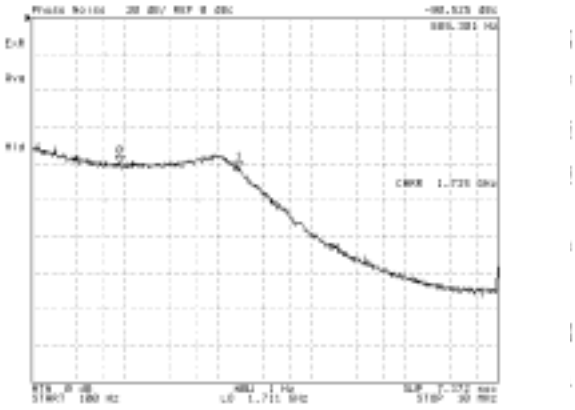


Figure 4. Phase Noise

Figure 5 shows the 200 KHz spurious signals to be an impressive -87.7 dBc, typical of the new Fujitsu SL Series of advanced PLL synthesizers, giving optimum performance for the latest digital wireless communications designs.

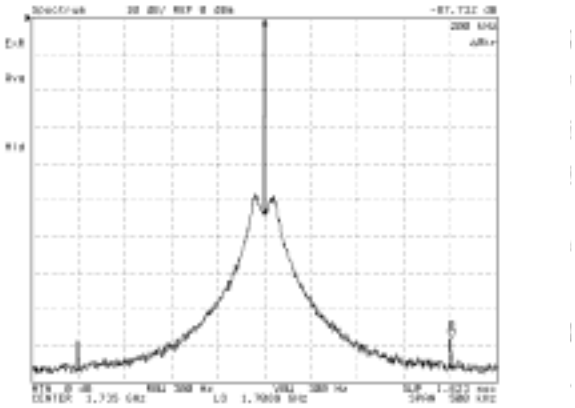


Figure 5. Spurious Response

Figure 6 shows that it takes 514 microseconds to change the frequency from 1675 MHz to 1735 MHz ±1000 Hz.

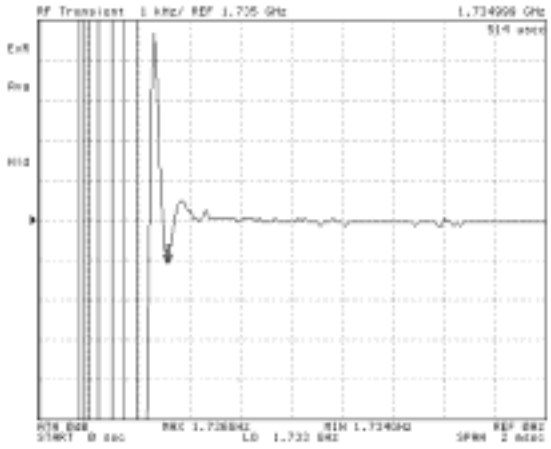


Figure 6. Hop Time

PLL Synthesizer Practical Considerations

Capacitors

An important part of the Loop Filter design is the use of components that will not degrade the performance of the synthesizer. The capacitors must have very low leakage.

Ceramic capacitors should not be used. The piezo-electric effect can cause noise and even microphonics on the VCO tuning line.

Film capacitors are recommended.

Resistors

The resistors should be the Metal or Carbon film type. Carbon composition is not recommended.

PCB Layout

The layout of the PC board can affect the level of VCO spurious signals and noise.

There are two very important things to do when laying out the PC board to reduce noise and spurs.

First, provide the shortest possible ground path between the PLL IC ground pins, Loop Filter ground, and the ground for the VCO Varicap tuning diode. If a packaged VCO is being used, it should be mounted close to the PLL IC and Loop Filter.

Second, bypass the Vcc lines that feed the PLL chip with a small value capacitor (0.1 mfd) and a large value capacitor (10 mfd). These capacitors should be placed as close as possible to the Vcc pins. Bypassing should also be used for the VCO. If the PLL and the VCO use the same Vcc, a 22-ohm resistor should be placed in the Vcc line between them to improve the isolation.

Conclusion

The purpose of this application note is to show that it is not difficult to design a high performance PLL synthesizer using the highly integrated parts available today.

Synthesizers operating well above 2000 MHz can be built with relatively few problems, provided good RF techniques are used for board layout and parts placement.

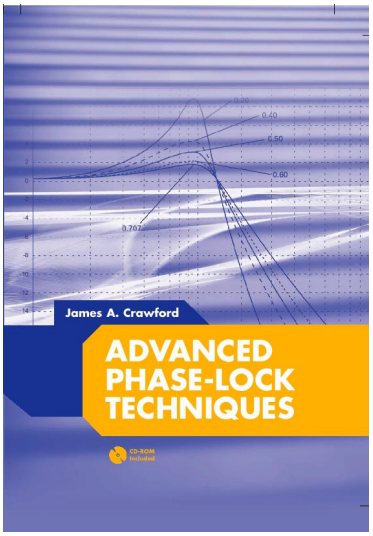
References:

Super PLL Application Guide
TC-AN-20731-11/98 - Fujitsu Microelectronics, Inc.
Ph. 800-866-8608

MB15FxxSL Series Data booklet
TC-DS-20788-2/99 - Fujitsu Microelectronics, Inc.
Ph. 800-866-8608

Microwave and Wireless Synthesizers
Ulrich L. Rohde
John Wiley & Sons, Inc.
ISBN 0-471-52019-5

Frequency Synthesizers
Vadim Manassewitsch
John Wiley & Sons, Inc.
ISBN 0-471-01116-9



Advanced Phase-Lock Techniques

James A. Crawford

2008

Artech House

510 pages, 480 figures, 1200 equations
CD-ROM with all MATLAB scripts

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ISBN-10: 1-59693-140-X

Chapter	Brief Description	*Pages*
1	*Phase-Locked Systems—A High-Level Perspective* An expansive, multi-disciplined view of the PLL, its history, and its wide application.	26
2	*Design Notes* A compilation of design notes and formulas that are developed in details separately in the text. Includes an exhaustive list of closed-form results for the classic type-2 PLL, many of which have not been published before.	44
3	*Fundamental Limits* A detailed discussion of the many fundamental limits that PLL designers may have to be attentive to or else never achieve their lofty performance objectives, e.g., Paley-Wiener Criterion, Poisson Sum, Time-Bandwidth Product.	38
4	*Noise in PLL-Based Systems* An extensive look at noise, its sources, and its modeling in PLL systems. Includes special attention to 1/*f* noise, and the creation of custom noise sources that exhibit specific power spectral densities.	66
5	*System Performance* A detailed look at phase noise and clock-jitter, and their effects on system performance. Attention given to transmitters, receivers, and specific signaling waveforms like OFDM, M-QAM, M-PSK. Relationships between EVM and image suppression are presented for the first time. The effect of phase noise on channel capacity and channel cutoff rate are also developed.	48
6	*Fundamental Concepts for Continuous-Time Systems* A thorough examination of the classical continuous-time PLL up through 4^{th}-order. The powerful Haggai constant phase-margin architecture is presented along with the type-3 PLL. Pseudo-continuous PLL systems (the most common PLL type in use today) are examined rigorously. Transient response calculation methods, 9 in total, are discussed in detail.	71
7	*Fundamental Concepts for Sampled-Data Control Systems* A thorough discussion of sampling effects in continuous-time systems is developed in terms of the *z*-transform, and closed-form results given through 4^{th}-order.	32
8	*Fractional-N Frequency Synthesizers* A historic look at the fractional-N frequency synthesis method based on the U.S. patent record is first presented, followed by a thorough treatment of the concept based on Δ-Σ methods.	54
9	*Oscillators* An exhaustive look at oscillator fundamentals, configurations, and their use in PLL systems.	62
10	*Clock and Data Recovery* Bit synchronization and clock recovery are developed in rigorous terms and compared to the theoretical performance attainable as dictated by the Cramer-Rao bound.	52