# Linear IC Converter cmos

# A/D Converter

(With 4-channel Input at 12-bit Resolution)

# MB88101A

#### **■ DESCRIPTION**

The MB88101A is an analog-to-digital converter that converts its analog input to a 12-bit digital value and outputs it as serial data.

The MB88101A employs a successive approximation method for A/D conversion.

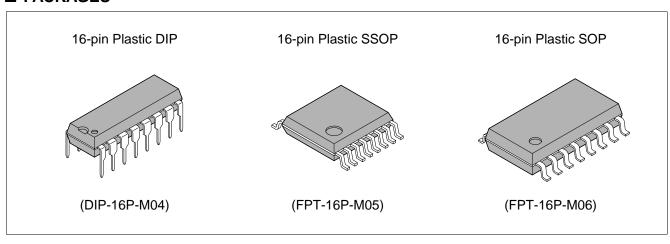
The MB88101A has four input channels selectable for analog input under control of the dedicated external pins.

The MB88101A can be switched to a mode for continuous A/D conversion, in which it outputs serial data from the MSB or LSB selectable depending on the mode setting.

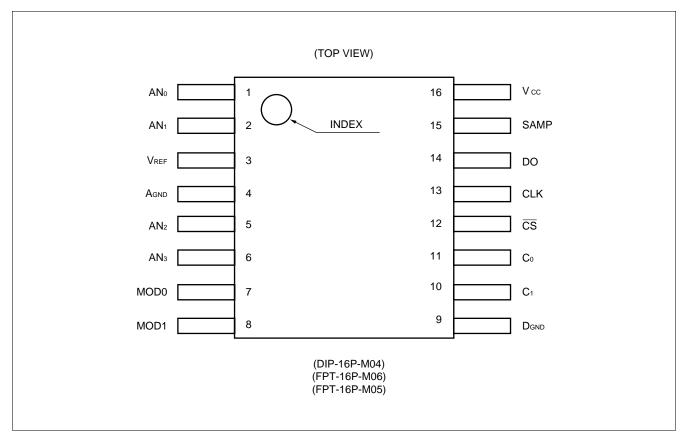
#### **■ FEATURES**

- 4-channel analog input
- One analog input channel selectable for conversion by external control
- CR-type successive approximation system with a sample-and-hole circuit
- 12-bit resolution
- · Serial output of 12-bit digital data
- Capable of continuous conversion (continuous conversion mode)
- MSB or LSB selectable for serial output
- CMOS process
- · Package options of 16-pin DIP, SSOP, and SOP available

#### ■ PACKAGES



### **■ PIN ASSIGNMENT**



### **■ PIN DESCRIPTION**

Pin no.	Symbol	I/O	Descriptions	
1 2 5 6	AN <sub>0</sub> AN <sub>1</sub> AN <sub>2</sub> AN <sub>3</sub>	I	Analog input pins. One of these channels can be selected depending on the $C_0$ and $C_1$ settings.	
14	DO	0	This pin outputs the result of A/D conversion. The result is 12-bit serial data output in synchronization with the rise of CLK.	
13	CLK	I	Clock input pin for A/D conversion	
12	<u>CS</u>	I	Chip select signal input pin. Setting the signal level to "L" after turning the power on starts A/D conversion; setting it to "H" stops A/D conversion. When this pin is "H", the DO and SAMP pins are "Hi-z".	
11 10	C <sub>0</sub> C <sub>1</sub>	I	Input pins for selecting the analog input channels from among pins ANo to AN3. See Table 1 for the correspondence between the pin settings and the channels selected. To switch the channel in mode 2 or 3, set these pins before the SAMP pin goes "H".	
7 8	MOD0 MOD1	I	Conversion mode setting pins. For the correspondence between the pin settings and the modes selected, see Table 2 and "■ FUNCTIONAL DESCRIPTION."	
15	SAMP	0	This pin becomes active in prior to data output. Serial data is output from the DO pin three clock cycles after the signal level at this pin goes "L" after "H" for one clock cycle.	
3	V <sub>REF</sub>	_	Reference voltage input pin	
4	Agnd	_	Analog circuit ground pin	
9	DGND	_	Digital circuit ground pin	
16	Vcc	_	Power supply pin	

### • Channel selection

### Table 1 Pin Settings and Channel Selection

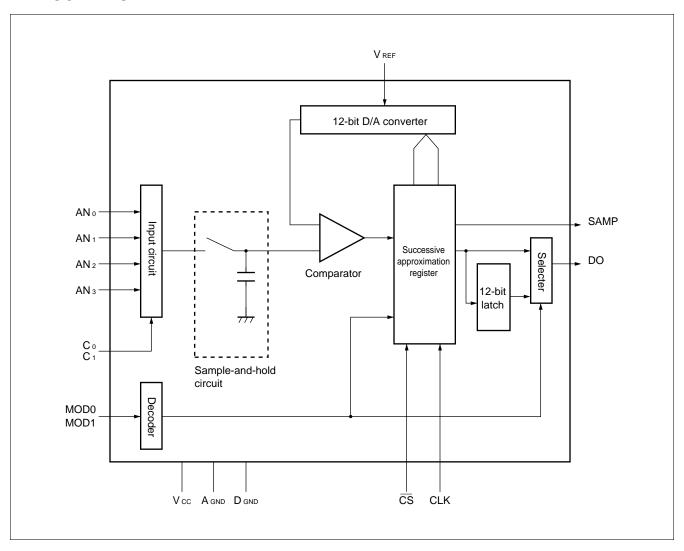
<b>C</b> <sub>1</sub>	C <sub>0</sub>	Channel
L	L	AN <sub>0</sub>
L	Н	AN <sub>1</sub>
Н	L	AN <sub>2</sub>
Н	Н	AN <sub>3</sub>

### • Mode selection

Table 2 Pin Settings and Mode Selection

MOD 0	MOD1	Mode
L	L	Mode 1
L	Н	Mode 2
Н	L	(Disabled)
Н	Н	Mode 3

### **■ BLOCK DIAGRAM**

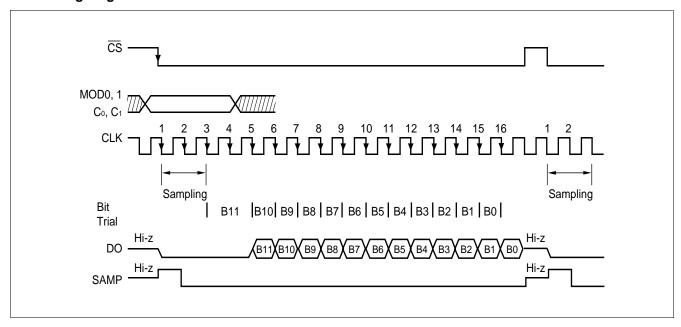


#### **■ FUNCTIONAL DESCRIPTION**

#### 1. Mode 1

This mode sets the DO pin to "L" and stops conversion upon completion of conversion of 12 bits. To restart conversion, set  $\overline{\text{CS}}$  to "H" once then to "L". In this mode, converted data is output from the MSB.

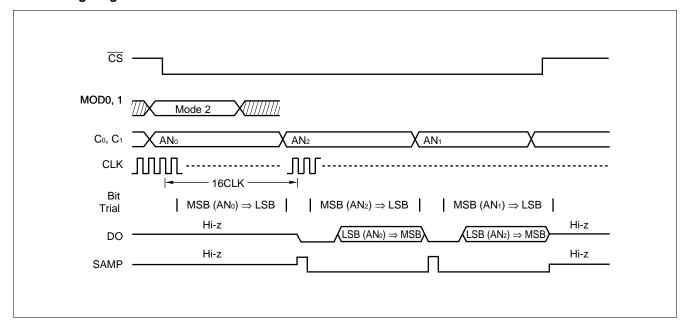
#### • Timing diagram



#### 2. Mode 2

This mode continues conversion until  $\overline{CS}$  becomes "H" after it becomes "L". Converted data is output from the LSB, with the first piece of converted data output 20 clock cycles after  $\overline{CS}$  becomes "L". Changing the channel select pin settings before starting sampling of one analog input allows another to be converted.

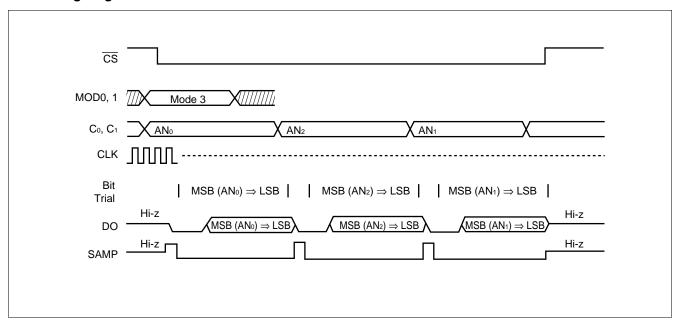
#### Timing diagram



### 3. Mode 3

This mode continues conversion until  $\overline{CS}$  becomes "H" after it becomes "L". Converted data is output from the MSB. Changing the channel select pin settings before starting sampling of one analog input allows another to be converted.

### • Timing diagram



#### ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rat	Unit	
Parameter	Symbol	Conditions	Min.	Max.	Offic
Power cumply voltage	Vcc		-0.3	+7.0	V
Power supply voltage	V <sub>REF</sub>	Based on GND	-0.3*	+7.0*	V
Input voltage	Vin	(Ta = +25°C)	-0.3	Vcc + 0.3	V
Output voltage	Vouт		-0.3	Vcc + 0.3	V
Power consumption	PD	_	_	150	mW
Operating temperature	Та	_	-20	+85	°C
Storage temperature	T <sub>stg</sub>	_	<b>-</b> 55	+150	°C

<sup>\*:</sup>  $V_{CC} \ge V_{REF}$ 

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

#### ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol		Unit		
raiailletei	Symbol	Min.	Тур.	Max.	Ollit
Dower aupply voltage	Vcc	3.3	_	5.5	V
Power supply voltage	GND	_	0	_	V
Operation temperature	Та	-20	_	+85	°C

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

### **■ ELECTRICAL CHARACTERISTIC**

### 1. DC Characteristics

### (1) Digital section

 $(Vcc = 3.3 \text{ V to } 5.5 \text{ V}, D_{GND} = 0 \text{ V}, Ta = -20^{\circ}\text{C to } +85^{\circ}\text{C})$ 

Parameter	Symbol Pin name	Conditions	Value			Unit	
Parameter	Symbol	rin name	Conditions	Min.	Тур.	Max.	Unit
Power supply voltage	Vcc		_	3.3	5.0	5.5	V
Power supply current	lcc	Vcc	Operation at CLK =166kHz (with no load)	_	0.8	2.0	mA
Input leakage current	IILK	MOD0, 1 CLK CS	Vin = 0 to Vcc	-10	_	10	μΑ
Low-level input voltage	VıL		_	V <sub>SS</sub> – 0.3	_	0.2 Vcc	V
High-level input voltage	VIH	C <sub>0</sub> C <sub>1</sub>	_	0.8 Vcc	_	Vcc+ 0.3	V
High-impedance output leakage current	lolz	DO SAMP	Vin = 0 to Vcc	-10	_	10	μΑ
Low-level output voltage	Vol		IoL = 2.5 mA	_	_	0.4	V
High-level output voltage	Vон		Іон = -400 μА	Vcc - 0.4	_	_	V

### (2) Analog section

(VREF, VCC = 3.3 V to 5.5 V (VCC  $\geq$  VREF), AGND = 0 V, Ta =  $-20^{\circ}$ C to  $+85^{\circ}$ C)

Parameter	Symbol	Pin name	Value			Unit
raiailletei	Symbol	Fili liallie	Min.	Тур.	Max.	Offic
Resolution	_		_	12	_	bits
Linearity error	_	AN₀ to AN₃	-4.0	_	2.0	LSB
Differential linearity error	_		-1.0	_	3.0	LSB
Conversion time	_	_	_	16	_	CLK
Consumption current	IREF	Vref	_	100	300	μΑ
Analog reference voltage	_	VKEF	3.3	5.0	Vcc	V
Analog input voltage	_	AN₀ to AN₃	0	_	V <sub>REF</sub>	V

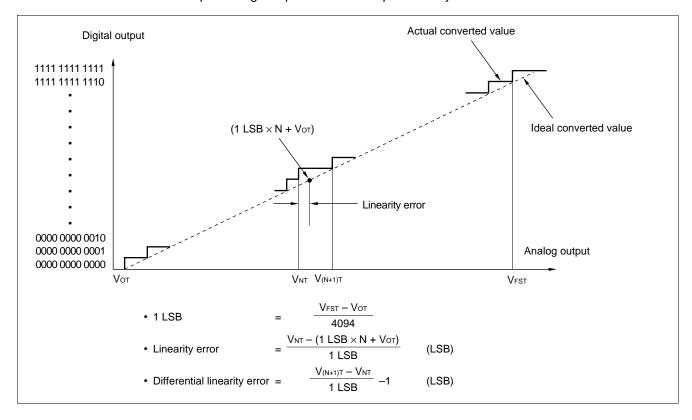
#### (3) Definitions of A/D converter terms

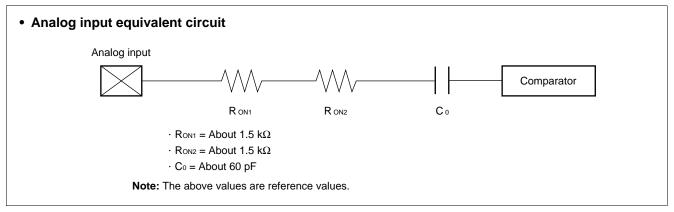
- Resolution
  - Analog transition identifiable by the A/D converter
- Linearity error

Deviation of the straight line drawn between the zero transition point (0000 0000 0000  $\leftrightarrow$  0000 0000 0001) and the full-scale transition point (1111 1111 1110  $\leftrightarrow$  1111 1111 1111) of the device from actual conversion characteristics

· Differential linearity error

Deviation from the ideal input voltage required to shift output code by one LSB





Notes: • The tolerance of output impedance of an external circuit connected to this A/D converter has an effect on conversion time (CLK frequency). See "■ TYPICAL CHARACTERISTICS".

- If the output impedance of the external input is too high, the analog voltage sampling time may be short.
- When turning the device on, turn the power supply for the digital system first before turning VREF on.

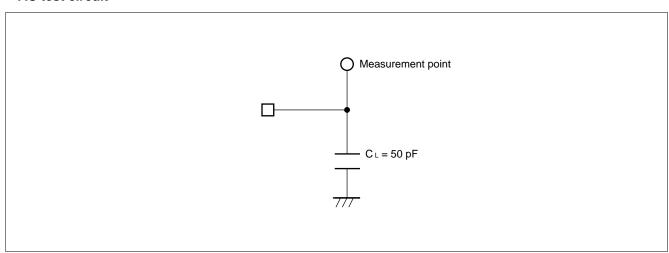
### 2. AC Characteristics

(VREF, VCC = 3.3 V to +5.5 V (VCC  $\geq$  VREF), AGND = 0 V, Ta =  $-20^{\circ}$ C to  $+85^{\circ}$ C)

Dorometer	Cumbal	Symbol Conditions		Value	
Parameter	Symbol	Conditions	Min.	Max.	Unit
Clask evals time	4	Vcc = 5 V ± 10% *1	1.0	30.0	μs
Clock cycle time	<b>t</b> clk	_	6.0	30.0	μs
Low-level clock pulse width	<b>t</b> ckl	_	2.8	14.8	μs
High-level clock pulse width	tскн	_	2.8	14.8	μs
Clock rise time Clock fall time	tcr tcf	_	_	0.2	μs
CS setup time	tcss	_	tckl + 0.4	_	μs
CS hold time	tсsн	_	1.0	_	μs
CS release time	tcsr	_	1.0	_	CLK
Channel setup time	<b>t</b> chs	_	0	_	μs
Channel hold time	tснн	_	1.0	_	CLK
Data output delay time	<b>t</b> DO	*2	_	0.5	μs
MOD setup time	tмos	_	0.2	_	μs
MOD hold time	<b>t</b> мон	_	0.1	_	μs
Data active delay time	<b>t</b> dve	_	_	0.5	μs
Data float delay time	<b>t</b> dze	_	_	0.5	μs
SAMP active delay time	<b>t</b> sve	_	_	0.5	μs
SAMP float delay time	tsze	_	_	0.5	μs
SAMP high-level output delay time	tshd	*2	_	0.5	μs
SAMP low-level output delay time	tsld	*2	_	0.5	μs

<sup>\*1:</sup> Depending on the output impedance of the external circuit connected to the analog input pin

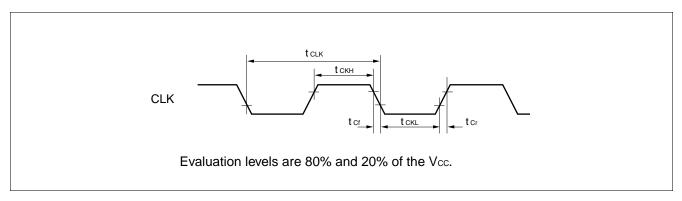
### • AC test circuit



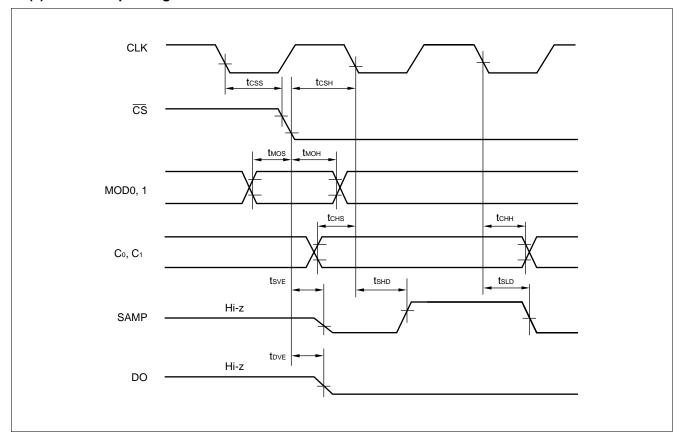
<sup>\*2:</sup> See ". AC test circuit."

### **■ TIMING DIAGRAM**

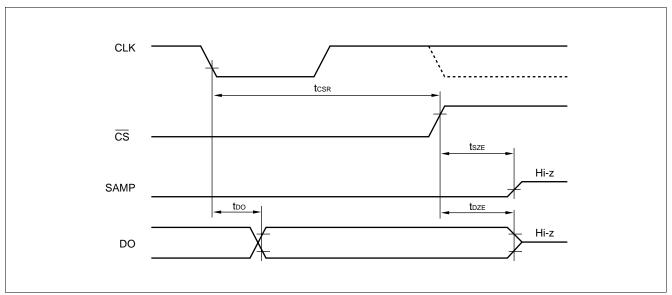
## (1) Input clock timing



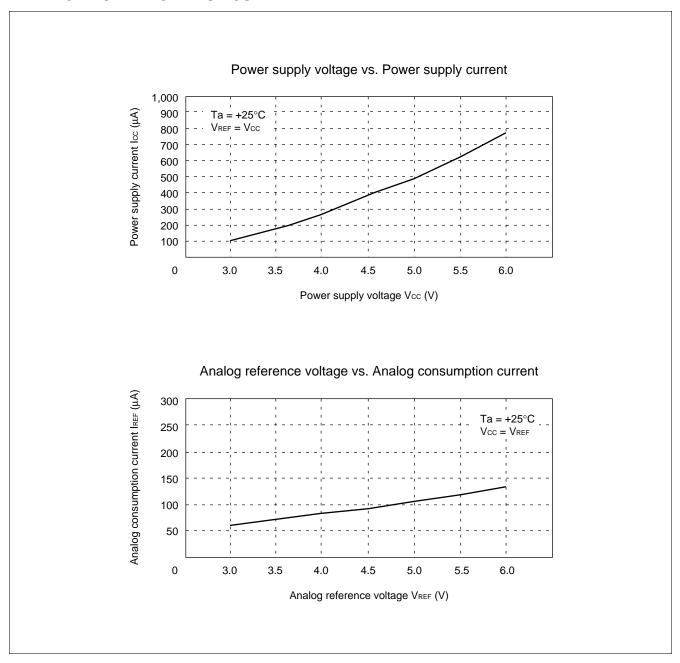
## (2) A/D startup timing

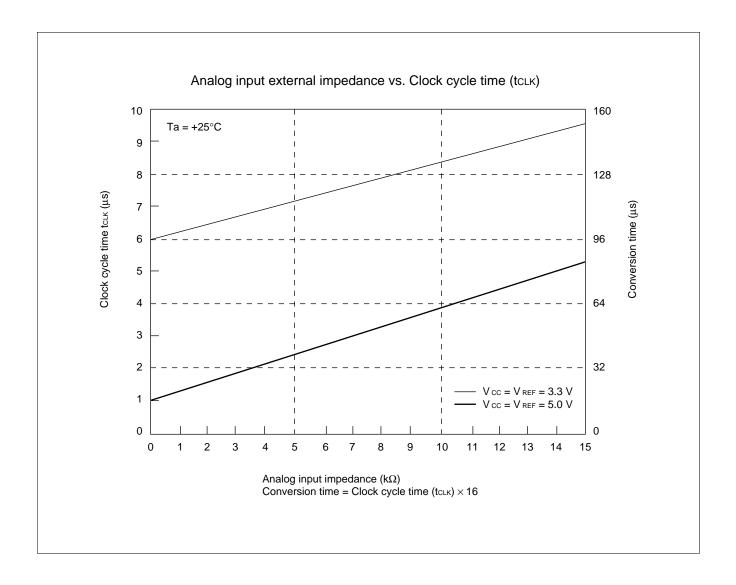


# (3) Data output delay time and A/D stop timing



### **■ TYPICAL CHARACTERISTICS**

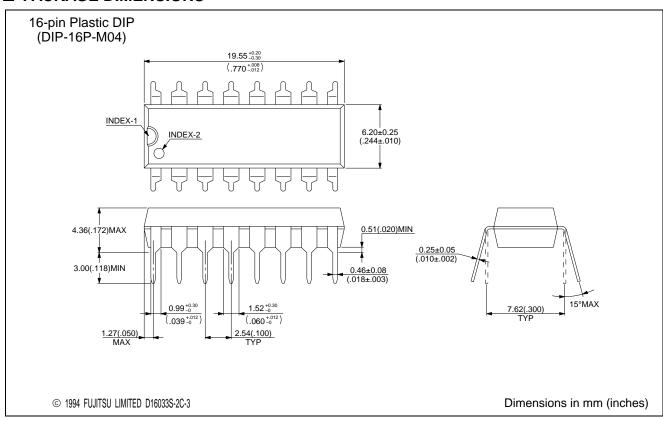


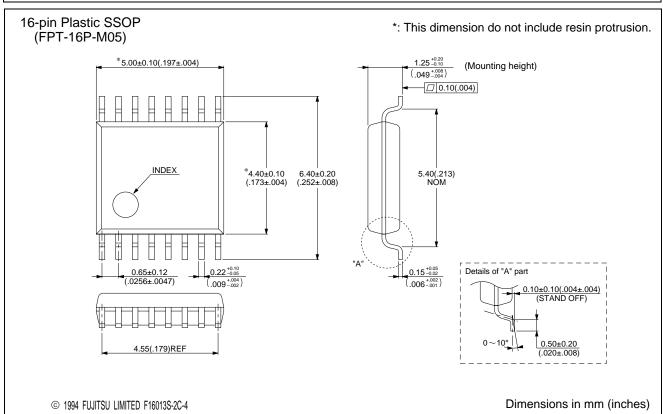


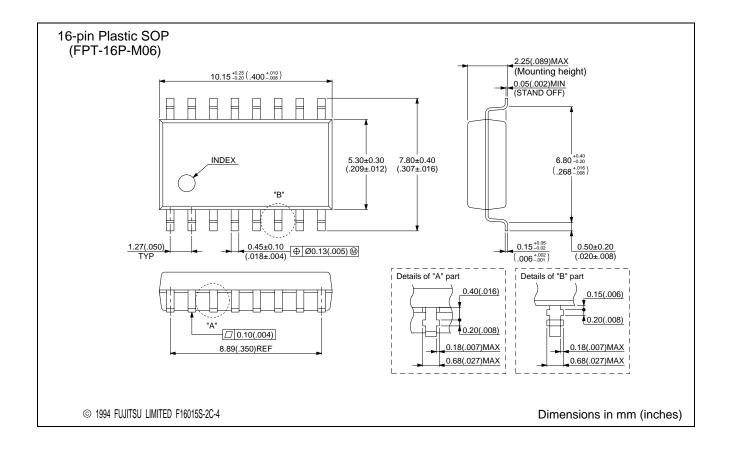
# **■** ORDERING INFORMATION

Part number	Package	Remarks
MB88101AP	16-pin Plastic DIP (DIP-16P-M04)	
MB88101APFV	16-pin Plastic SSOP (FPT-16P-M05)	
MB88101APF	16-pin Plastic SOP (FPT-16P-M06)	

### **■ PACKAGE DIMENSIONS**







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