Using the NM93CS EEPROM Family Features

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The NM93CS Family consists of four members as shown in Table I. Each of these members is available in a variety of temperature ranges, operating voltage ranges, and packaging options. These EEPROMs are a superset of the industry standard NM93C Family. The differentiating features of the NM93CS Family are the Sequential Register Read and the Memory Protect Register. The purpose of this application note is to more fully describe these features.

TABLE I. NM93CS Family Members

Part Number	Memory Size	Internal Organization
NM93CS06	256-bit	16 x 16
NM93CS46	1024-bit	64 x 16
NM93CS56	2048-bit	128 x 16
NM93CS66	4096-bit	256 x 16

SEQUENTIAL REGISTER READ

This read mode is entered the same way as the standard word read. First a start bit is transmitted, followed by the op code for a read cycle and then the first address to be read. It is always necessary to define the first address to be read since the address register's state is not guaranteed.

Up until this point, the data out (DO) will remain in TRI-STATE®, but beginning with the same rising edge of the clock (SK) that clocks in address bit A0, the data out will drive a low level. This first bit is always a zero. Starting with the next clock, valid data will appear on the data out pin. The leading zero in the data field will only appear in the first word read in a sequential read sequence, all subsequent data words will be clocked out on the data out pin in an uninterrupted stream. Refer to Figure 1 for the timing sequence.

Any number of data words may be read with a single sequential read instruction. When the top of memory is reached it will automatically wrap around to address 0 and continue in the sequential read mode. Using this feature it would be possible to read the entire memory in an endless loop if desired.

The Memory Protect Register has no effect on Sequential Read. The Sequential Read will cross the write protection boundary and read to the top of the memory and cycle back to address 0 (possibly in the unprotected field) regardless of the Protect Register status.

To terminate a sequential read operation, the host must drop chip select (low). At any time CS is transitioned to a low, the current instruction will be terminated. It is not necessary to observe word boundaries when terminating a read or sequential read operation. It may be terminated at any time without affect on the EEPROM.

MEMORY PROTECT REGISTER

The protect register is a unique method of write protecting the contents of a variable number of memory registers. The basic concept is shown in Figure 2 using the NM93CS66 4096-bit EEPROM. For the other family members everything remains the same except the memory size and the corresponding maximum address that can be set in the protect register. One other difference that needs to be noted is the address length for the NM93CS06 and NM93CS46 is 6 bits and for the NM93CS56 and NM93CS66, 8 bits. The difference in address length produces a corresponding difference in length of the protect register.

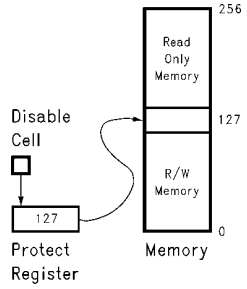

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FIGURE 2. Memory Protect Register

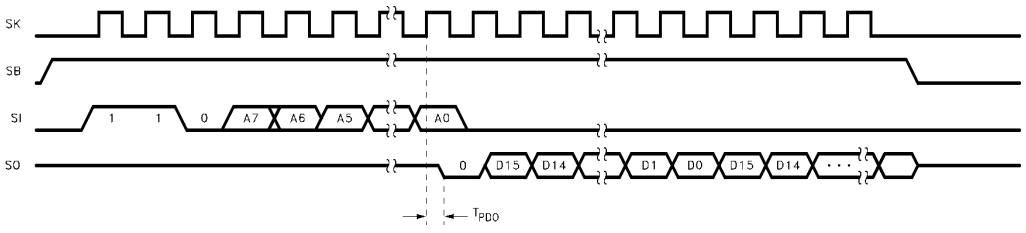

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FIGURE 1. Sequential Read Instruction Sequence

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There are two basic elements to the protection scheme, the Protect Register and the Disable Cell. Both the Protect Register and the Disable Cell are implemented in EEPROM latches, therefore do not require the introduction of additional technologies onto the die. The purpose of the Protect Register is to contain the address of the first write protected location in memory. The location in memory defined by the address written into the protect register and all others above that location, to the maximum address in memory are write protected.

The Protect Register is writable from the serial bus in a manner similar to writing a memory register, the only difference being the input PRE (Protect Register Enable) must be high and the instruction immediately preceding the write to the protect register must be a Protect Register Enable (PREN) instruction. By requiring this specific sequence and set of conditions, both hardware and software oriented, the chances of inadvertently changing the contents of the protect register or an unauthorized user changing the data without specific knowledge of the operation of the EEPROM are very remote.

The Disable Cell is a single EEPROM latch that may be set via a Protect Register Disable (PRDS) instruction. Like the Protect Register Write (PRWRITE) instruction, it must be executed with the input PRE high and immediately preceded by a PREN instruction. Once the Disable Cell is written, it cannot be cleared because the PRDS instruction is a one time only instruction. Once the PRDS instruction has been executed, the Protect Register cannot be updated again in the life of the part and the defined portion of memory is permanently protected.

A typical instruction sequence for storing manufacturing and factory calibration information in a NM93CS family part is shown as follows:

Instruction	Description
1.	Power On
2. WEN	Enable all programming instructions.
3. WRITE A(max)	Write maximum address location.
4. WRITE A(max-1)	Write maximum address location -1.
5. WRITE A(max-2)	Write max. address location -2.
:	:
:	:
:	:
6. WRITE A(max-y)	Write maximum address location -y.
7. PREN	Enable programming of Protect Register.
8. PRWRITE (A(max-y))	Write address (max-y) to Protect Register.
9. PREN	Enable programming of the Disable Cell.
10. PRDS	Disable all future programming of the protect register and protected memory.
11. WDS	Disable all programming instructions.

It is not necessary to do steps 9 and 10. The PRDS instruction makes the protection permanent. Without executing the PRDS instruction the option remains to remove the write protection thus allowing changing the data in the formerly protected portion of memory. The following sequence will remove the write protection and clear the contents of the Protect Register:

Instruction	Description
1. WEN	Enable all programming instruction.
2. PREN	Enable programming of the Protect Register.
3. PRCLEAR	Enable writing of all memory locations and clear the Protect Register.
4. WDS	Disable all programming instruction.

In both examples above the final step is a Write Disable (WDS) instruction. This instruction would normally be delayed until all programming is complete, but should be included as a minimal level of data protection for otherwise unprotected memory locations.

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