FAIRCHILD SEMICONDUCTOR™

October 1996
Revised August 2004

NC7SZ38
TinyLogic® UHS 2-Input NAND Gate (Open Drain Output)

General Description

The NC7SZ38 is a single 2-Input NAND Gate with open drain output stage from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage. The open drain output stage will tolerate voltages up to 6V independent of V_{CC} when in the high impedance state.

Features

- Space saving SOT23 or SC70 5-lead package
- Ultra small MicroPak™ leadless package
- Open Drain output stage for OR tied applications
- Ultra High Speed; t_{PD} 2.4 ns Typ into 50 pF at 5V V_{CC}
- High Output Sink Drive; 24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range; 1.65V to 5.5V
- Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/output
- Overvoltage Tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ38M5X	MA05B	7Z38	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ38P5X	MAA05A	Z38	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ38L6X	MAC06A	A6	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Pin Descriptions

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	*H
L	H	*H
H	L	*H
H	H	L

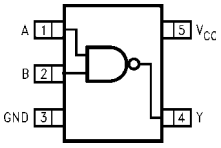
H = HIGH Logic Level L = LOW Logic Level
*H = HIGH Impedance output state (Open Drain)

Logic Symbol

IEEE/IEC

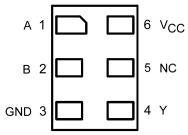
Connection Diagrams

Pin Assignments for SC70 and SOT23



(Top View)

Pad Assignment for MicroPak



(Top Thru View)

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MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +6V
DC Input Voltage (V_{IN})	−0.5V to +6V
DC Output Voltage (V_{OUT})	−0.5V to +6V
DC Input Diode Current (I_{IK})	
@V_{IN} < −0.5V	−50 mA
@ V_{IN} > 6V	+20 mA
DC Output Diode Current (I_{OK})	
@V_{OUT} < −0.5V	−50 mA
@ V_{OUT} > 6V, V_{CC} = GND	+20 mA
DC Output Current (I_{OUT})	+50 mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature under Bias (T_J)	150°C
Junction Lead Temperature (T1);	
(Soldering, 10 seconds)	260°C
Power Dissipation (P_D) @ +85°C	
SOT23-5	200 mW
SC70-5	150 mW

Recommended Operating Conditions (Note 2)

Supply Voltage Operating (V_{CC})	1.65V to 5.5V
Supply Voltage Data Retention (V_{CC})	1.5V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Operating Temperature (T_A)	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 1.8V, 2.5V ± 0.2V	0 ns/V to 20 ns/V
V_{CC} = 3.3V ± 0.3V	0 ns/V to 10 ns/V
V_{CC} = 5.0V ± 0.5V	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	
SOT23-5	300°C/W
SC70-5	425°C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V		
		2.3 to 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input Voltage	1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V		
		2.3 to 5.5			0.3 V_{CC}		0.3 V_{CC}			
I_{LKG}	HIGH Level Output Leakage	5.5			±5		±10	µA	V_{IN} = V_{IL} V_{OUT} = V_{CC} or GND	
V_{OL}	LOW Level Output Voltage	1.65		0.0	0.1		0.1	V	V_{IN} = V_{IH}	I_{OL} = 100 µA
		1.8		0.0	0.1		0.1			
		2.3		0.0	0.1		0.1			
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		1.65		0.08	0.24		0.24			
		2.3		0.10	0.3		0.3			I_{OL} = 8 mA
		3.0		0.15	0.4		0.4			I_{OL} = 16 mA
		3.0		0.22	0.55		0.55			I_{OL} = 24 mA
		4.5		0.22	0.55		0.55			I_{OL} = 32 mA
I_{IN}	Input Leakage Current	5.5			±1		±10	µA	V_{IN} = 5.5V, GND	
I_{OFF}	Power Off Leakage Current	0.0			1		10	µA	V_{IN} or V_{OUT} = 5.5V	
I_{CC}	Quiescent Supply Current	5.5			2.0		20	µA	V_{IN} = 5.5V, GND	

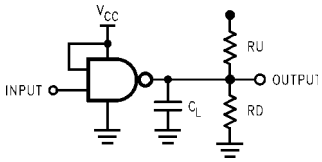
AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t_{PZL}	Propagation Delay	1.65	1.5	6.5	12.7	1.5	13.2	ns	$C_L = 50$ pF $RU = 500\Omega$ $RD = 500\Omega$ $V_I = 2 \times V_{CC}$	Figures 1, 3
		1.8	1.5	5.4	10.5	1.5	11.0			
		2.5 ± 0.2	0.8	3.5	7.0	0.8	7.5			
		3.3 ± 0.3	0.8	2.8	5.0	0.8	5.2			
		5.0 ± 0.5	0.5	2.2	4.3	0.5	4.5			
t_{PLZ}	Propagation Delay	1.65	1.5	5.5	12.7	1.5	13.2	ns	$C_L = 50$ pF $RU = 500\Omega$ $RD = 500\Omega$ $V_I = 2 \times V_{CC}$	Figures 1, 3
		1.8	1.5	4.6	10.5	1.5	11.0			
		2.5 ± 0.2	0.8	3.0	7.0	0.8	7.5			
		3.3 ± 0.3	0.8	2.1	5.0	0.8	5.2			
		5.0 ± 0.5	0.5	1.3	4.3	0.5	4.5			
C_{IN}	Input Capacitance	0		4				pF		
C_{OUT}	Output Capacitance	0		5						
C_{PD}	Power Dissipation Capacitance	3.3		5.1				pF	(Note 3)	Figure 2
		5.0		7.3						

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression:

$I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}$ static).

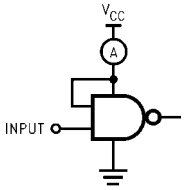
AC Loading and Waveforms



C_L includes load and stray capacitance

Input PRR = 1.0 MHz; t_w = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; $t_r = t_f = 1.8$ ns

PRR = 10 MHz; Duty Cycle = 50%

FIGURE 2. I_{CCD} Test Circuit

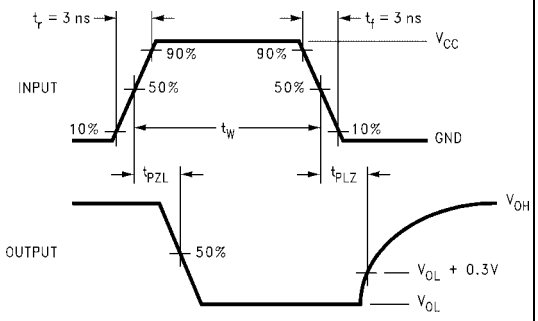


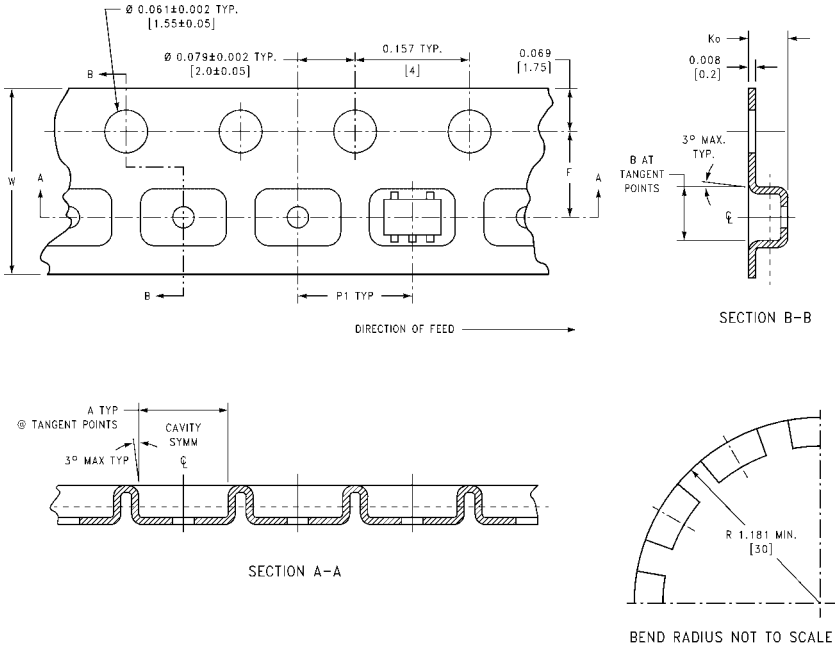
FIGURE 3. AC Waveforms

Tape and Reel Specification

TAPE FORMAT for SC70 and SOT23

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

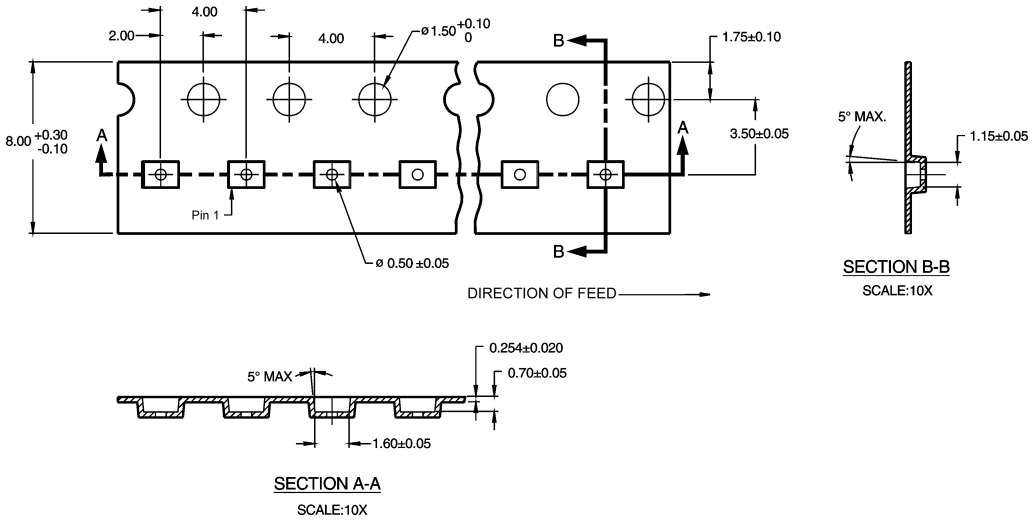


Package	Tape Size	DIM A	DIM B	DIM F	DIM K_o	DIM P1	DIM W
SC70-5	8 mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8 mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

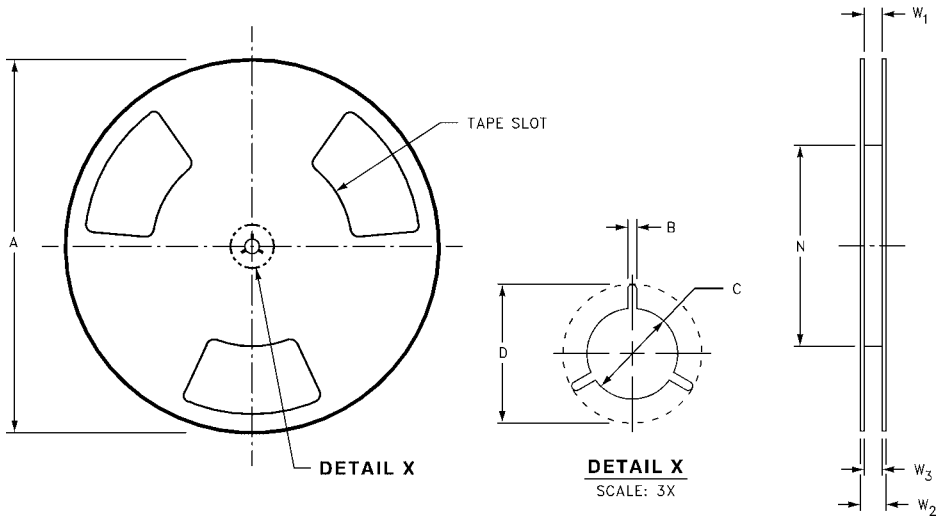
Tape and Reel Specification (Continued)

TAPE FORMAT for MircoPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

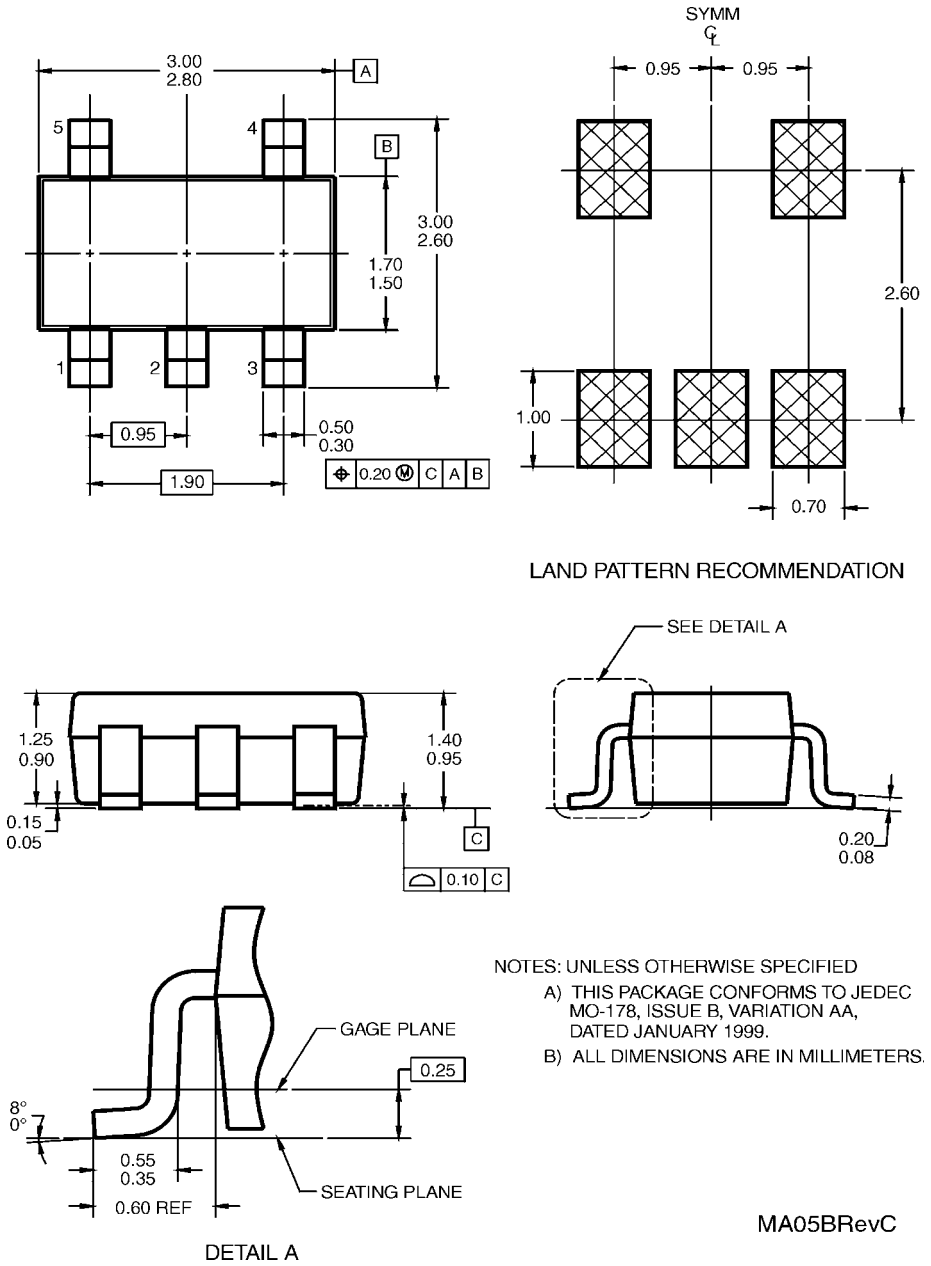


REEL DIMENSIONS inches (millimeters)



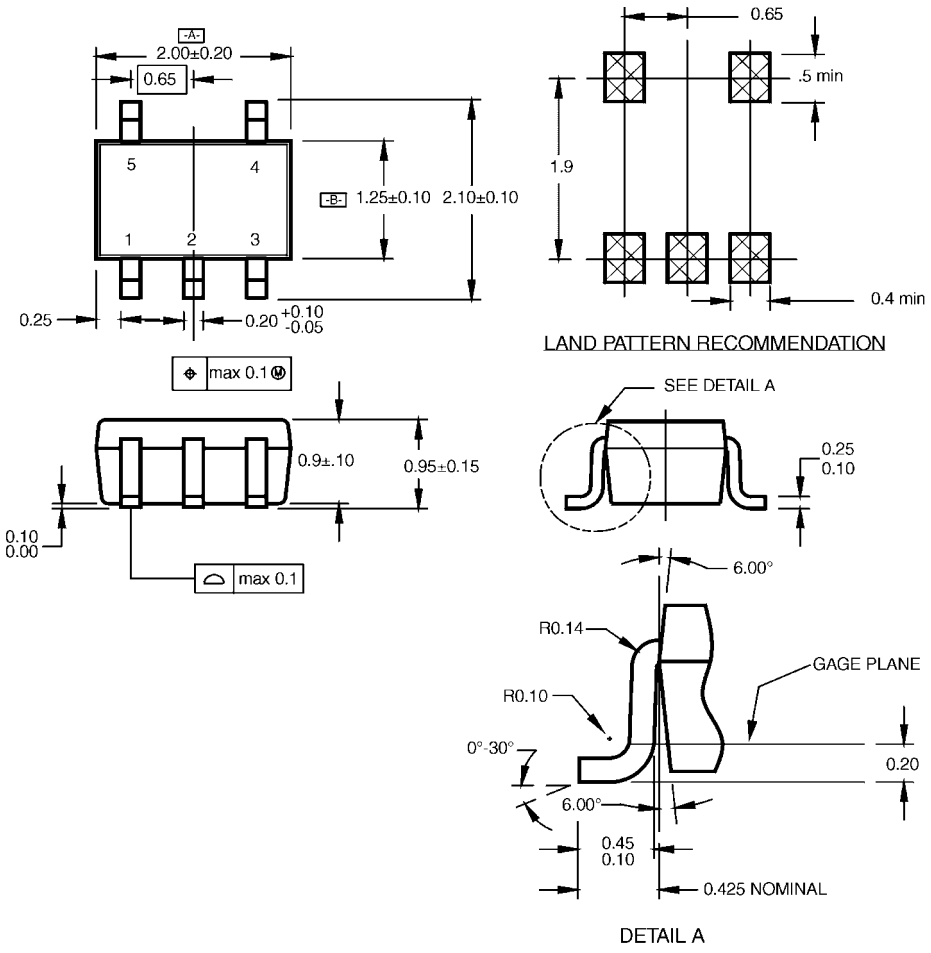
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



5-Lead SOT23, JEDEC MO-178, 1.6mm
Package Number MA05B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



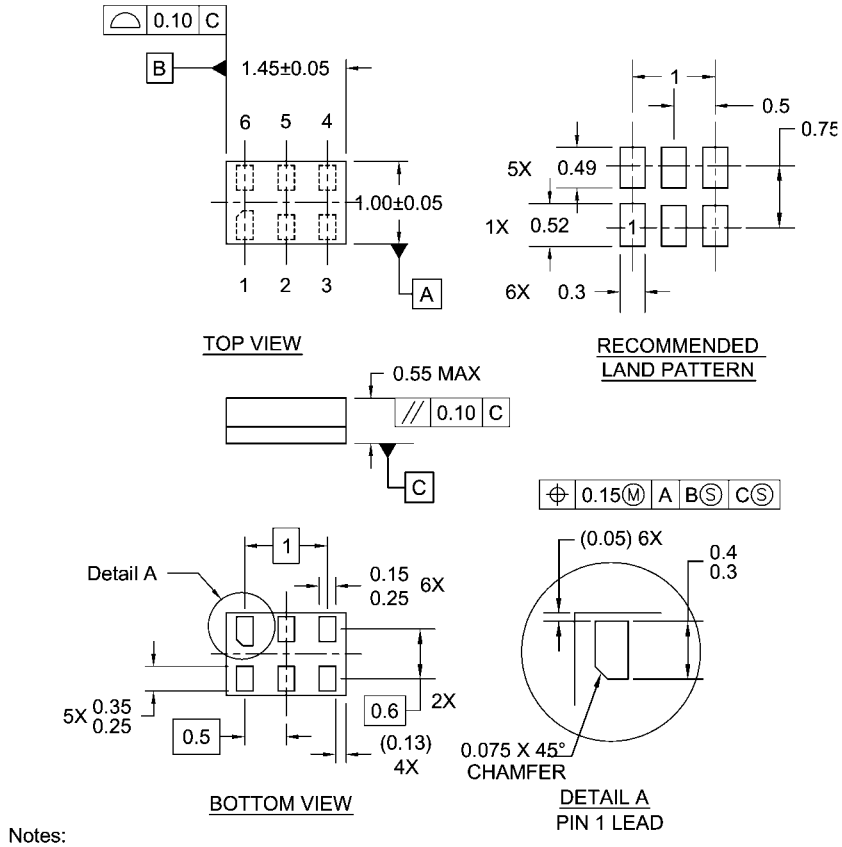
NOTES:

A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88A.
B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.
C. DIMENSIONS ARE IN MILLIMETERS.

MAA05ARevC

5-Lead SC70, EIAJ SC-88a, 1.25mm Wide
Package Number MAA05A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide
Package Number MAC06A