FAIRCHILD
SEMICONDUCTOR®

March 2008

NC7SZ00

TinyLogic® UHS 2-Input NAND Gate

Features

■ Space saving SOT23 or SC70 5-lead package

■ Ultra small MicroPak™ leadless package

■ Ultra High Speed; t_{PD} 2.4ns typ. into 50pF at 5V V_{CC}

■ High Output Drive; ±24mA at 3V V_{CC}

■ Broad V_{CC} Operating Range; 1.65V–5.5V

■ Matches the performance of LCX when operated at 3.3V V_{CC}

■ Power down high impedance inputs/output

■ Overvoltage tolerant inputs facilitate 5V to 3V translation

■ Patented noise/EMI reduction circuitry implemented

General Description

The NC7SZ00 is a single 2-Input NAND Gate from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a broad V_{CC} operating range. The device is specified to operate over the 1.65V to 5.5V V_{CC} operating range. The inputs and output are high impedance when V_{CC} is 0V. Inputs tolerate voltages up to 6V independent of V_{CC} operating voltage.

Ordering Information

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SZ00M5X	MA05B	7Z00	5-Lead SOT23, JEDEC MO-178, 1.6mm	3k Units on Tape and Reel
NC7SZ00P5X	MAA05A	Z00	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3k Units on Tape and Reel
NC7SZ00L6X	MAC06A	YY	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

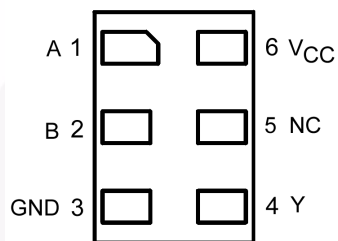🌱 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignments for SC70 and SOT23
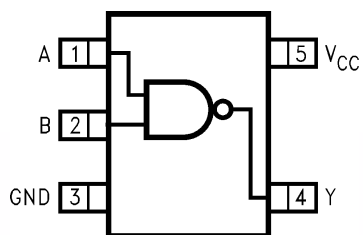
(Top View)

Pad Assignment for MicroPak

(Top Thru View)

Logic Symbol

IEEE/IEC

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level

L = LOW Logic Level

Pin Description

Pin Names	Description
A, B	Inputs
Y	Output
NC	No Connect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +6V
V_{IN}	DC Input Voltage	–0.5V to +6V
V_{OUT}	DC Output Voltage	–0.5V to +6V

I_{IK}	DC Input Diode Current
	    @ $V_{IN} < -0.5V$
	    @ $V_{IN} > 6V$
		
		–50mA
		+20mA

I_{OK}	DC Output Diode Current
	    @ $V_{OUT} < -0.5V$
	    @ $V_{OUT} > 6V$, $V_{CC} = GND$
		
		–50mA
		+20mA

I_{OUT}	DC Output Current	±50mA
I_{CC}/I_{GND}	DC V_{CC}/GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_J	Junction Temperature under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C

P_D	Power Dissipation @ +85°C
	    SOT23-5
	    SC70-5
		
		200mW
		150mW

Recommended Operating Conditions[1]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage Operation	1.65V to 5.5V
V_{CC}	Supply Voltage Data Retention	1.5V to 5.5V
V_{IN}	Input Voltage	0V to 5.5V
V_{OUT}	Output Voltage	0V to V_{CC}
T_A	Operating Temperature	–40°C to +85°C

t_r, t_f	Input Rise and Fall Time
	    V_{CC} @ 1.8V, 2.5V ± 0.2V
	    V_{CC} @ 3.3V ± 0.3V
	    V_{CC} @ 5.0V ± 0.5V
		
		0ns/V to 20ns/V
		0ns/V to 10ns/V
		0ns/V to 5ns/V

θ_{JA}	Thermal Resistance
	    SOT23-5
	    SC70-5
		
		300°C/W
		425°C/W

Notes:

1. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40°C to +85°C		Unit
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	1.65–1.95			0.75 x V_{CC}			0.75 x V_{CC}		V
		2.3–5.5			0.70 x V_{CC}			0.70 x V_{CC}		
V_{IL}	LOW Level Input Voltage	1.65–1.95					0.25 x V_{CC}		0.25 x V_{CC}	V
		2.3–5.5					0.30 x V_{CC}		0.30 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	1.65	$V_{IN} = V_{IL}$	$I_{OH} = -100\mu A$	1.55	1.65		1.55		V
		1.8			1.7	1.8		1.7		
		2.3			2.2	2.3		2.2		
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		1.65		$I_{OH} = -4mA$	1.29	1.52		1.29		
		2.3		$I_{OH} = -8mA$	1.9	2.15		1.9		
		3.0		$I_{OH} = -16mA$	2.4	2.80		2.4		
		3.0		$I_{OH} = -24mA$	2.3	2.68		2.3		
		4.5		$I_{OH} = -32mA$	3.8	4.20		3.8		
V_{OL}	LOW Level Output Voltage	1.65	$V_{IN} = V_{IH}$	$I_{OL} = 100\mu A$		0.0	0.1		0.08	V
		1.8				0.0	0.1		0.1	
		2.3				0.0	0.1		0.1	
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		1.65		$I_{OL} = 4mA$		0.08	0.24		0.24	
		2.3		$I_{OL} = 8mA$		0.10	0.3		0.3	
		3.0		$I_{OL} = 16mA$		0.15	0.4		0.4	
		3.0		$I_{OL} = 24mA$		0.22	0.55		0.55	
		4.5		$I_{OL} = 32mA$		0.22	0.55		0.55	
I_{IN}	Input Leakage Current	0–5.5	$V_{IN} = 5.5V$, GND				±1		±10	µA
I_{OFF}	Power Off Leakage Current	0.0	V_{IN} or $V_{OUT} = 5.5V$				1		10	µA
I_{CC}	Quiescent Supply Current	1.65–5.5	$V_{IN} = 5.5V$, GND				2.0		20	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C			T_A = −40°C to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PHL}	Propagation Delay	1.65	C_L = 15pF, R_L = 1MΩ	2.0	5.4	11.4	2.0	12	ns	Figure 1 Figure 3
		1.8		2.0	4.5	9.5	2.0	10.0		
		2.5 ± 0.2		0.8	3.0	6.5	0.8	7.0		
		3.3 ± 0.3		0.5	2.4	4.5	0.5	4.7		
		5.0 ± 0.5		0.5	2.0	3.9	0.5	4.1		
t_{PLH}, t_{PHL}	Propagation Delay	3.3 ± 0.3	C_L = 50pF, R_L = 500Ω	1.5	2.9	5.0	1.5	5.2	ns	Figure 1 Figure 3
		5.0 ± 0.5		0.8	2.4	4.3	0.8	4.5		
C_{IN}	Input Capacitance	0			4				pF	
C_{PD}	Power Dissipation Capacitance	3.3	(2)		24				pF	Figure 2
		5.0			30					

Note:

2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{IN}) + (I_{CC}\text{static})$.

AC Loading and Waveforms
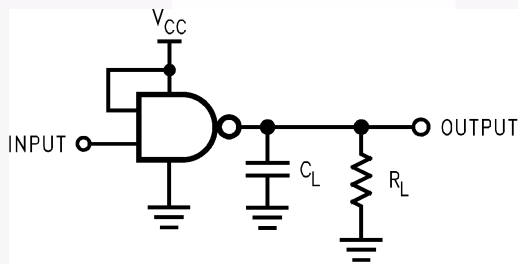
C_L includes load and stray capacitance
Input PRR = 1.0MHz; t_w = 500ns
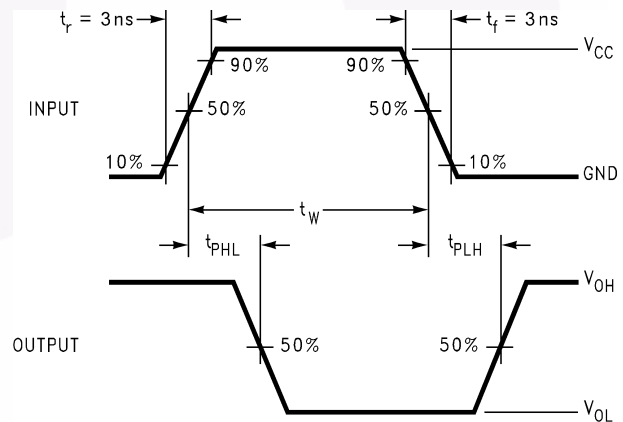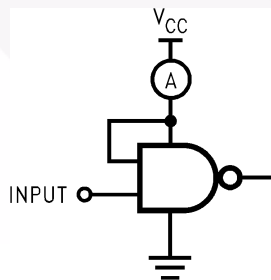
Figure 1. AC Test Circuit

Figure 3. AC Waveforms

Input = AC Waveform; $t_r = t_f$ = 1.8ns;
PRR = 10MHz; Duty Cycle = 50%

Figure 2. I_{CCD} Test Circuit

Tape and Reel Specifications

Tape Format for SC70 and SOT23

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
M5X, P5X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

Tape Dimensions inches (millimeters)

SECTION B-B

SECTION A-A

BEND RADIUS NOT TO SCALE
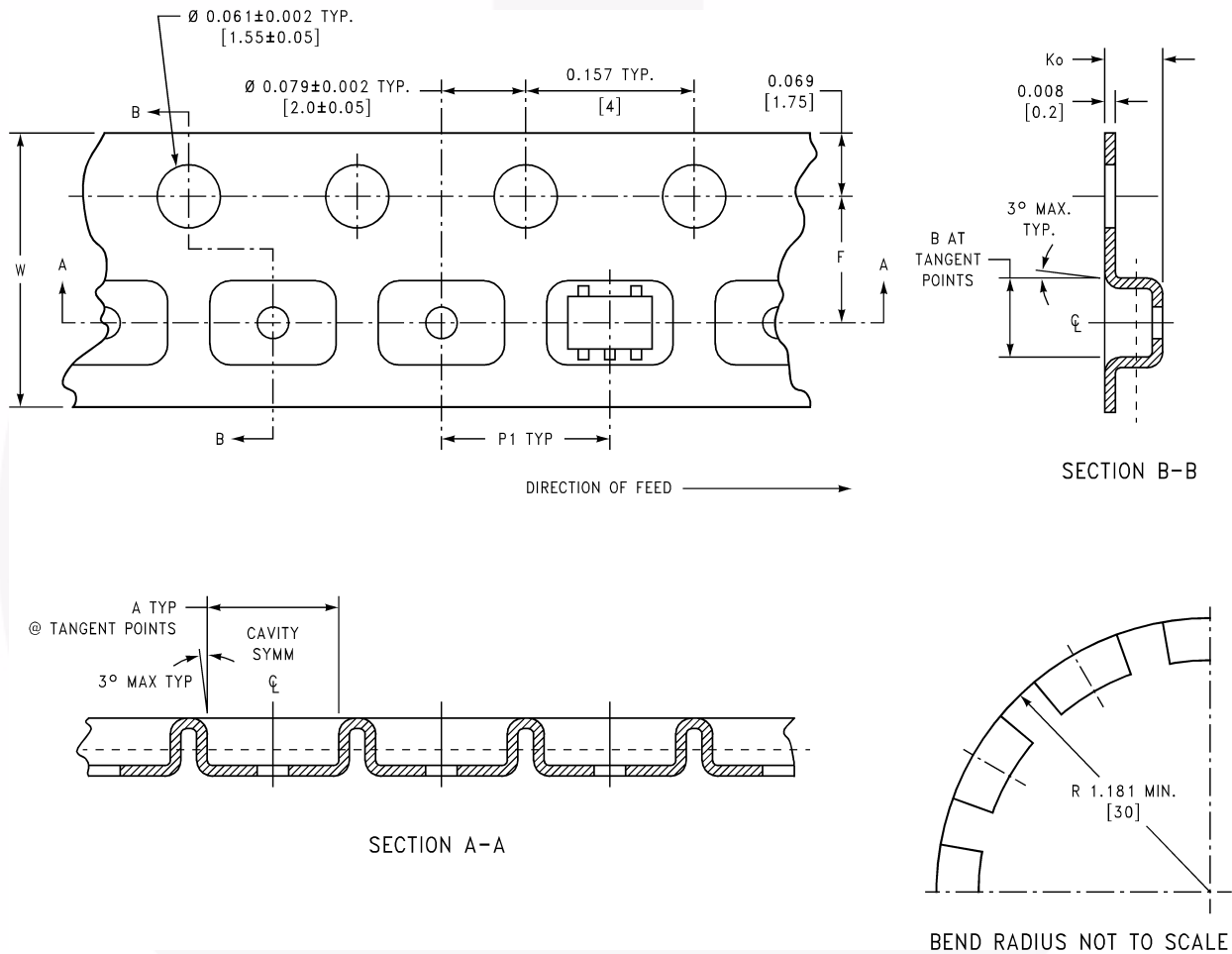
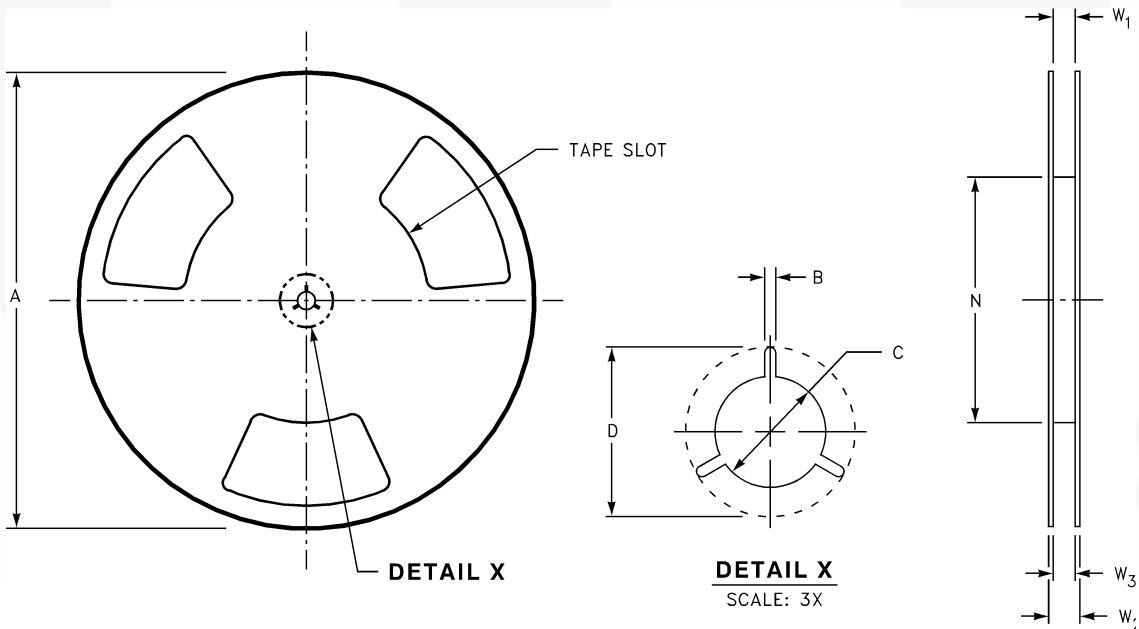| Package	Tape Size	Dim A	Dim B	Dim F	Dim K$_O$	Dim P1	Dim W
SC70-5	8mm	0.093 (2.35)	0.096 (2.45)	0.138 ± 0.004 (3.5 ± 0.10)	0.053 ± 0.004 (1.35 ± 0.10)	0.157 (4)	0.315 ± 0.004 (8 ± 0.1)
SOT23-5	8mm	0.130 (3.3)	0.130 (3.3)	0.138 ± 0.002 (3.5 ± 0.05)	0.055 ± 0.004 (1.4 ± 0.11)	0.157 (4)	0.315 ± 0.012 (8 ± 0.3)

Tape and Reel Specifications (Continued)

Tape Format for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L6X	Leader (Start End)	125 (typ.)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ.)	Empty	Sealed

SECTION B-B
SCALE:10X

SECTION A-A
SCALE:10X

DIRECTION OF FEED
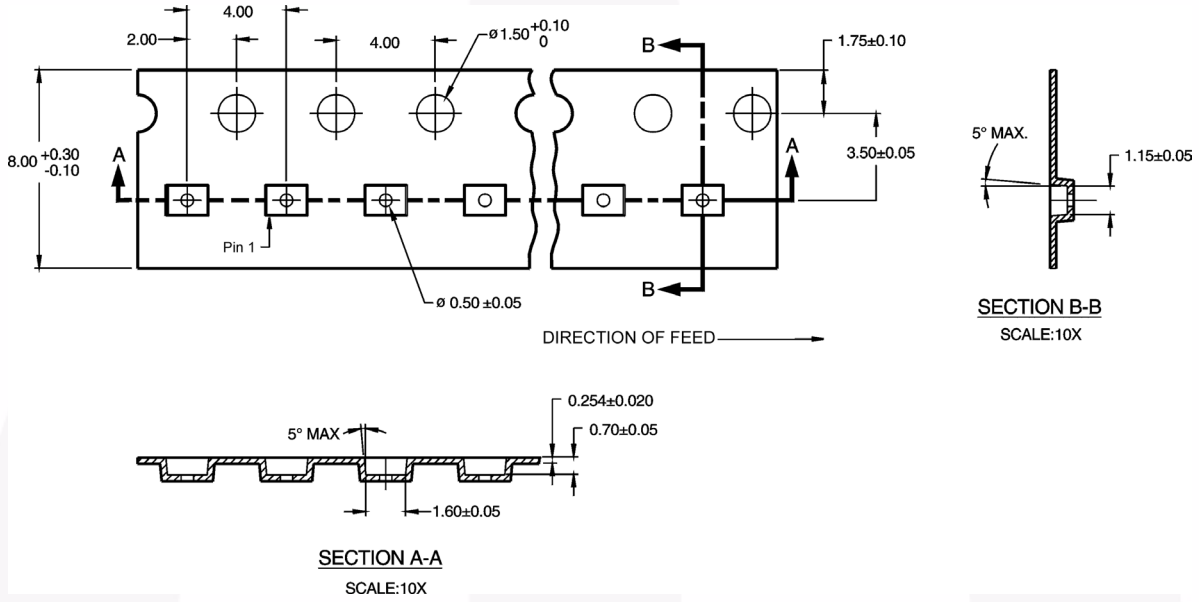
Reel Dimensions inches (millimeters)

TAPE SLOT

DETAIL X

DETAIL X
SCALE: 3X

Tape Size	A	B	C	D	N	W1	W2	W3
8mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions

TOP VIEW

LAND PATTERN RECOMMENDATION

SEE DETAIL A

GAGE PLANE

0.25

8°
0°

0.55
0.35

0.60 REF

SEATING PLANE

NOTES: UNLESS OTHEWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
    MO-178, ISSUE B, VARIATION AA,
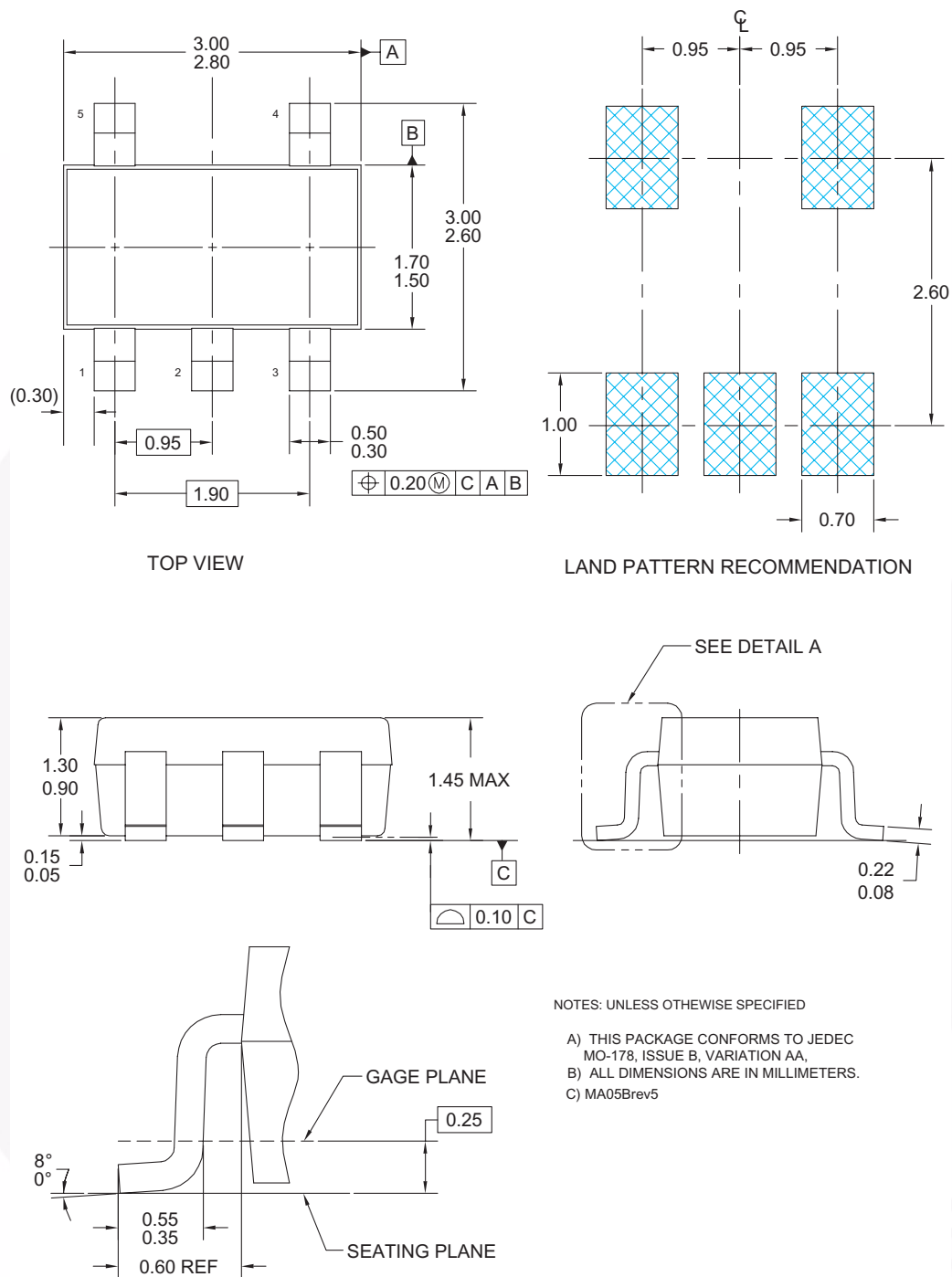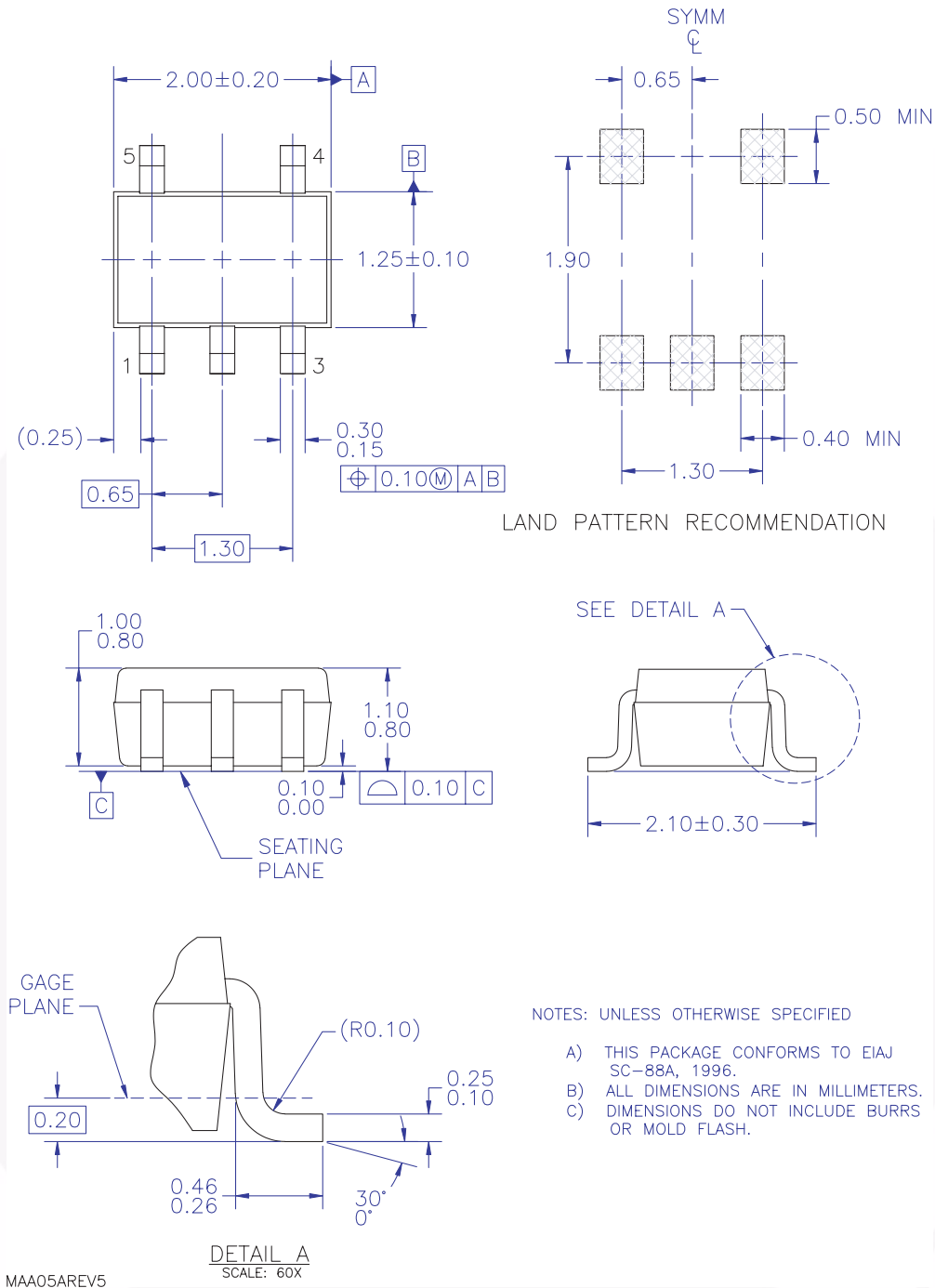B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) MA05Brev5

Figure 4. 5-Lead SOT23, JEDEC MO-178, 1.6mm

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Physical Dimensions (Continued)

2.00±0.20 [A]

5   4   [B]

1.25±0.10

1   3

(0.25)

0.30
0.15

0.65

[⊕ | 0.10 (M) | A | B]

1.30

SYMM
C

0.65

0.50 MIN

1.90

0.40 MIN

1.30

LAND PATTERN RECOMMENDATION

1.00
0.80

1.10
0.80

0.10
0.00

[⌒ | 0.10 | C]

[C]

SEATING
PLANE

SEE DETAIL A

2.10±0.30

GAGE
PLANE

(R0.10)

0.25
0.10

[0.20]

0.46
0.26

30°
0°

DETAIL A
SCALE: 60X

MAA05AREV5

NOTES: UNLESS OTHERWISE SPECIFIED

A)   THIS PACKAGE CONFORMS TO EIAJ
     SC—88a, 1996.
B)   ALL DIMENSIONS ARE IN MILLIMETERS.
C)   DIMENSIONS DO NOT INCLUDE BURRS
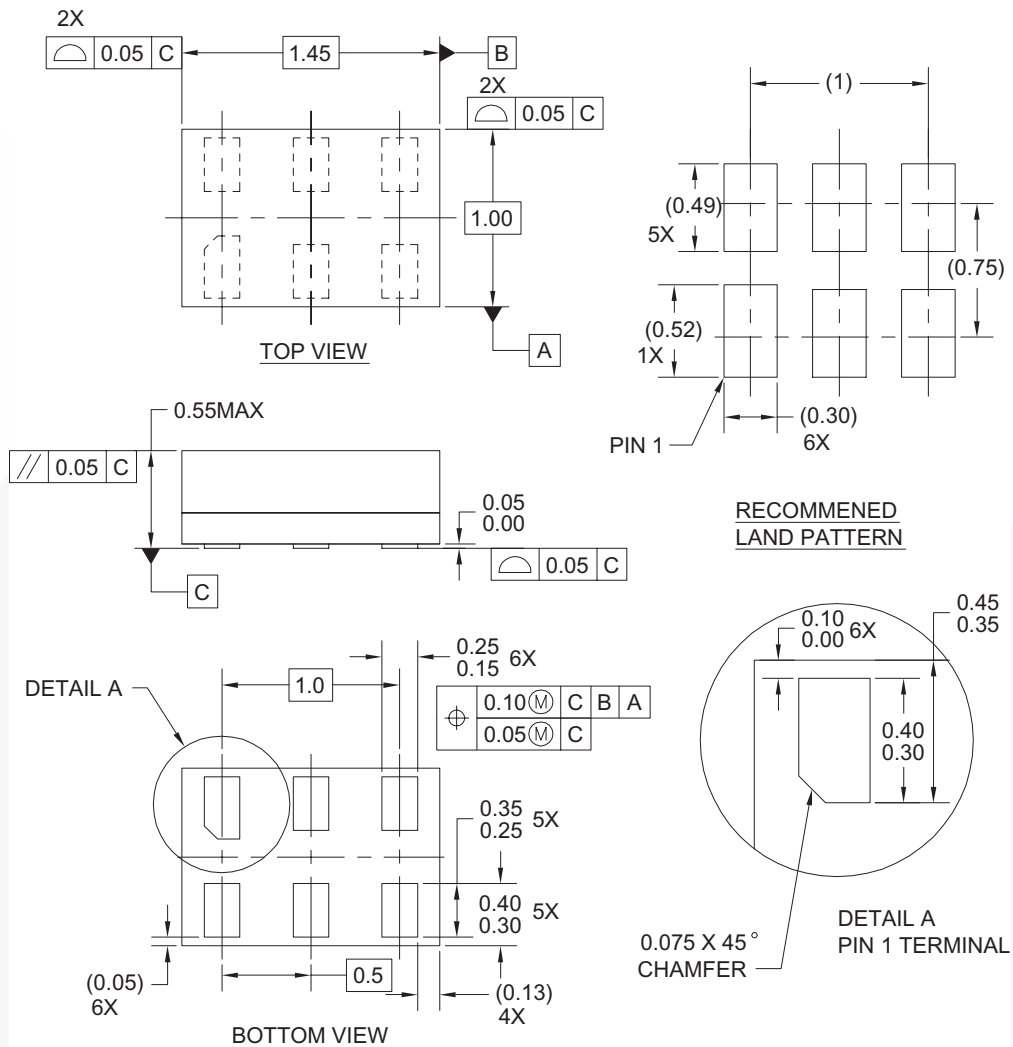   OR MOLD FLASH.

Figure 5. 5-Lead SC70, EIAJ SC-88a, 1.25mm Wide

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Physical Dimensions (Continued)

2X

| ⌒ | 0.05 | C |

1.45

B

2X

| ⌒ | 0.05 | C |

1.00

A

TOP VIEW

0.55MAX

| ∥ | 0.05 | C |

0.05
0.00

| ⌒ | 0.05 | C |

C

(1)

(0.49)
5X

(0.75)

(0.52)
1X

(0.30)
6X

PIN 1

RECOMMENED
LAND PATTERN

DETAIL A

1.0

0.25 6X
0.15

| ⊕ | 0.10 Ⓜ | C B A |
| | 0.05 Ⓜ | C |

0.35 5X
0.25

0.40 5X
0.30

(0.05)
6X

0.5

(0.13)
4X

BOTTOM VIEW

0.10 6X
0.00

0.45
0.35

0.40
0.30

DETAIL A
PIN 1 TERMINAL

0.075 X 45°
CHAMFER

Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06AREVC

Figure 6. 6-Lead MicroPak, 1.0mm Wide

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