National Semiconductor

LMP8270
High Common Mode, Gain of 20, Precision Voltage Difference Amplifier

General Description

The LMP8270 is a fixed gain differential amplifier with a −2V to 27V input common mode voltage range and a supply voltage range of 4.75V to 5.5V. The LMP8270 is part of the LMP™ precision amplifier family which will detect, amplify and filter small differential signals in the presence of high common mode voltages. The gain is fixed at 20 and is adequate to drive an ADC to full scale in most cases. This gain is achieved in two stages, a preamplifier with a fixed gain of 10 and a second stage amplifier with a fixed gain of 2. The internal signal path between these two stages is brought out on two pins, A1 and A2, which provide a connection for a filter network.

The LMP8270 will operate with reduced specifications over the extended common mode input voltage range of −2V to 36V. This feature makes the device suitable for applications with load dump in automotive systems.

Features

Typical Values, T_A = 25˚C

- Input offset voltage — ±1 mV max
- TCV_{OS} — ±15 µV/˚C max
- CMRR — 80 dB min
- Extended CMVR — −2V to 36V
- Output voltage swing — Rail-to-rail
- Bandwidth — 80 kHz
- Operating temperature range (ambient) — −40˚C to 125˚C
- Supply voltage — 4.75V to 5.5V
- Supply current — 1 mA

Applications

- Fuel injection control
- High and low side driver configuration current sensing
- Power management systems

Typical Application

Low Side Current Sensing

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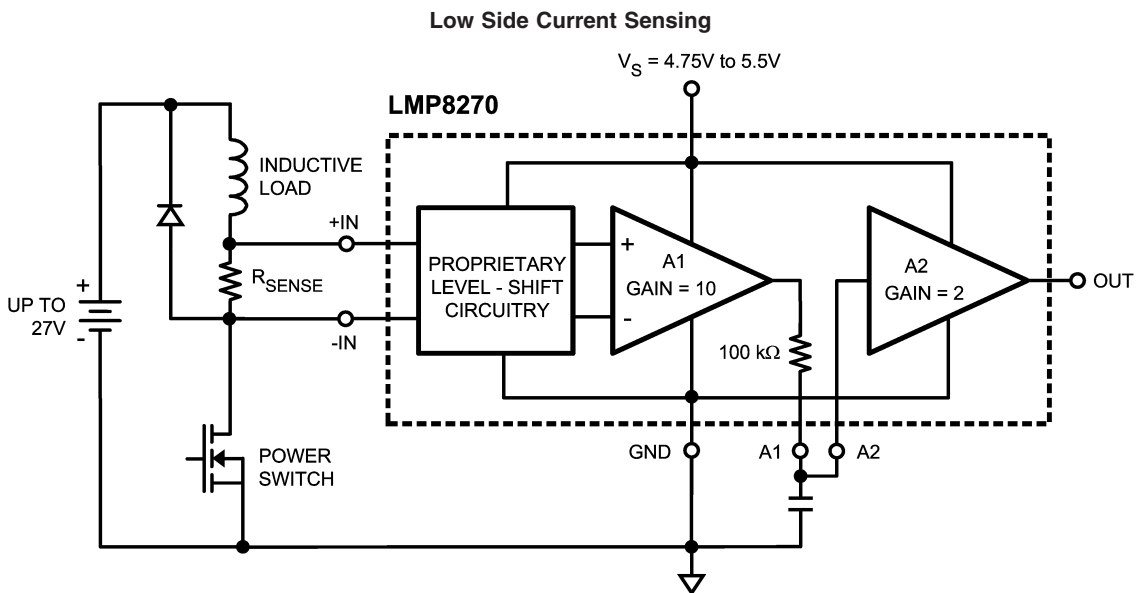
Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	
For +IN and −IN	±4000V
For all other pins	±2000V
Machine Model	200V
Supply Voltage (V_S - GND)	5.75V
Voltage on +IN and −IN	−5V to 42V
Transient (400 ms)	−7V to 45V
Storage Temperature Range	−65°C to +150°C

Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range	
Packaged Device (Note 3)	−40°C to +125°C
Supply Voltage (V_S - GND)	4.75V to 5.5V
Package Thermal Resistance (θ_{JA} (Note 3))	
8-Pin SOIC	190°C/W

5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_S = 5V, GND = 0V, −2V ≤ V_{CM} ≤ 27V, R_L = Open. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_{OS}	Input Offset Voltage	V_{CM} = V_S/2 (Note 6)			±0.25	±1.0	mV
TCV_{OS}	Input Offset Voltage Drift	V_{CM} = V_S/2	25°C ≤ T_A ≤ 125°C		±6	**±15**	µV/°C
			−40°C ≤ T_A ≤ 25°C		±6	**±20**	
A2 I_B	Input Bias Current of A2	(Note 7)			−20		pA
						±20	nA
I_S	Supply Current				1.0	1.2	mA
						1.4	
R_{CM}	Input Impedance Common Mode			**160**	200	**240**	kΩ
R_{DM}	Input Impedance Differential Mode			**320**	400	**480**	kΩ
CMVR	Input Common-Mode Voltage Range			**−2**		**+27**	V
ECMVR	Extended Common-Mode Voltage Range			−2		36	V
DC CMRR	DC Common Mode Rejection Ratio	0°C ≤ T_A ≤ 125°C	−2V ≤ V_{CM} ≤ 27V	**80**	103		dB
			−2V ≤ V_{CM} ≤ 36V	**60**			
		−40°C ≤ T_A ≤ 0°C	−2V ≤ V_{CM} ≤ 27V	**77**			
			−2V ≤ V_{CM} ≤ 36V	**60**			
AC CMRR	AC Common Mode Rejection Ratio (Note 8)	−2V ≤ V_{CM} ≤ 27V	f = 1 kHz	80	95		dB
			f = 10 kHz		78		
PSRR	Power Supply Rejection Ratio	4.75V ≤ V_S ≤ 5.5V		**70**	80		dB
$R_{F\text{-}INT}$	Filter Resistor			**97**	100	**103**	kΩ
$TCR_{F\text{-}INT}$	Filter Resistor Drift				±20		ppm/°C
A_V	Total Gain			19.8	20	20.2	V/V
	Gain Drift				±2	**±25**	ppm/°C
A_{V1}	A1 Gain			9.9	10	10.1	V/V
A_{V2}	A2 Gain			1.98	2	2.02	V/V
A1 V_{OUT}	A1 Output Voltage Swing	VOL			0.004	0.01	V
		VOH		4.80	4.95		
A2 V_{OUT}	A2 Output Voltage Swing (Notes 9, 10)	R_L = 100 kΩ on Output	VOL		0.007	0.02	V
			VOH	4.80	4.99		
		R_L = 10 kΩ on Output	VOL		0.03		V
			VOH		4.95		
SR	Slew Rate (Note 11)				0.7		V/µs

5V Electrical Characteristics (Note 4) (Continued)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_S = 5V, GND = 0V, −2V ≤ V_{CM} ≤ 27V, R_L = Open. **Bold-face** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
BW	Bandwidth			80		kHz
Noise	0.1 Hz to 10 Hz			5.7		μV_{PP}
	Spectral Density	f = 1 kHz		452		nV/$\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model is 1.5 kΩ in series with 100 pF. Machine Model is 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Note 5: Typical values represent the parametric norm at the time of characterization.

Note 6: The V_{OS} maximum limit indicated does not include effects of lifetime drift, see Application Note.

**Note 7:** Positive current corresponds to current flowing into the device.

Note 8: AC Common Mode Signal is a 24 V_{PP} sine-wave (0V to 24V) at the given frequency.

Note 9: For VOL, R_L is connected to V_S and for VOH, R_L is connected to GND.

Note 10: For this test input is driven from A1 stage.

Note 11: Slew rate is the average of the rising and falling slew rates.
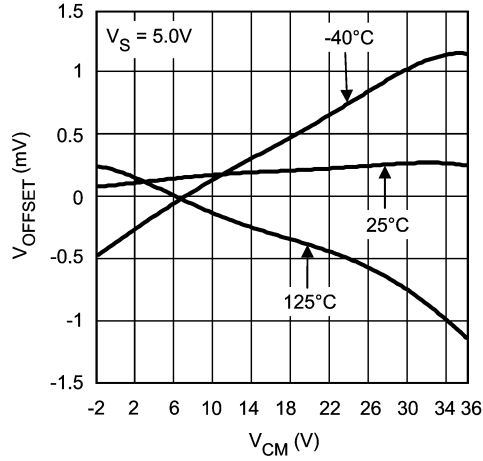
Connection Diagram

Top View
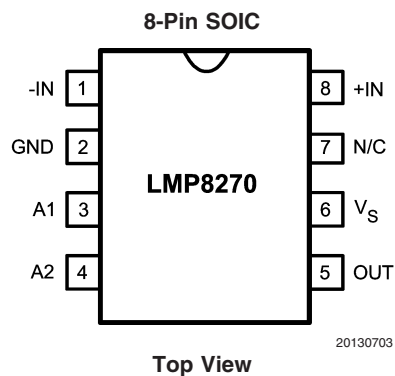
Ordering Information

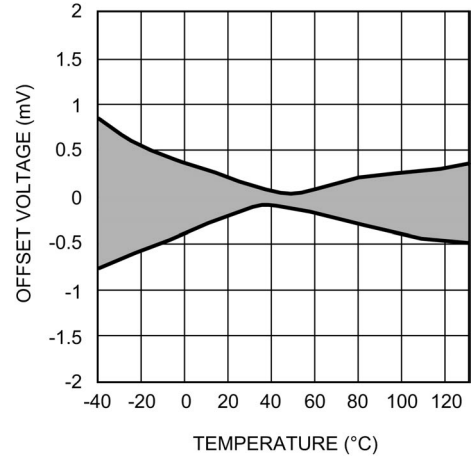| Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMP8270MA	LMP8270MA	95 Units/Rail	M08A
	LMP8270MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics
Unless otherwise specified: $T_A = 25°C$, $V_S = 5V$, $V_{CM} = V_S/2$

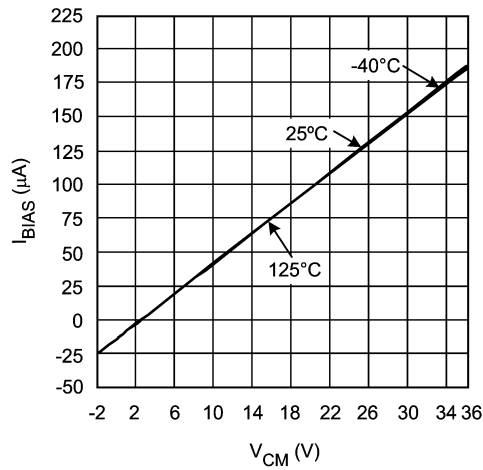### V_{OS} vs. V_{CM} Over Temperature

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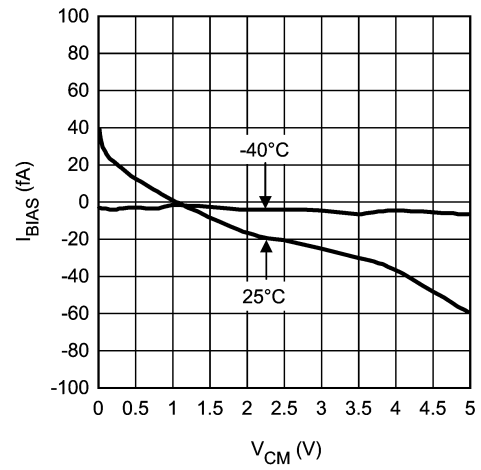### Typical V_{OS} vs. Temperature

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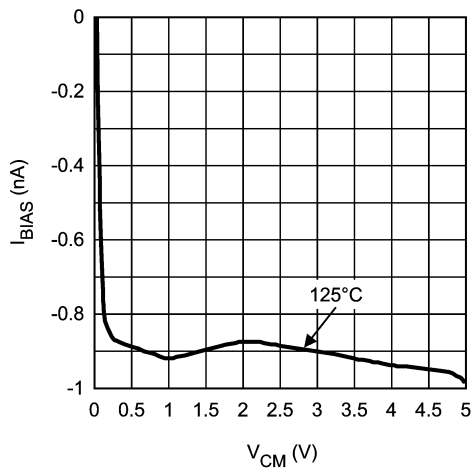### Input Bias Current Over Temperature (A1 Inputs)

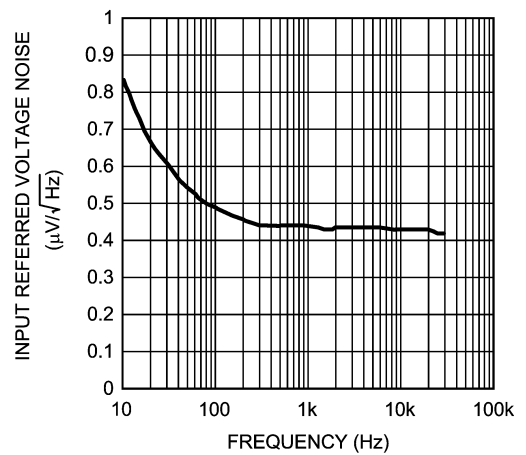20130728

Input Bias Current Over Temperature (A2 Input)

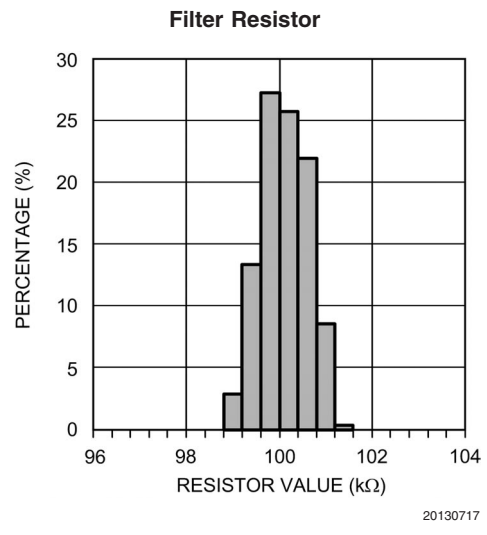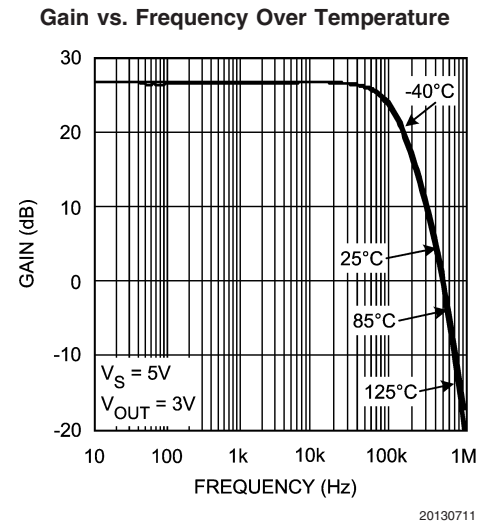20130718

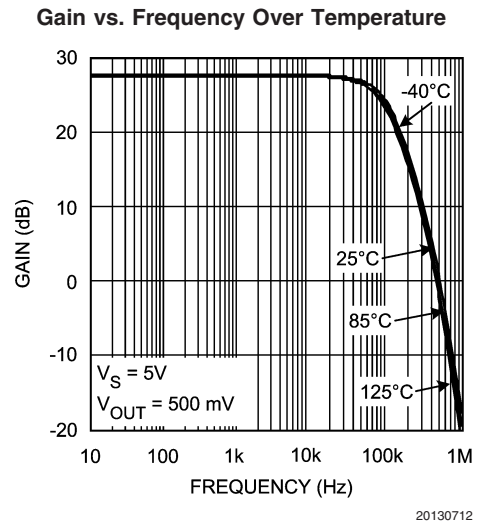### Input Bias Current Over Temperature (A2 Input)
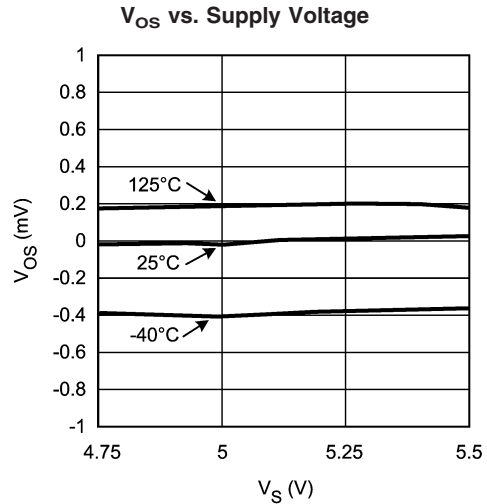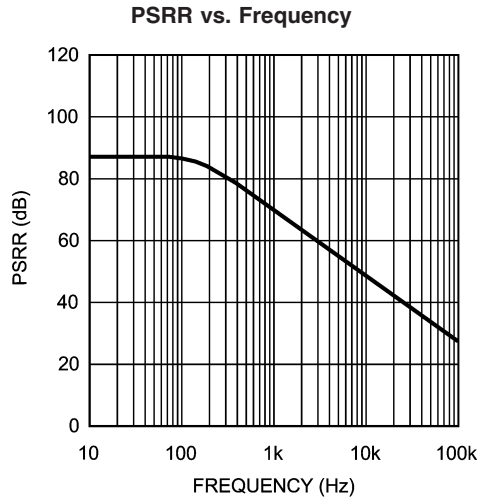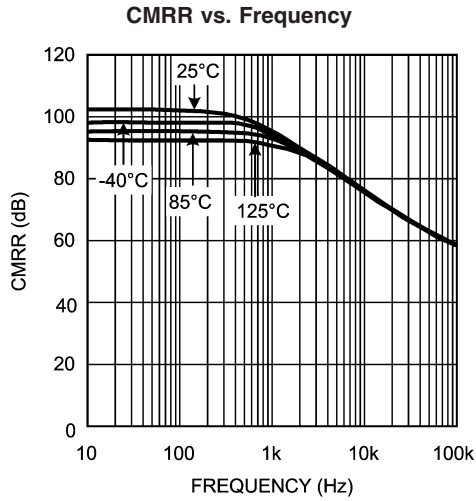

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Input Referred Voltage Noise vs. Frequency

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Typical Performance Characteristics Unless otherwise specified: $T_A = 25°C$, $V_S = 5V$, $V_{CM} = V_S/2$
(Continued)

PSRR vs. Frequency

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V_{OS} vs. Supply Voltage

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Gain vs. Frequency Over Temperature

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Gain vs. Frequency Over Temperature

20130711

Offset Voltage Distribution

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Filter Resistor

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Typical Performance Characteristics Unless otherwise specified: T_A = 25°C, V_S = 5V, V_{CM} = V_S/2

(Continued)

CMRR vs. Frequency

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Step Response

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Settling Time (Rising Edge)

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Settling Time (Falling Edge)

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Output Voltage Swing vs. R_L to V_S

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Output Voltage Swing vs. R_L to GND
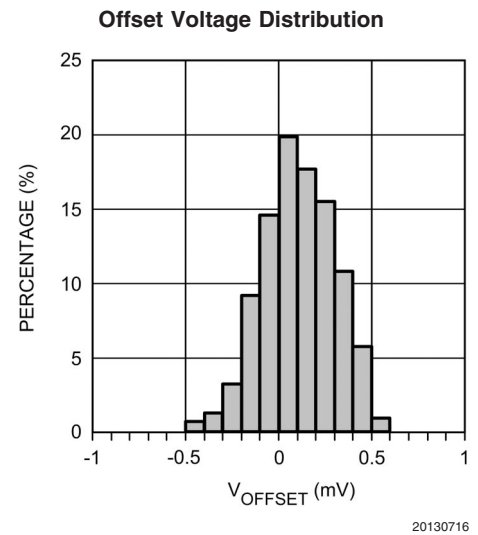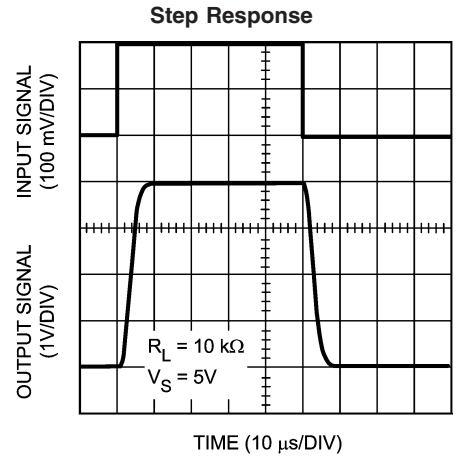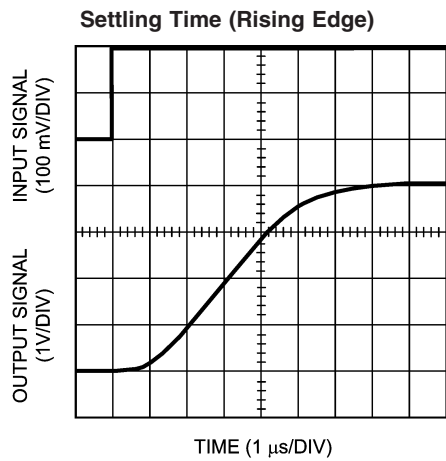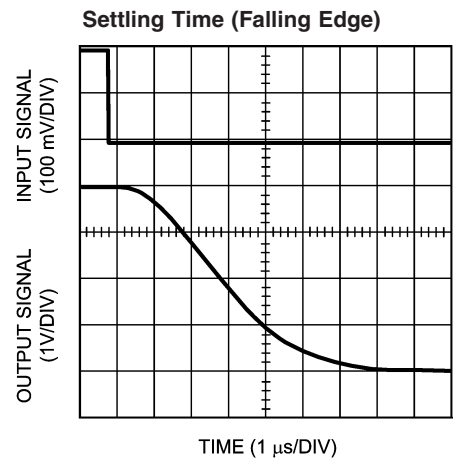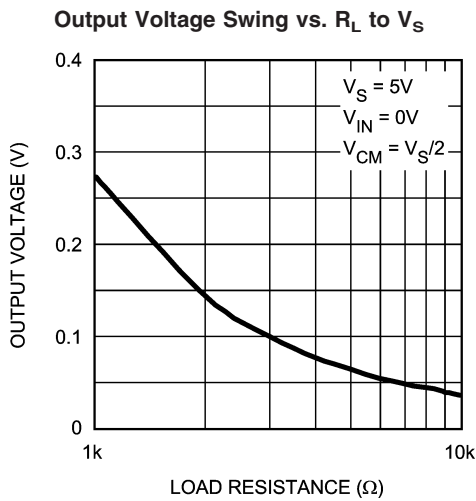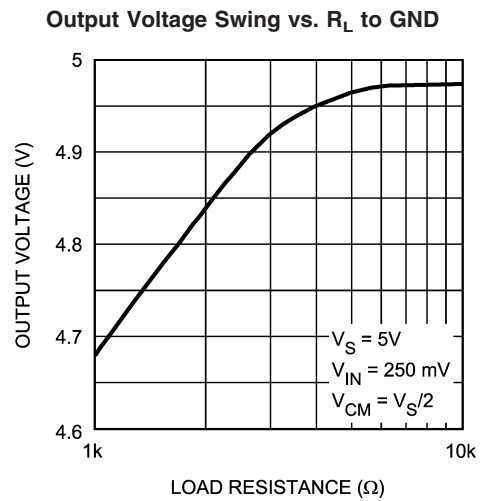

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Application Note

LMP8270

The LMP8270 is a single supply amplifier with a fixed gain of 20 and an extended common mode voltage range of −2V to 36V. The fixed gain is achieved in two separate stages, a preamplifier with gain of +10 and a second stage amplifier with gain of +2. A block diagram of the LMP8270 is shown in *Figure 1*.
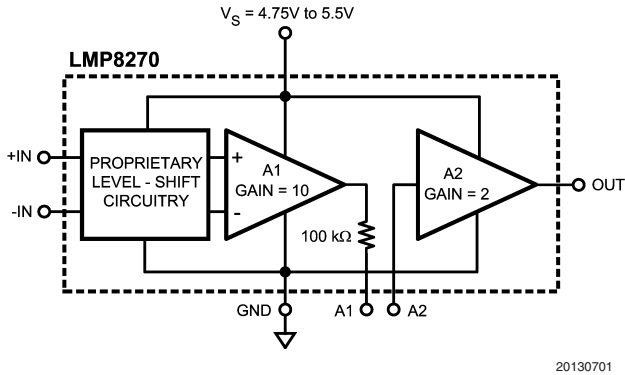

FIGURE 1. LMP8270

The overall offset of the LMP8270 is minimized by trimming amplifier A1. This is done in such a way that the output referred offset of A1 cancels the input referred offset of A2 or $10V_{OS1} = -V_{OS2}$.

Because of this offset voltage relationship, the offset of each individual amplifier stage may be more than the limit specified for the overall system in the datasheet tables. If the signal going from A1 to A2 is amplified or attenuated (by use of amplifiers and resistors), the overall LMP8270 offset will be affected as a result. Filtering the signal between A1 and A2 or simply connecting the two pins will not change the offset of the LMP8270.

Referencing the input referred offset voltages of each input stage, the following relationship holds:

$$\frac{(10V_{OS1}) + (V_{OS2})}{10} = V_{OS} \text{ (LMP8270)}$$

If the signal on pin 3 is scaled, attenuated or amplified, by a factor **X**, then the offset of the overall system will become:

$$\frac{(10V_{OS1}) \times (X) + (V_{OS2})}{10 \ (X)} = V_{OS} \text{ (LMP8270)}$$

LIFETIME DRIFT

Input Offset Voltage is an electrical parameter which may drift over time. This drift, known as lifetime drift, is very common in operational amplifiers; however, its effect is more evident in precision amplifiers. This is due to the very low Input Offset Voltage specifications in these amplifiers.

Numerous reliability tests have been performed to characterize this drift for the LMP8270. Prior to each long term reliability test the Input Offset Voltage of the LMP8270 was measured at room temperature. The LMP8270 was then subjected to a preconditioning sequence consisting of a 16

hour bake at 125˚C; an unbiased 168 hour Temperature Humidity Storage Test, THST, at 85˚C and 85% humidity; four passes of infra-red reflow with a maximum temperature of 260˚C; and finally one hundred 30 min Temperature Cycles, TMCL, between −65˚C and 150˚C (15 min at each temperature).

The long term reliability tests include Operating Life Time, OPL, performed at 150˚C for an extended period of time; Temperature Humidity Bias Testing, THBT, at 85˚C and 85% humidity for an extended period of time and repeated cycles of TMCL.

The Offset Voltage was measured again after each reliability test at room temperature. The Offset Voltage Drift is the difference between the initial measurement, before preconditioning, and the later measurement, post preconditioning and reliability test.

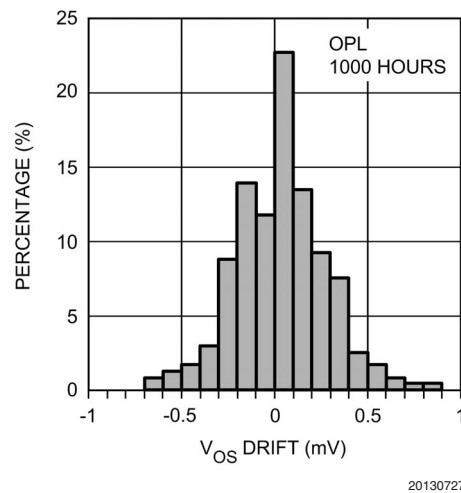*Figure 2* below shows the offset voltage drift after preconditioning and 1000 hours of OPL.

FIGURE 2. OPL Drift Histogram

Figure 3 shows the offset voltage drift after preconditioning and 1000 hours of THBT.
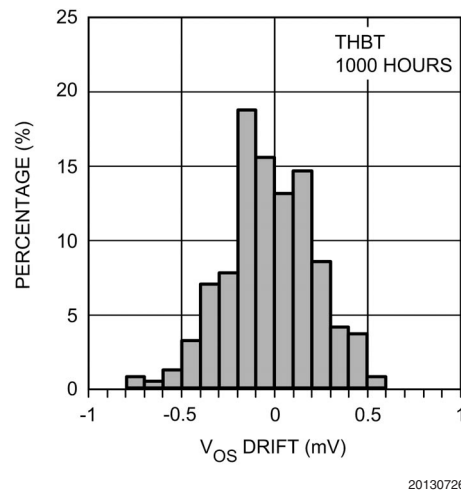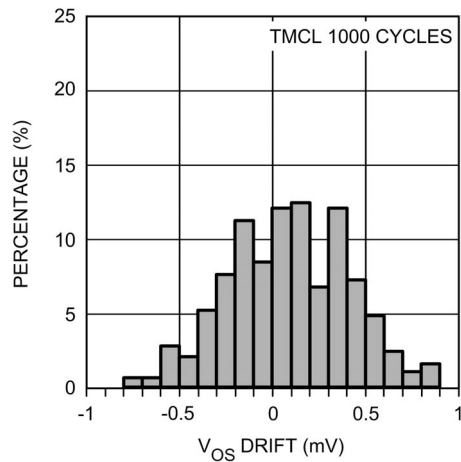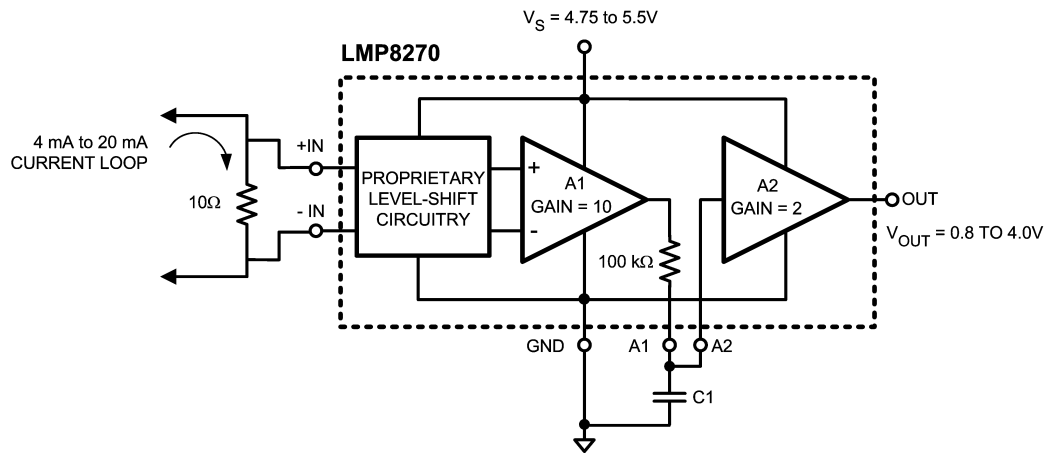

FIGURE 3. THBT Drift Histogram

Application Note (Continued)

Figure 4 shows the offset voltage drift after preconditioning and a total of 1000 TMCL cycles.

FIGURE 4. TMCL Drift Histogram

POWER SUPPLY DECOUPLING

In order to decouple the LMP8270 from AC noise on the power supply, it is recommended to use a 0.1 µF on the supply pin. It is best to use a 0.1 µF capacitor in parallel with a 10 µF capacitor. This will generate an AC path to ground for most frequency ranges and will greatly reduce the noise introduced by the power supply.

CURRENT LOOP RECEIVER

Many types of process control instrumentation use 4 to 20 mA transmitters to transmit the sensor's analog value to a central control room. The LMP8270 can be used as a current loop receiver as shown in *Figure 5*.

FIGURE 5. Current Loop Receiver

HIGH SIDE CURRENT SENSING

High side current measurement requires a differential amplifier with gain. Here the DC voltage source represents a common mode voltage with the +IN input at the supply voltage and the –IN input very close to the supply voltage. The LMP8270 can be used with a common mode voltage, V_{DC} in this case, of up to 36V.

The LMP8270 can be used for high side current sensing. The large common mode voltage range of this device allows it to sense signals outside of its supply voltage range. Also, the LMP8270 has very high CMRR, which enables it to sense very small signals in the presence of larger common mode signals. The system in *Figure 6* couples these two characteristics of the LMP8270 in an automotive application. The signal through R_{S1} is detected and amplified by the LMP8270 in the presence of a common mode signal of up to 27V with the highest accuracy.
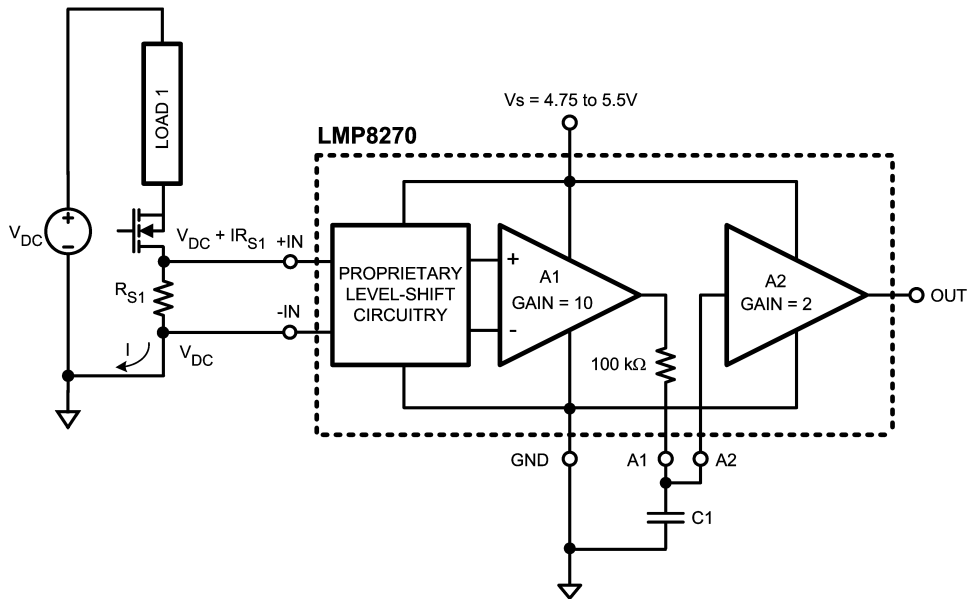
Application Note (Continued)
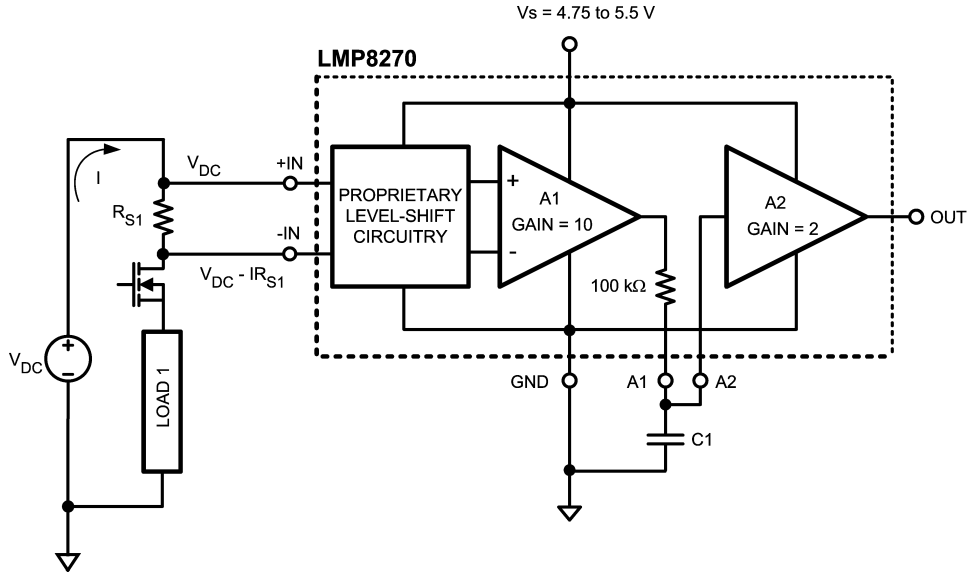
FIGURE 6. High Side Current Sensing

LOW SIDE CURRENT SENSING

Low side current measurements can cause a problem for operational amplifiers by exceeding the negative common mode voltage limit of the device. In *Figure 7*, the load current is returning to the power source through a common connection that has a parasitic resistance. The voltage drop across the parasitic resistances can cause the ground connection of the measurement circuits to be at a positive voltage with respect to the common side of the sense resistor. This will result in one or both of the inputs being negative with respect to the circuit's ground. The LMP8270 has a wide input common mode voltage range of −2V to 36V and will function in this condition.
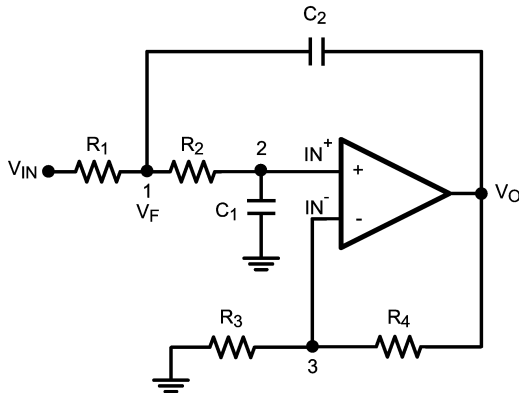

FIGURE 7. Low Side Current Sensing

Application Note (Continued)

SECOND ORDER LOW-PASS FILTER

The LMP8270 can be used to build a second order Sallen-Key low pass filter. The general filter is shown in *Figure 8*:

FIGURE 8. Second Order Low-Pass Filter

With the general transfer function:

$$\frac{V_O}{V_{IN}} = \frac{K}{M - KN}$$

(1)

Where:

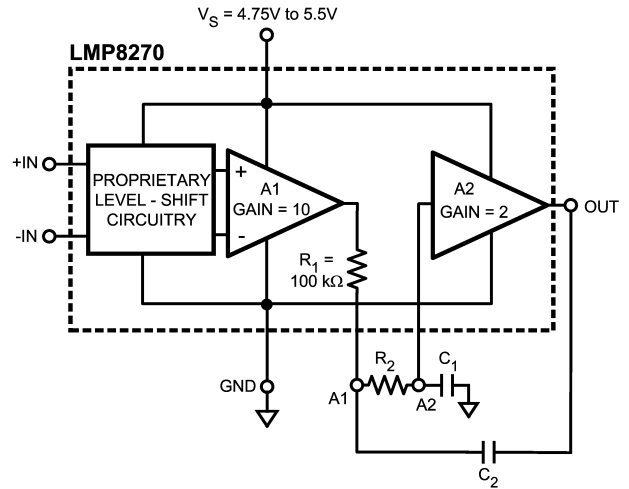$$M = s^2 C_1 C_2 R_1 R_2 + s(R_1 C_1 + R_1 C_2 + C_1 R_2) + 1$$
$$N = s C_2 R_1$$

and

$$\frac{1}{K} = \frac{1}{A_{VOL}} + \frac{R_3}{R_3 + R_4}$$

K represents the sum of DC closed loop gain and the non-ideality behavior of the operational amplifier. Assuming ideal behavior, the equation for K simply reduces to the DC gain, which is +2 for the LMP8270.

The LMP8270 can be used to realize this configuration as shown in figure *Figure 9*:

FIGURE 9. Low-Pass Filter With LMP8270

Using *Equation (1)* the filter parameters can be calculated as follows:

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$f_c = \frac{1}{2\pi \sqrt{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_1 + (1-K) R_1 C_2}$$

for the LMP8270, $R_1 = 100$ kΩ. Setting $R_1 = R_2$ and $C_1 = C_2$ results in a low-pass filter with Q = 1. Since the values of resistors are predetermined, the corner frequency of this implementation of the filter depends on the capacitor values.
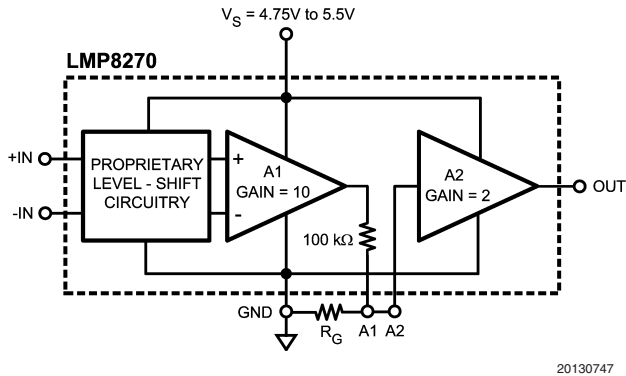
GAINS OTHER THAN 20

The LMP8270 has an internal gain of +20; however, this gain can be modified. The signal path between the two amplifiers is available as external pins.

Application Note (Continued)

GAINS LESS THAN 20

Figure 10 shows the configuration used to reduce the LMP8270 gain.
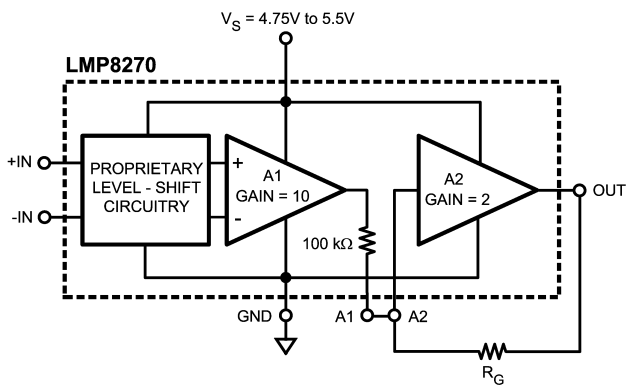

FIGURE 10. Gains Less than 20

Where:

$$GAIN\ (NEW) = \frac{20\ R_G}{R_G + 100\ k\Omega}$$

and

$$R_G = (100\ k\Omega)\ \frac{GAIN\ (NEW)}{20 - GAIN\ (NEW)}$$

GAINS GREATER THAN 20

A higher gain can be achieved by using positive feedback on the second stage amplifier, A2, of LMP8270. *Figure 11* shows the configuration:

FIGURE 11. Gains Greater than 20

The total gain is given by:

$$GAIN\ (NEW) = \frac{20\ R_G}{R_G - 100\ k\Omega}$$

(2)
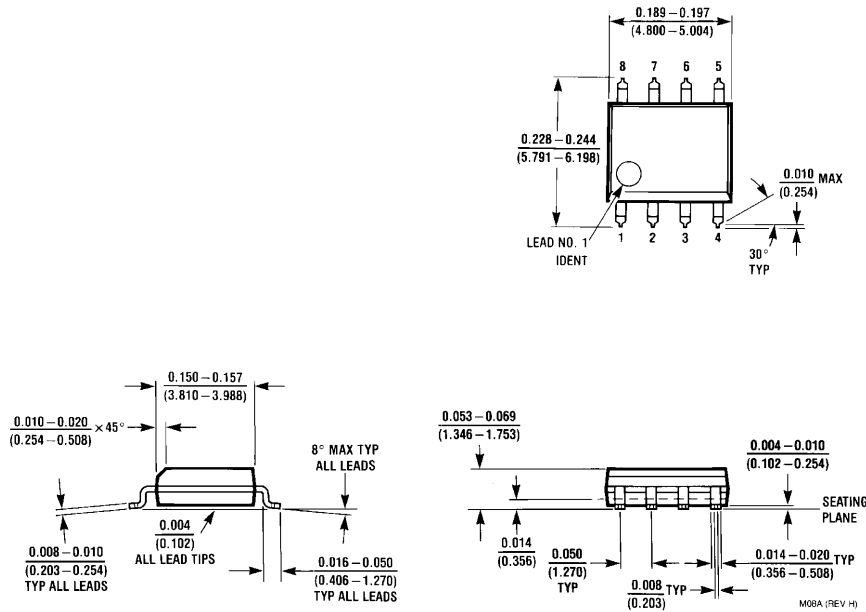
which can be rearranged to calculate R_G:

$$R_G = (100\ k\Omega)\ \frac{GAIN\ (NEW)}{GAIN\ (NEW) - 20}$$

The inverting gain of the second amplifier is set at 2, giving a total system gain of 20. The non-inverting gain which is achieved through positive feedback can be less than or equal to this gain without any issues. This implies a total system gain of 40 or less is easily achievable. Once the positive gain surpasses the negative gain, the system might oscillate.

As the value of gain resistor, R_G, approaches that of the internal 100 kΩ resistor, maintaining gain accuracy will become more challenging. This is because Gain(new) is inversely proportional to (R_G-100 kΩ), see *Equation (2)* . As $R_G \rightarrow$ 100 kΩ, the denominator of *Equation (2)* gets smaller. This smaller value will be comparable to the tolerance of the 100 kΩ resistor and R_G and hence the gain will be dominated by accuracy level of these resistors and the gain tolerance will be determined by the tolerance of the external resistor used for R_G and the 3% tolerance of the internal 100 kΩ resistor.

Physical Dimensions   inches (millimeters) unless otherwise noted

$\dfrac{0.189 - 0.197}{(4.800 - 5.004)}$

8 7 6 5

$\dfrac{0.228 - 0.244}{(5.791 - 6.198)}$

$\dfrac{0.010}{(0.254)}$ MAX

LEAD NO. 1
IDENT

1 2 3 4

30°
TYP

$\dfrac{0.150 - 0.157}{(3.810 - 3.988)}$

$\dfrac{0.010 - 0.020}{(0.254 - 0.508)} \times 45°$

8° MAX TYP
ALL LEADS

$\dfrac{0.008 - 0.010}{(0.203 - 0.254)}$
TYP ALL LEADS

$\dfrac{0.004}{(0.102)}$
ALL LEAD TIPS

$\dfrac{0.016 - 0.050}{(0.406 - 1.270)}$
TYP ALL LEADS

$\dfrac{0.053 - 0.069}{(1.346 - 1.753)}$

$\dfrac{0.004 - 0.010}{(0.102 - 0.254)}$

SEATING
PLANE

$\dfrac{0.014}{(0.356)}$

$\dfrac{0.050}{(1.270)}$
TYP

$\dfrac{0.008}{(0.203)}$ TYP

$\dfrac{0.014 - 0.020}{(0.356 - 0.508)}$ TYP

M08A (REV H)

8-Pin SOIC
NS Package Number M08A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor follows the provisions of the Product Stewardship Guide for Customers (CSP-9-111C2) and Banned Substances and Materials of Interest Specification (CSP-9-111S2) for regulatory environmental compliance. Details may be found at: www.national.com/quality/green.

Lead free products are RoHS compliant.