

LM4928 Boomer® Audio Power Amplifier Series

1.2 Watt Stereo Fully Differential Audio Amplifier with RF Suppression and Shutdown Low

General Description

The LM4928 is an stereo fully differential stereo audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication devices. It is capable of delivering 1.2 watts of continuous average power to a 8Ω load with less than 1% distortion (THD+N) from a 5V_{DC} power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4928 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4928 features a low-power consumption shutdown mode. To facilitate this, shutdown may be enabled by logic low. Additionally, the LM4928 features an internal thermal shutdown protection mechanism.

The LM4928 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Key Specifications

- Improved PSRR at 217Hz 90dB (typ)
- Output Power at 5.0V @ 1% THD+N (8Ω) 1.2W (typ)
- Output Power at 3.0V @ 1% THD+N (8Ω) 400mW (typ)
- Shutdown Current 0.1μA (typ)

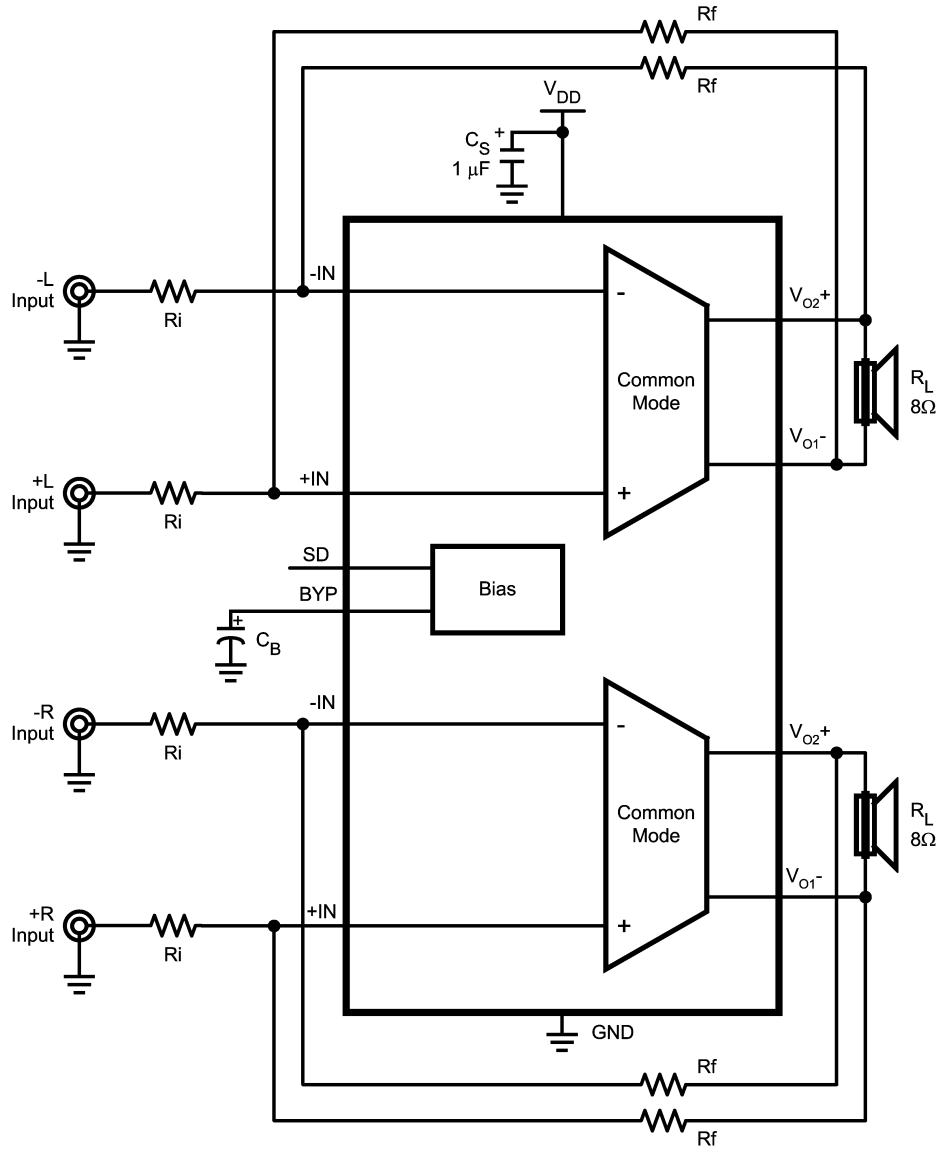
Features

- RF Suppression Circuitry
- Fully differential amplification
- Available in space-saving micro SMD and LLP packages
- Ultra low current shutdown mode
- Can drive capacitive loads up to 100pF
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.4 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required

Applications

- Mobile phones
- PDAs
- Portable electronic devices and accessories

Typical Application

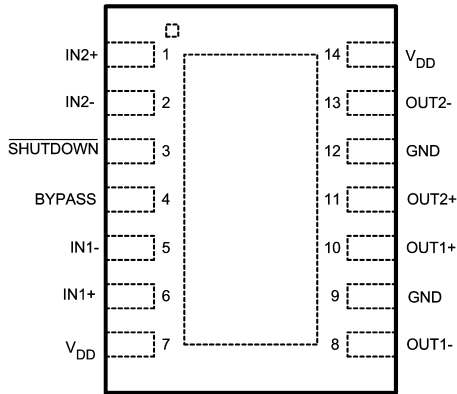


201600B7

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

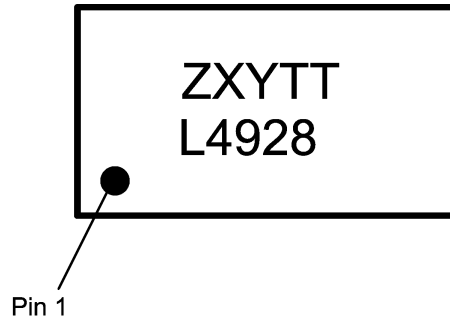
LLP Package



20160006

Top View
Order Number LM4928SD
See NS Package Number SDA14A

LLP Package Marking

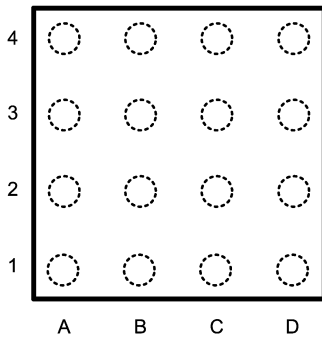


20160004

Top View
Z — Assembly Plant Code
XY — 2 Digit Date Code
TT — Die Traceability
L4928 — LM4928

micro SMD Package

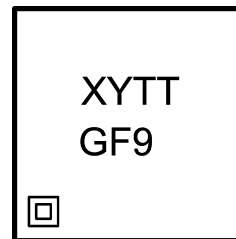
Top View



20160003

Top View
Order Number LM4928TL
See NS Package Number TLA16

micro SMD Package Marking



20160005

Top View
XY — 2 Digit Date Code
TT — Die Traceability
G — Boomer Family
F9 — LM4928T

LM4928TL Pin Descriptions

A1	IN1+
B1	IN1-
C1	IN2-
D1	IN2+
A2	V _{DD}
B2	BYPASS
C2	SHUTDOWN
D2	V _{DD}
A3	OUT1-
B3	OUT1+
C3	OUT2+
D3	OUT2-
A4	GND
B4	NC
C4	NC
D4	GND

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150°C
Thermal Resistance	

 θ_{JA} (SD) 50°C/W θ_{JA} (micro SMD) 74°C/W

Soldering Information

See AN-1187

Operating Ratings

Temperature Range

 $T_{MIN} \leq T_A \leq T_{MAX}$ $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$

Supply Voltage

 $2.4V \leq V_{DD} \leq 5.5V$ **Electrical Characteristics $V_{DD} = 5V$** (Notes 1, 2)

The following specifications apply for $V_{DD} = 5V$, $A_V = 1$, and 8Ω load unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4928		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V$, no load $V_{IN} = 0V$, $R_L = 8\Omega$ (Both amplifiers)	4 4	7.5	mA (max)
I_{SD}	Shutdown Current	$V_{SHUTDOWN} = GND$ (Both amplifiers)	0.1	1.0	μA (max)
P_o	Output Power	THD = 1% (max); $f = 1\text{ kHz}$ LM4928SD, $R_L = 4\Omega$ (Note 9) $R_L = 8\Omega$	1.8 1.2	1.0	W
		THD = 10% (max); $f = 1\text{ kHz}$ LM4928SD, $R_L = 4\Omega$ (Note 9) $R_L = 8\Omega$	2.2 1.5		W
THD+N	Total Harmonic Distortion + Noise	$P_o = 1\text{ Wrms}$; $f = 1\text{ kHz}$	0.04		%
PSRR	Power Supply Rejection Ratio	$V_{ripple} = 200\text{ mV sine p-p}$			
		$f = 217\text{ Hz}$ (Note 8)	90		dB
		$f = 1\text{ kHz}$ (Note 8)	90		
CMRR	Common-Mode Rejection Ratio	$f = 217\text{ Hz}$, $V_{CM} = 200\text{ mV}_{pp}$	70	50	dB (min)
V_{OS}	Output Offset	$V_{IN} = 0V$	4	18	mV (max)
V_{SDIH}	Shutdown Voltage Input High			1.4	V
V_{SDIL}	Shutdown Voltage Input Low			0.4	V
SNR	Signal-to-Noise Ratio	$P_o = 1W$, $f = 1\text{ kHz}$	105		dB
T_{WU}	Wake-up time from Shutdown	$C_{bypass} = 1\mu\text{F}$	13		ms

Electrical Characteristics $V_{DD} = 3V$ (Notes 1, 2)

The following specifications apply for $V_{DD} = 3V$, $A_V = 1$, and 8Ω load unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4928		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
I_{DD}	Quiescent Power Supply Current	$V_{IN} = 0V$, no load $V_{IN} = 0V$, $R_L = 8\Omega$ (Both amplifiers)	3.5 3.5		mA
I_{SD}	Shutdown Current	$V_{SHUTDOWN} = GND$ (Both amplifiers)	0.1	1	μA (max)

Electrical Characteristics $V_{DD} = 3V$ (Notes 1, 2)

The following specifications apply for $V_{DD} = 3V$, $A_V = 1$, and 8Ω load unless otherwise specified. Limits apply for $T_A = 25^\circ C$. (Continued)

Symbol	Parameter	Conditions	LM4928		Units (Limits)
			Typical	Limit	
			(Note 6)	(Note 7)	
P_o	Output Power	THD = 1% (max); $f = 1$ kHz $R_L = 4\Omega$ $R_L = 8\Omega$	0.55 0.40		W
		THD = 10% (max); $f = 1$ kHz $R_L = 4\Omega$ $R_L = 8\Omega$	0.68 0.50		W
THD+N	Total Harmonic Distortion + Noise	$P_o = 0.25W_{rms}$; $f = 1$ kHz	0.05		%
PSRR	Power Supply Rejection Ratio	$V_{ripple} = 200mV$ sine p-p			
		$f = 217Hz$ (Note 8)	90		dB
		$f = 1kHz$ (Note 8)	90		
CMRR	Common-Mode Rejection Ratio	$f = 217Hz$, $V_{CM} = 200mV_{pp}$	70	50	dB (min)
V_{OS}	Output Offset	$V_{IN} = 0V$	4	18	mV (max)
V_{SDIH}	Shutdown Voltage Input High			1.4	V
V_{SDIL}	Shutdown Voltage Input Low			0.4	V
SNR	Signal-to-Noise Ratio	$P_o = 0.4W$, $f = 1kHz$	105		dB
T_{WU}	Wake-up time from Shutdown	$C_{bypass} = 1\mu F$	9		ms

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM4928, see power derating curve for additional information.

Note 4: Human body model, 100pF discharged through a 1.5k Ω resistor.

Note 5: Machine Model, 220pF – 240pF discharged through all pins.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Inputs are AC terminated to GND.

Note 9: When driving 4 Ω loads from a 5V power supply, the LM4928SD must be mounted to a circuit board with the exposed-DAP area soldered down to at least 4in² plane of 1oz, copper.

Note 10: Data taken with BW = 80kHz and $A_V = 1$ except where specified.

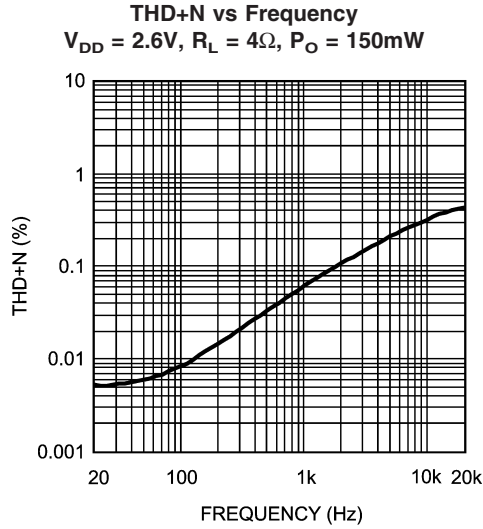
Note 11: Maximum Power Dissipation (P_{DMAX}) in the device occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 4 shown in the Application section. It may also be obtained from the Power Dissipation graphs.

External Components Description

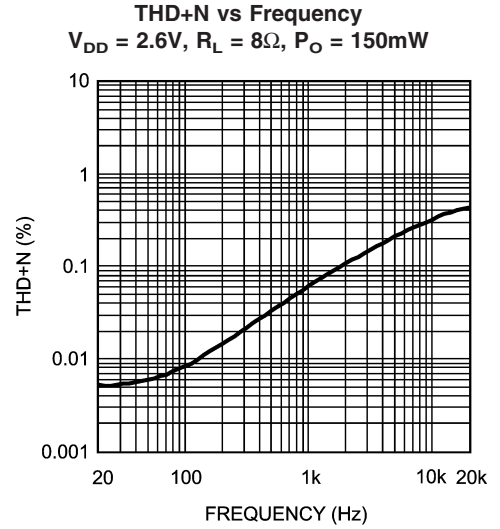
(Figure 1)

Components	Functional Description
1. C_S	Supply bypass capacitor which provides power supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of the supply bypass capacitor.
2. C_B	Bypass pin capacitor which provides half-supply filtering. Refer to the Power Supply Bypassing section for information concerning proper placement and selection of C_B .
3. R_i	Inverting input resistance which sets the closed-loop gain in conjunction with R_f .
4. R_f	External feedback resistance which sets the closed-loop gain in conjunction with R_i .

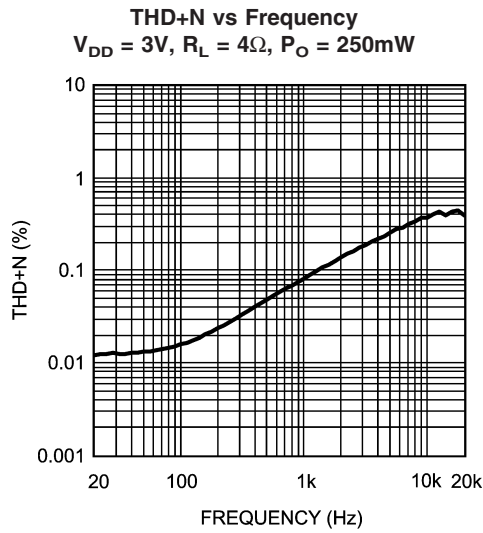
Typical Performance Characteristics (Note 10)



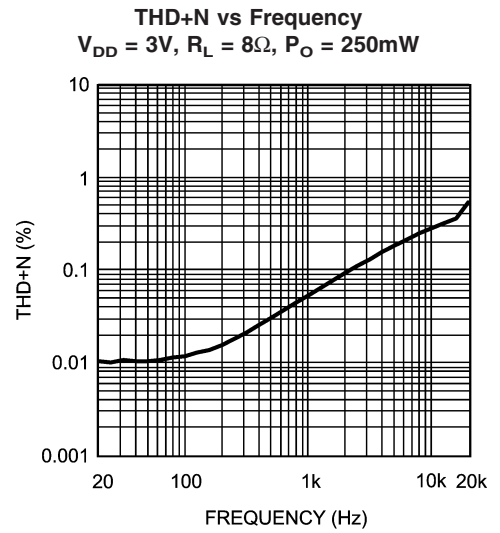
20160016



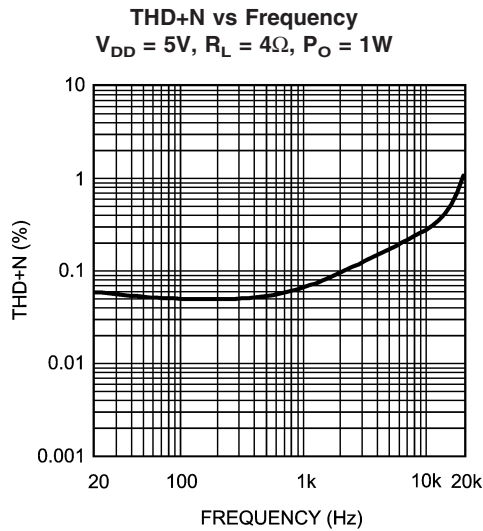
20160017



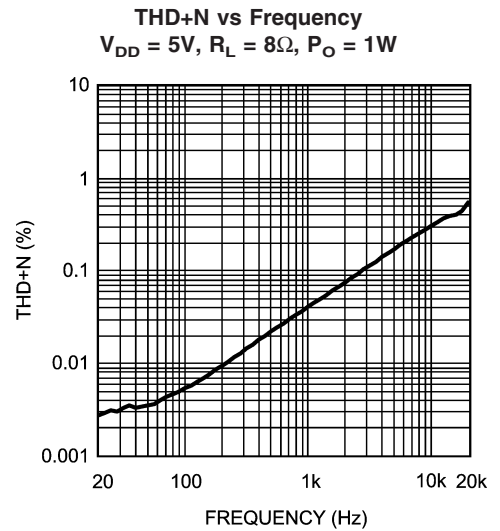
20160018



20160019

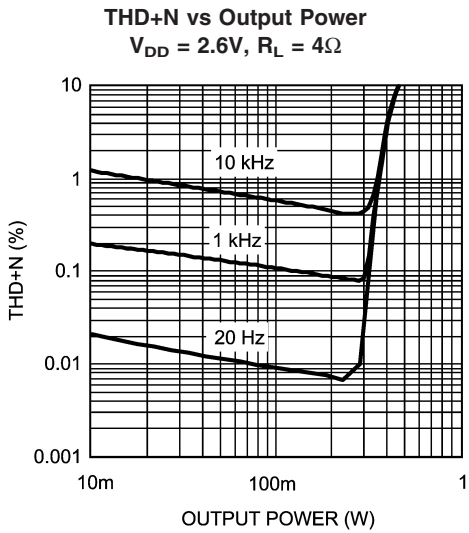


20160020

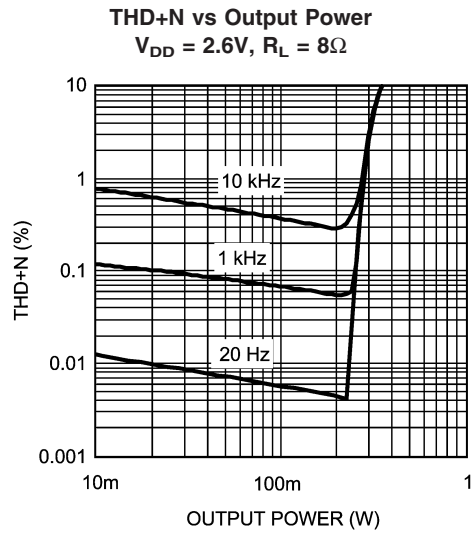


20160021

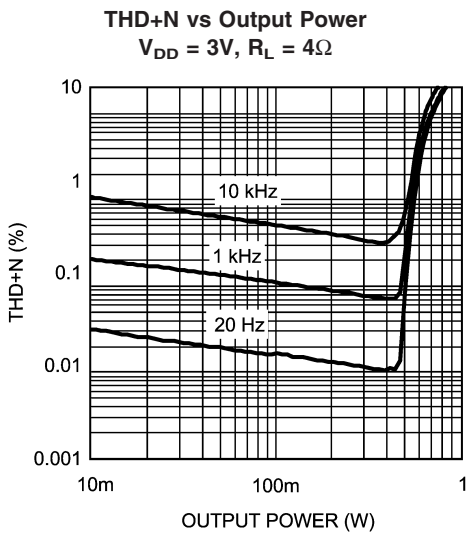
Typical Performance Characteristics (Note 10) (Continued)



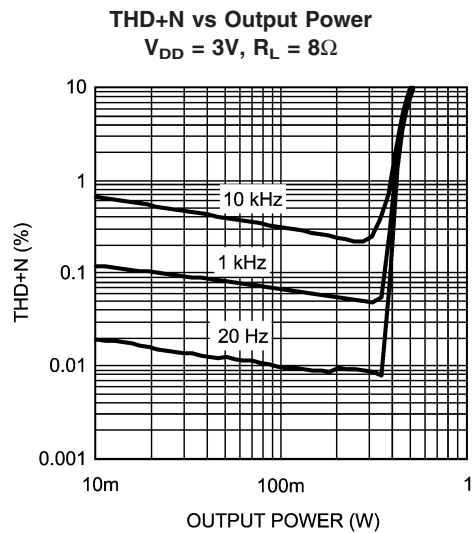
20160022



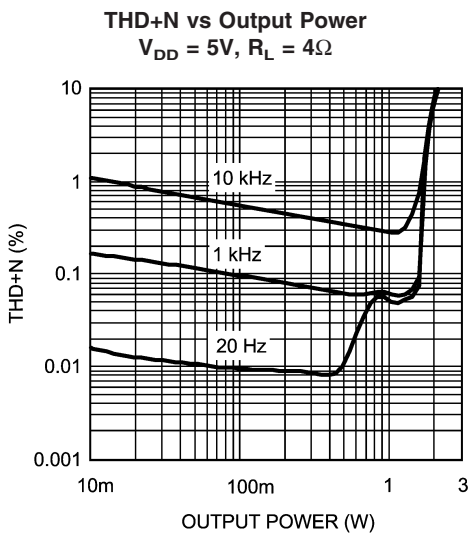
20160023



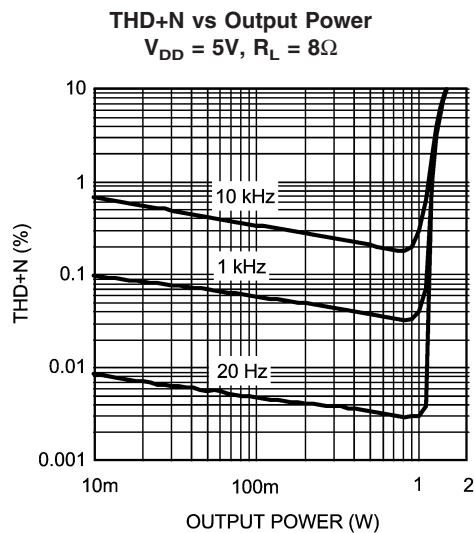
20160024



20160025



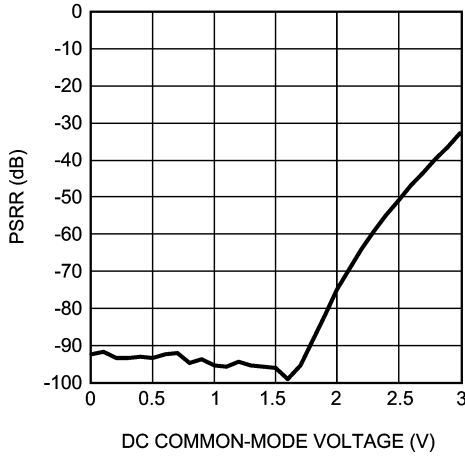
20160026



20160027

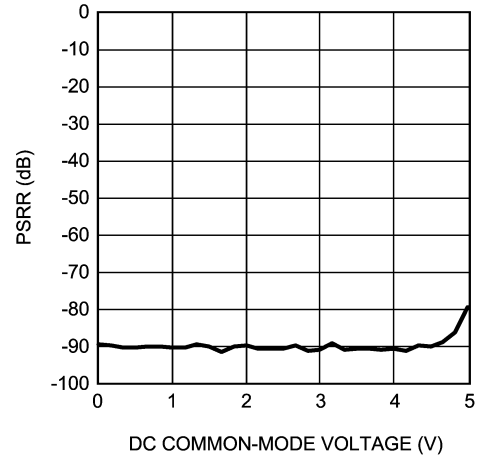
Typical Performance Characteristics (Note 10) (Continued)

PSRR vs Common Mode Voltage
 $V_{DD} = 3V, R_L = 8\Omega, f = 217Hz$



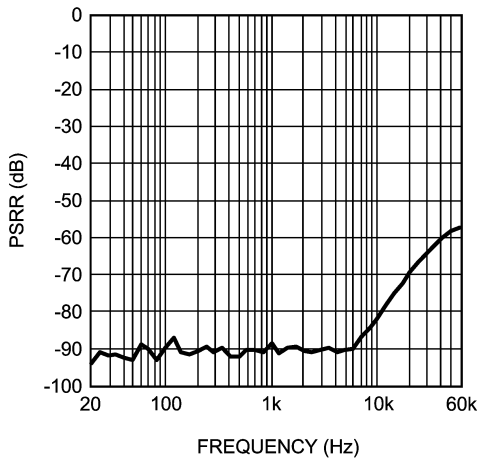
201600C8

PSRR vs Common Mode Voltage
 $V_{DD} = 5V, R_L = 8\Omega, f = 217Hz$



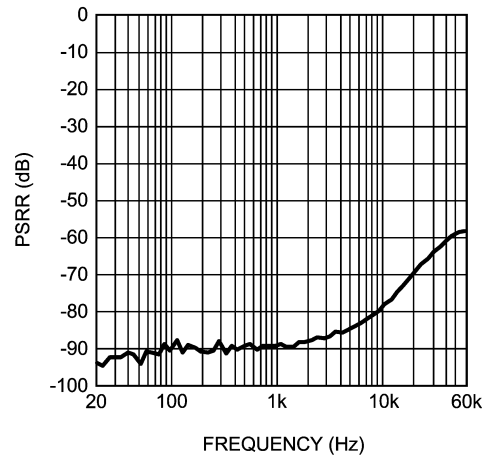
201600C9

PSRR vs Frequency
 $V_{DD} = 3V, R_L = 8\Omega$
 Input Terminated to GND, BW = 500kHz



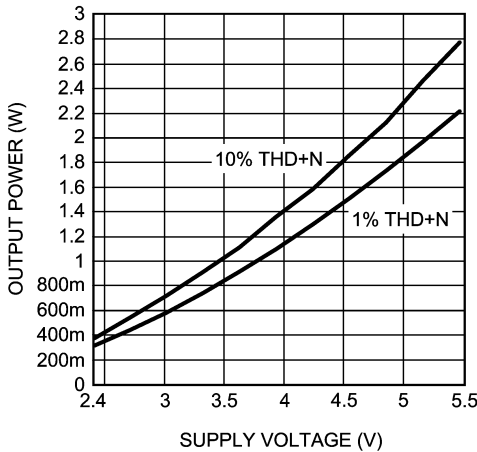
201600D0

PSRR vs Frequency
 $V_{DD} = 5V, R_L = 8\Omega$
 Input Terminated to GND, BW = 500kHz



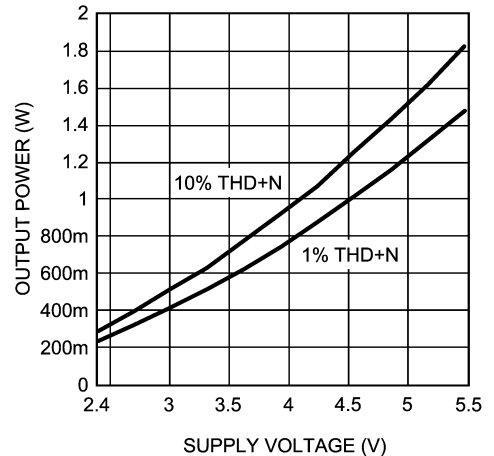
201600D1

Output Power vs Supply Voltage
 $R_L = 4\Omega$



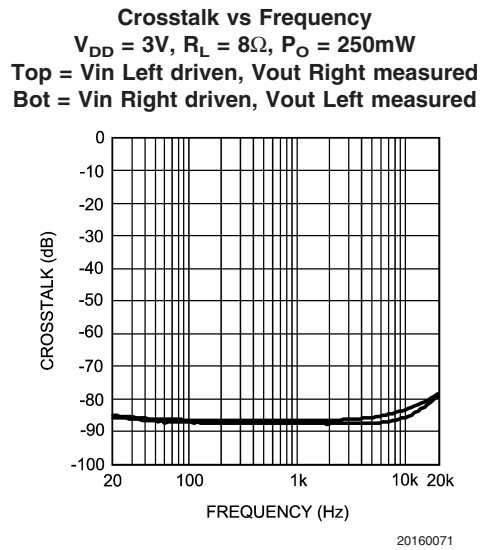
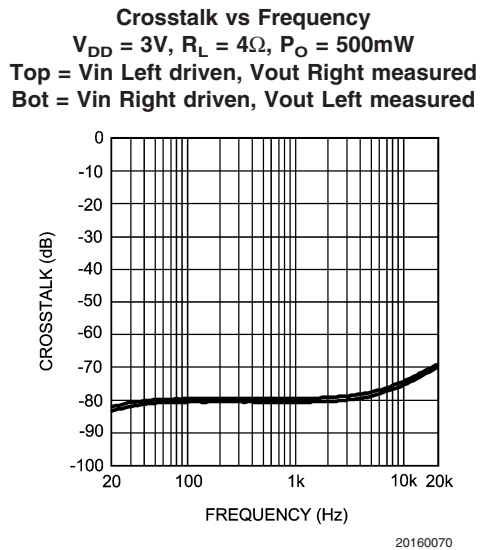
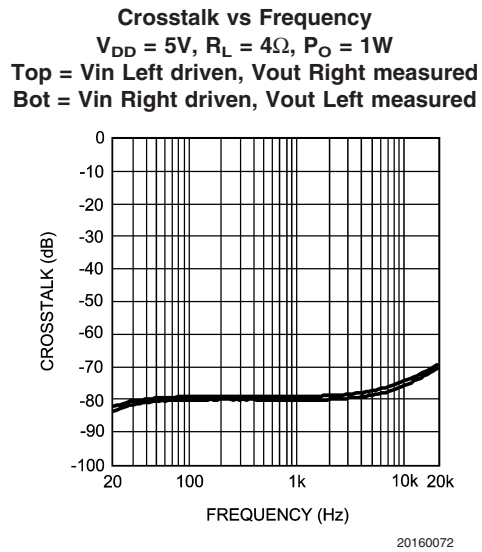
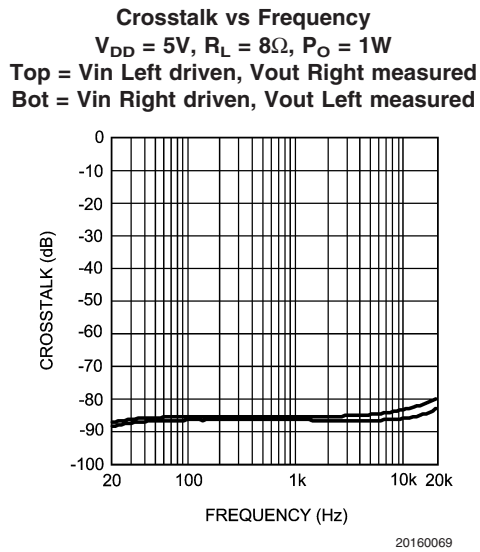
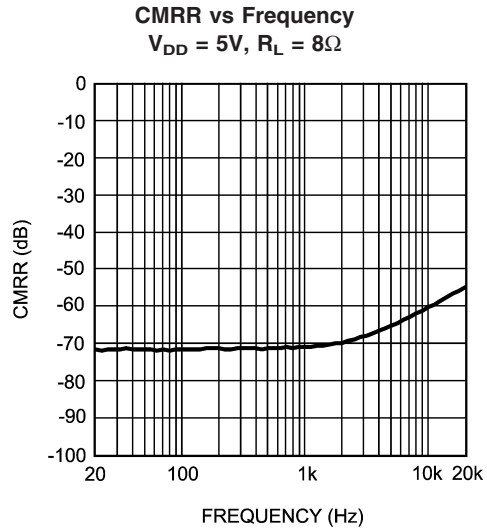
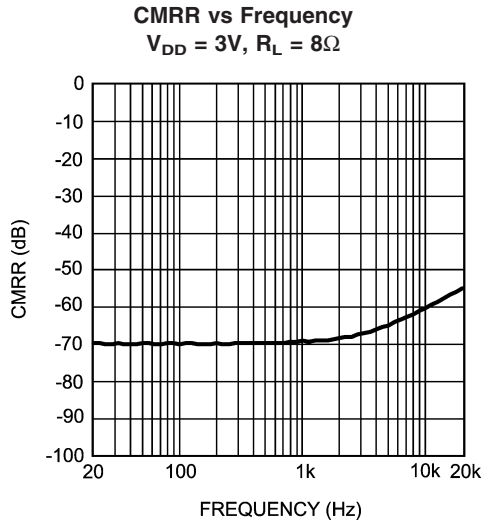
201600D2

Output Power vs Supply Voltage
 $R_L = 8\Omega$



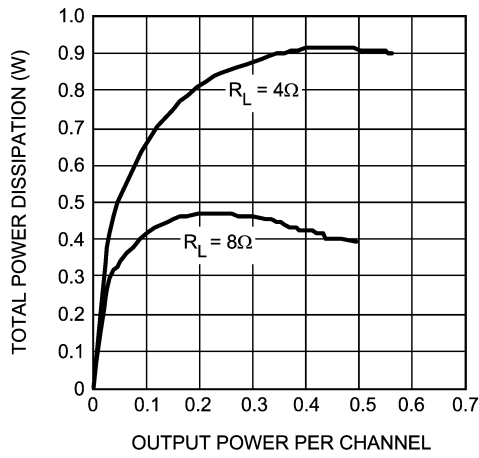
201600C5

Typical Performance Characteristics (Note 10) (Continued)

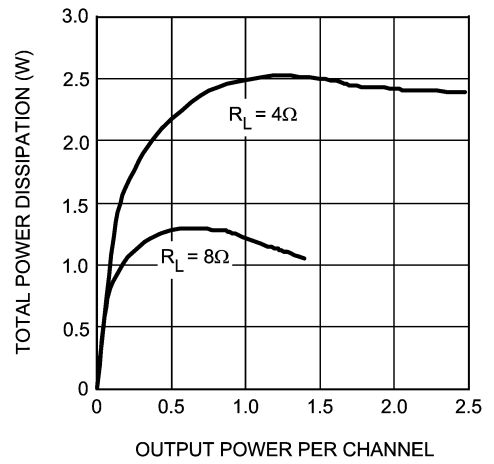


Typical Performance Characteristics (Note 10) (Continued)

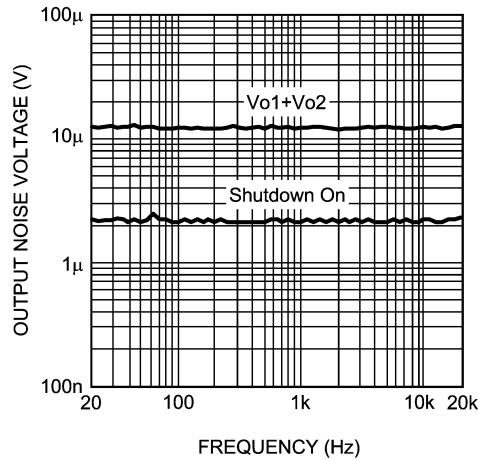
Power Dissipation vs Output Power
 $V_{DD} = 3V$



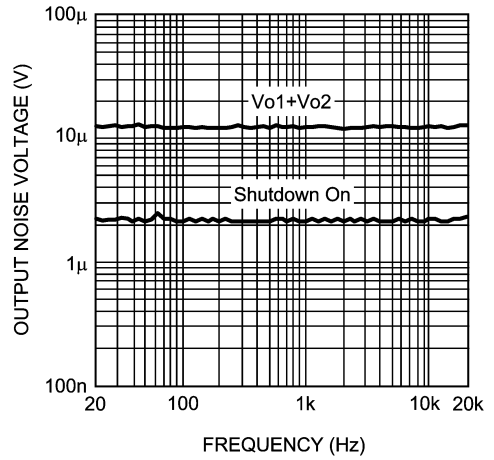
Power Dissipation vs Output Power
 $V_{DD} = 5V$



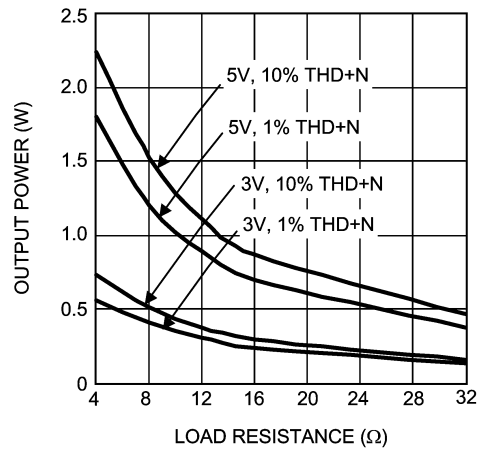
Noise Floor
 $V_{DD} = 3V$



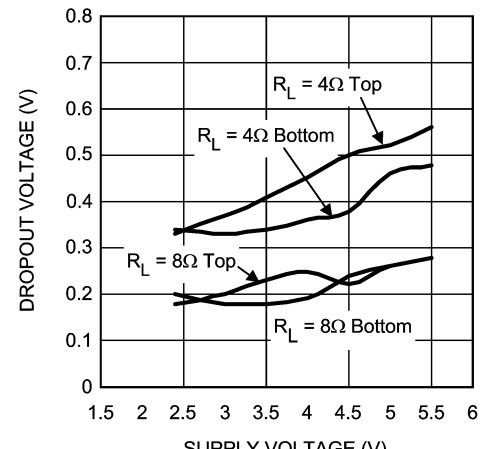
Noise Floor
 $V_{DD} = 5V$



Output Power vs Load Resistance



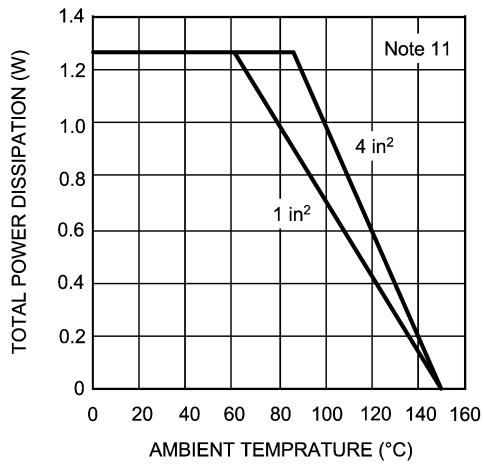
Clipping Voltage vs Supply Voltage



Typical Performance Characteristics (Note 10) (Continued)

Power Derating Curve (SD Package)

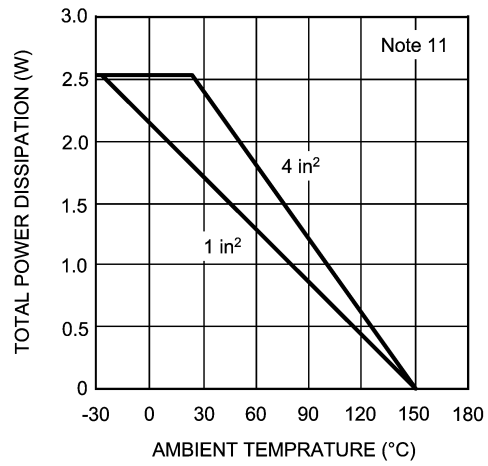
$f_{in} = 1\text{kHz}$, $R_L = 8\Omega$



20160068

Power Derating Curve (SD Package)

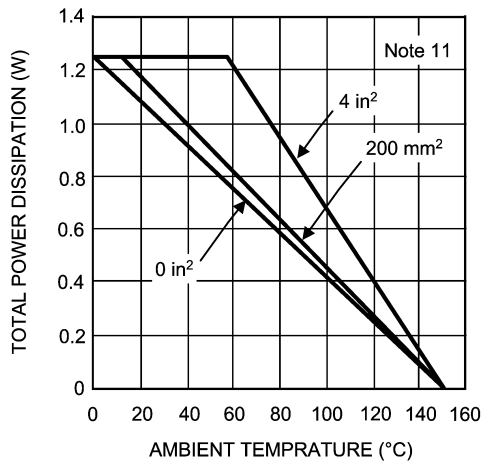
$f_{in} = 1\text{kHz}$, $R_L = 4\Omega$



20160067

Power Derating Curve (TL Package)

$f_{in} = 1\text{kHz}$, $R_L = 8\Omega$



20160066

Application Information

DIFFERENTIAL AMPLIFIER EXPLANATION

The LM4928 is a fully differential audio amplifier that features differential input and output stages. Internally this is accomplished by two circuits: a differential amplifier and a common mode feedback amplifier that adjusts the output voltages so that the average value remains $V_{DD} / 2$. When setting the differential gain, the amplifier can be considered to have "halves". Each half uses an input and feedback resistor (R_{i1} and R_{F1}) to set its respective closed-loop gain (see Figure 1). With $R_{i1} = R_{i2}$ and $R_{F1} = R_{F2}$, the gain is set at $-R_F / R_i$ for each half per channel. This results in a differential gain of

$$A_{VD} = -R_F/R_i \quad (1)$$

It is extremely important to match the input resistors to each other, as well as the feedback resistors to each other for best amplifier performance. See the **Proper Selection of External Components** section for more information. A differential amplifier works in a manner where the difference between the two input signals is amplified. In most applications, this would require input signals that are 180° out of phase with each other. The LM4928 can be used, however, as a single ended input amplifier while still retaining its fully differential benefits. In fact, completely unrelated signals may be placed on the input pins. The LM4928 simply amplifies the difference between them.

All of these applications provide what is known as a "bridged mode" output (bridge-tied-load, BTL). This results in output signals at V_{o1} and V_{o2} that are 180° out of phase with respect to each other. Bridged mode operation is different from the single-ended amplifier configuration that connects the load between the amplifier output and ground. A bridged amplifier design has distinct advantages over the single-ended configuration: it provides differential drive to the load, thus doubling maximum possible output swing for a specific supply voltage. Four times the output power is possible compared with a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excess clipping, please refer to the **Audio Power Amplifier Design** section.

A bridged configuration, such as the one used in the LM4928, also creates a second advantage over single-ended amplifiers. Since the differential outputs, V_{o1} and V_{o2} , are biased at half-supply, no net DC voltage exists across the load. This assumes that the input resistor pair and the feedback resistor pair are properly matched (see **Proper Selection of External Components**). BTL configuration eliminates the output coupling capacitor required in single-supply, single-ended amplifier configurations. If an output coupling capacitor is not used in a single-ended output configuration, the half-supply bias across the load would result in both increased internal IC power dissipation as well as permanent loudspeaker damage. Further advantages of bridged mode operation specific to fully differential amplifiers like the LM4928 include increased power supply rejection ratio, common-mode noise reduction, and click and pop reduction.

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The LM4928's exposed-DAP (die attach paddle) package (LLP) provide a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. Failing to optimize thermal design may compromise the LM4928's high power performance and activate unwanted, though necessary, thermal shutdown protection. The LLP package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with at least 4 vias thermal via. The via diameter should be 0.012in - 0.013in. Ensure efficient thermal conductivity by plating-through and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the LM4928's thermal shutdown protection. The LM4928's power de-rating curve in the **Typical Performance Characteristics** shows the maximum power dissipation versus temperature. Example PCB layouts are shown in the Demonstration Board Layout section. Further detailed and specific information concerning PCB layout, fabrication, and mounting an LLP package is available from National Semiconductor's package Engineering Group under application note AN1187.

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. Equation 2 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

Application Information (Continued)

$$P_{\text{DMAX}} = (V_{\text{DD}})^2 / (2\pi^2 R_L) \text{ Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation versus a single-ended amplifier operating at the same conditions.

$$P_{\text{DMAX}} = 4(V_{\text{DD}})^2 / (2\pi^2 R_L) \text{ Bridge Mode per channel} \quad (3)$$

$$P_{\text{DMAX}} = 8(V_{\text{DD}})^2 / (2\pi^2 R_L) \text{ Bridge Mode both channel} \quad (4)$$

Since the LM4928 has bridged outputs, the maximum internal power dissipation is 4 times that of a single-ended amplifier. Even with this substantial increase in power dissipation, the LM4928 does not require additional heatsinking under most operating conditions and output loading. From Equation 3, assuming a 5V power supply and an 8Ω load, the maximum power dissipation point is 625mW per channel. Then multiply by two or use equation 4 to get 1.25W total power dissipation for both channels. The maximum power dissipation point obtained from Equation 4 must not be greater than the power dissipation results from Equation 5:

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (5)$$

Depending on the ambient temperature, T_A , of the system surroundings, Equation 5 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 4 is greater than that of Equation 5, then either the supply voltage must be decreased, the load impedance increased, the ambient temperature reduced, or the θ_{JA} reduced with heatsinking. In many cases, larger traces near the output, V_{DD} , and GND pins can be used to lower the θ_{JA} . The larger areas of copper provide a form of heatsinking allowing higher power dissipation. For the typical application of a 5V power supply, with an 8Ω load in the LLP package, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 85°C provided that device operation is around the maximum power dissipation point. Recall that internal power dissipation is a function of output power. If typical operation is not around the maximum power dissipation point, the LM4928 can operate at higher ambient temperatures. Refer to the **Typical Performance Characteristics** curves for power dissipation information.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection ratio (PSRR). The capacitor location on both the bypass and power supply pins should be as close to the device as possible. A larger half-supply bypass capacitor improves PSRR because it increases half-supply stability. Typical applications employ a 5V regulator with 10μF and 0.1μF bypass capacitors that increase supply stability. This, however, does not eliminate the need for bypassing the supply nodes of the LM4928. The LM4928 will operate without the bypass capacitor C_B , although the PSRR may decrease. A 1μF capacitor is recommended for C_B . This value maximizes PSRR performance. Lesser values may be used,

but PSRR decreases at frequencies below 1kHz. The issue of C_B selection is thus dependant upon desired PSRR and click and pop performance.

OPTIMIZING RF IMMUNITY

The internal circuitry of the LM4928 suppresses the amount of RF signal that is coupled into the chip. However, certain external factors, such as output trace length, output trace orientation, distance between the chip and the antenna, antenna strength, speaker type, and type of RF signal, may affect the RF immunity of the LM4928. In general, the RF immunity of the LM4928 is application specific. Nevertheless, optimal RF immunity can be achieved by using short output traces and increasing the distance between the LM4928 and the antenna.

SHUTDOWN FUNCTION

In order to reduce power consumption while not in use, the LM4928 contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. The device may then be placed into shutdown mode by toggling the Shutdown Select pin to logic low. The trigger point for shutdown is shown as a typical value in the Supply Current vs Shutdown Voltage graphs in the **Typical Performance Characteristics** section. It is best to switch between ground and supply for maximum performance. While the device may be disabled with shutdown voltages in between ground and supply, the idle current may be greater than the typical value of 0.1μA. In either case, the shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry, which provides a quick, smooth transition to shutdown. Another solution is to use a single-throw switch in conjunction with an external pull-up resistor. This scheme guarantees that the shutdown pin will not float, thus preventing unwanted state changes.

PROPER SELECTION OF EXTERNAL COMPONENTS

Proper selection of external components in applications using integrated power amplifiers is critical when optimizing device and system performance. Although the LM4928 is tolerant to a variety of external component combinations, consideration of component values must be made when maximizing overall system quality.

The LM4928 is unity-gain stable, giving the designer maximum system flexibility. The LM4928 should be used in low closed-loop gain configurations to minimize THD+N values and maximize signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1V_{rms} are available from sources such as audio codecs. Please refer to the Audio Power Amplifier Design section for a more complete explanation of proper gain selection. When used in its typical application as a fully differential power amplifier the LM4928 does not require input coupling capacitors for input sources with DC common-mode voltages of less than V_{DD} . Exact allowable input common-mode voltage levels are actually a function of V_{DD} , R_i , and R_f and may be determined by Equation 6:

$$V_{\text{CMi}} < (V_{\text{DD}} - 1.2)(R_i + R_f) / R_f - V_{\text{DD}} / 2(R_i / R_f) \quad (6)$$

Application Information (Continued)

Special care must be taken to match the values of the input resistors (R_{i1} and R_{i2}) and (R_{f1} and R_{f2}) to each other. Because of the balanced nature of differential amplifiers, resistor matching differences can result in net DC currents across the load. This DC current can increase power consumption, internal IC power dissipation, reduce PSRR, CMRR, and possibly damaging the loudspeaker. The chart below demonstrates this problem by showing the effects of differing values between the input resistors while assuming that the feedback resistors are perfectly matched. The results below apply to the application circuit shown in Figure 1, and assumes that $V_{DD} = 5V$, $R_L = 8\Omega$, and the system has DC coupled inputs tied to ground.

Tolerance	R_{i1}	R_{i2}	$V_{O2} - V_{O1}$	I_{LOAD}
20%	0.8R	1.2R	-0.500V	62.5mA
10%	0.9R	1.1R	-0.250V	31.25mA
5%	0.95R	1.05R	-0.125V	15.63mA
1%	0.99R	1.01R	-0.025V	3.125mA
0%	R	R	0	0

Similar results would occur if the feedback resistors were not carefully matched. Adding input coupling resistors in between the signal source and the input resistors will eliminate this problem, however. To achieve best performance with minimum component count, it is highly recommended that both the feedback and input resistors matched to 1% tolerance or better for best performance.

AUDIO POWER AMPLIFIER DESIGN

Design a 1W/8Ω Audio Amplifier

Given:

Power Output	1Wrms
Load Impedance	8Ω
Maximum Input Level	1Vrms
Maximum Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. The supply rail can easily be found by extrapolating from the Output Power vs Supply Voltage graphs in the **Typical Performance Characteristics** section. A second way to determine the minimum supply rail is to calculate the required V_{OPEAK} using Equation 7 and add the dropout voltages. Using this method, the minimum supply voltage is ($V_{Opeak} + (V_{DO\ TOP} + V_{DO\ BOT})$), where $V_{DO\ BOT}$ and $V_{DO\ TOP}$ are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **Typical Performance Characteristics** section.

$$V_{Opeak} = \sqrt{(2R_L P_O)} \quad (7)$$

Using the Output Power vs Supply Voltage graph for an 8Ω load, the minimum supply rail just about 4.5V. Extra supply voltage creates headroom that allows the LM4928 to reproduce peaks in excess of 1W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the **Power Dissipation** section. Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 8.

$$A_{VD} \geq \sqrt{(P_O R_L)} / (V_{IN}) = V_{Orms} / V_{Inrms} \quad (8)$$

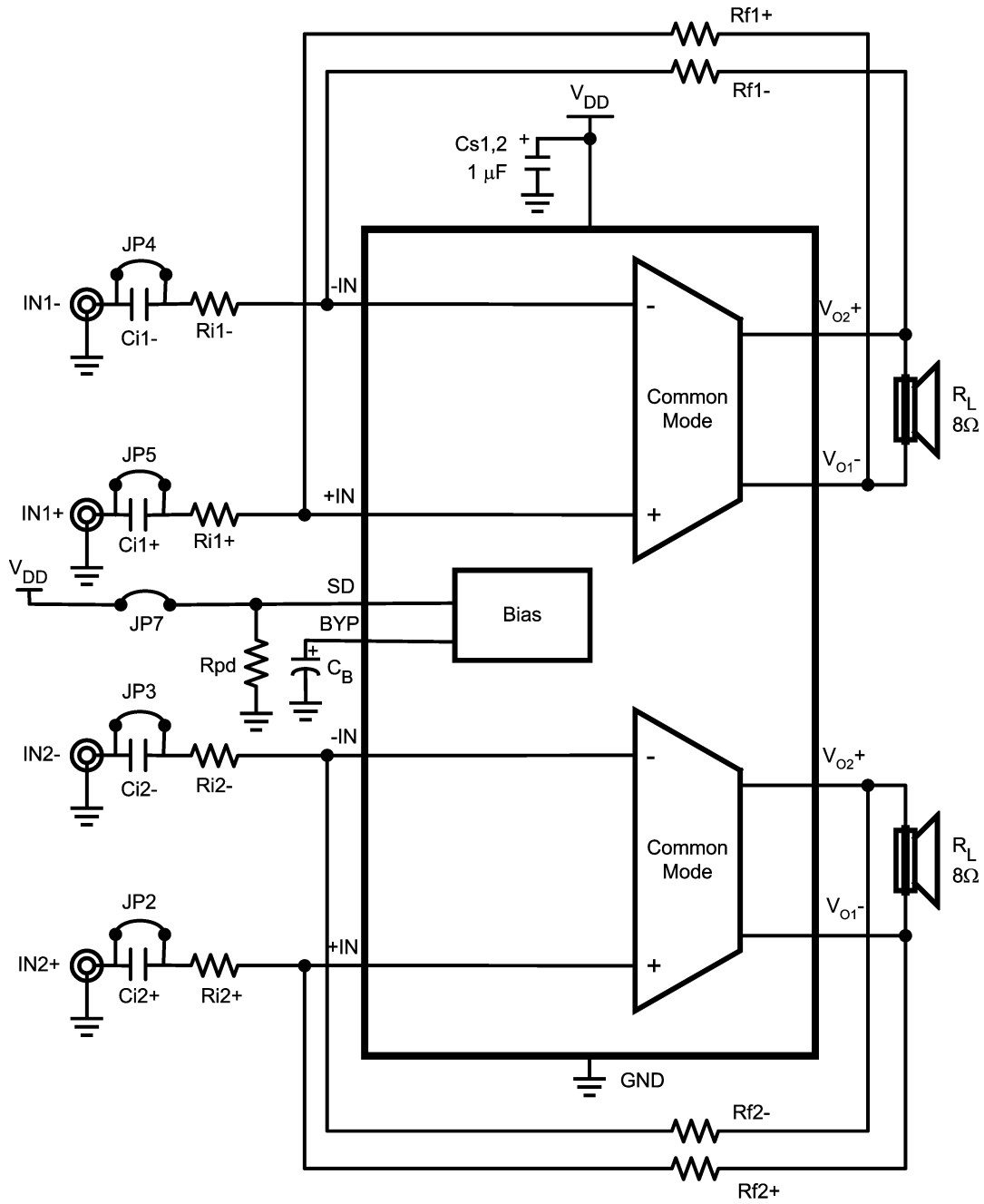
$$R_f / R_i = A_{VD}$$

From Equation 8, the minimum A_{VD} is 2.83. With $R_f = 40k\Omega$, a ratio of R_f to R_i of 2.83 gives $R_i = 14k\Omega$. The final design step is to address the bandwidth requirement which must be stated as a single -3dB frequency point. Five times away from a -3dB point is 0.17dB down from passband response which is better than the required ±0.25dB specified.

$$f_H = 20kHz * 5 = 100kHz$$

The high frequency pole is determined by the product of the desired frequency pole, f_H , and the differential gain, A_{VD} . With a $A_{VD} = 2.83$ and $f_H = 100kHz$, the resulting GBWP = 283kHz which is much smaller than the LM4928 GBWP of 10MHz. This figure displays that if a designer has a need to design an amplifier with a higher differential gain, the LM4928 can still be used without running into bandwidth limitations.

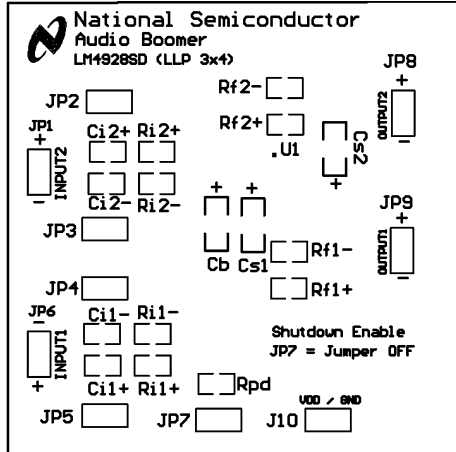
LM4928 Demo Board Schematic



20160073

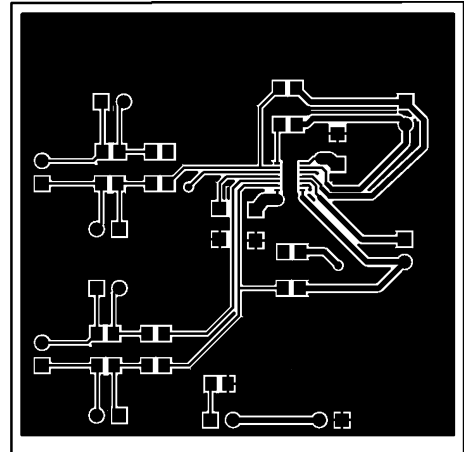
LM4928 LLP Demo Board Artwork

Top Silkscreen



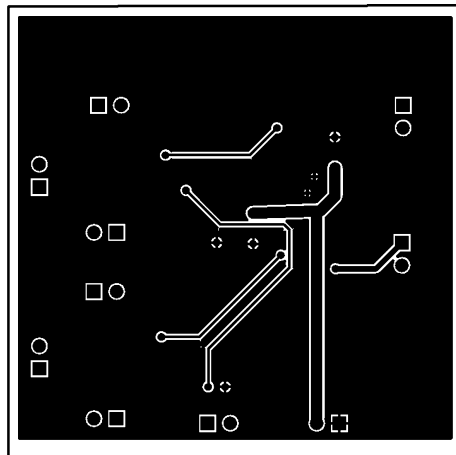
20160009

Top Layer



20160008

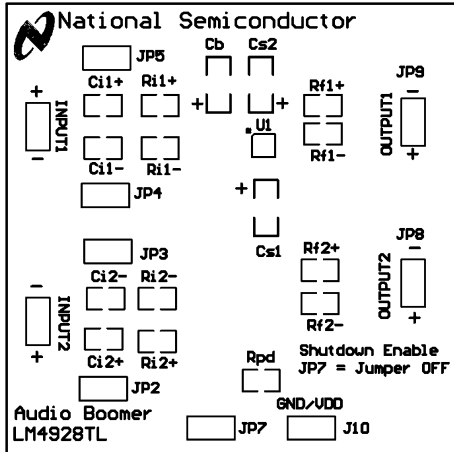
Bottom Layer and Ground Plane



20160007

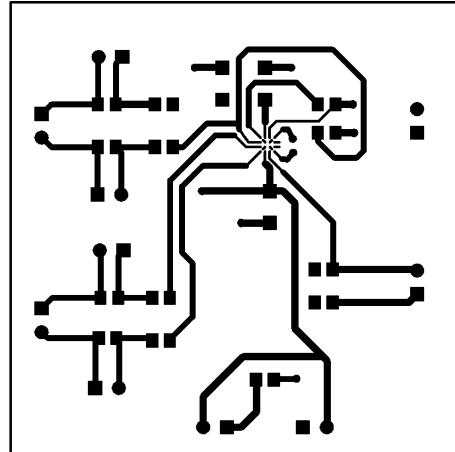
LM4928 microSMD Board Artwork

Top Silkscreen



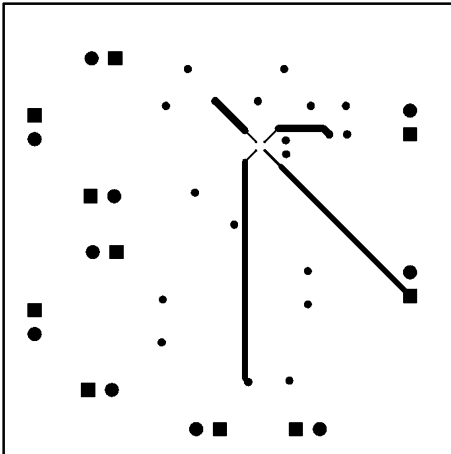
20160013

Top Layer



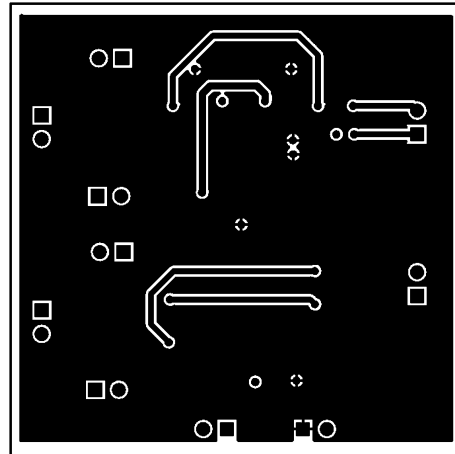
20160012

Middle Layer



20160010

Bottom Layer and Ground Plane

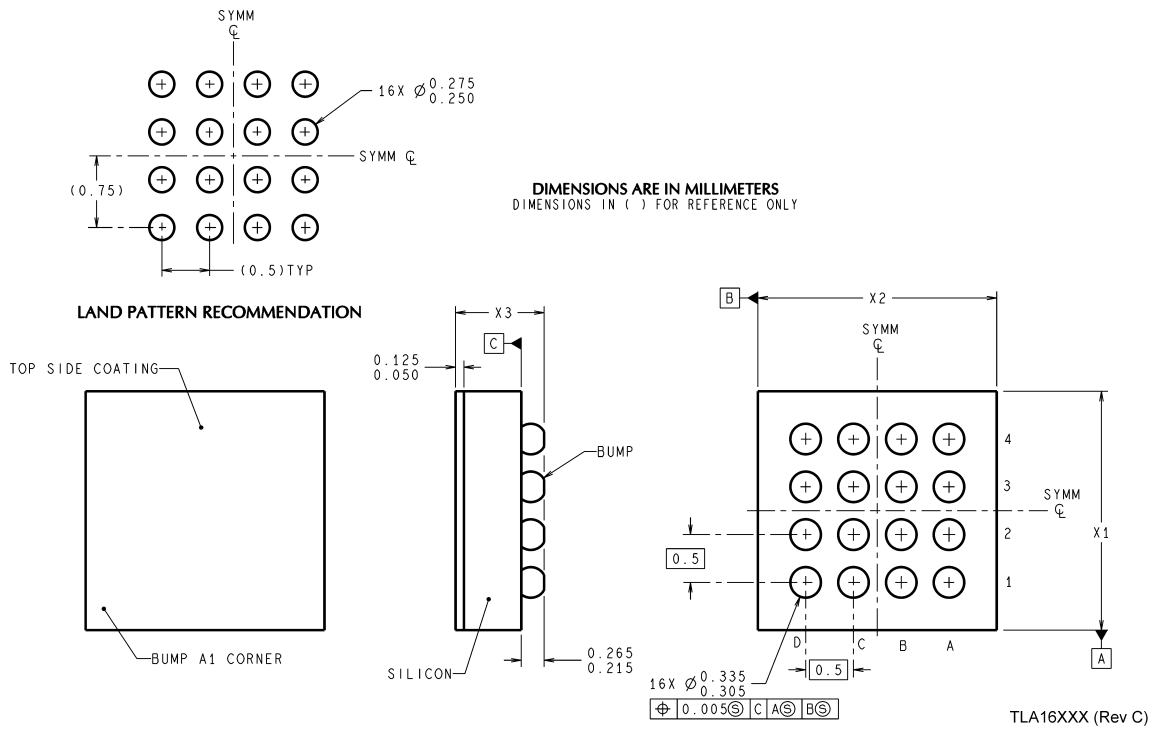
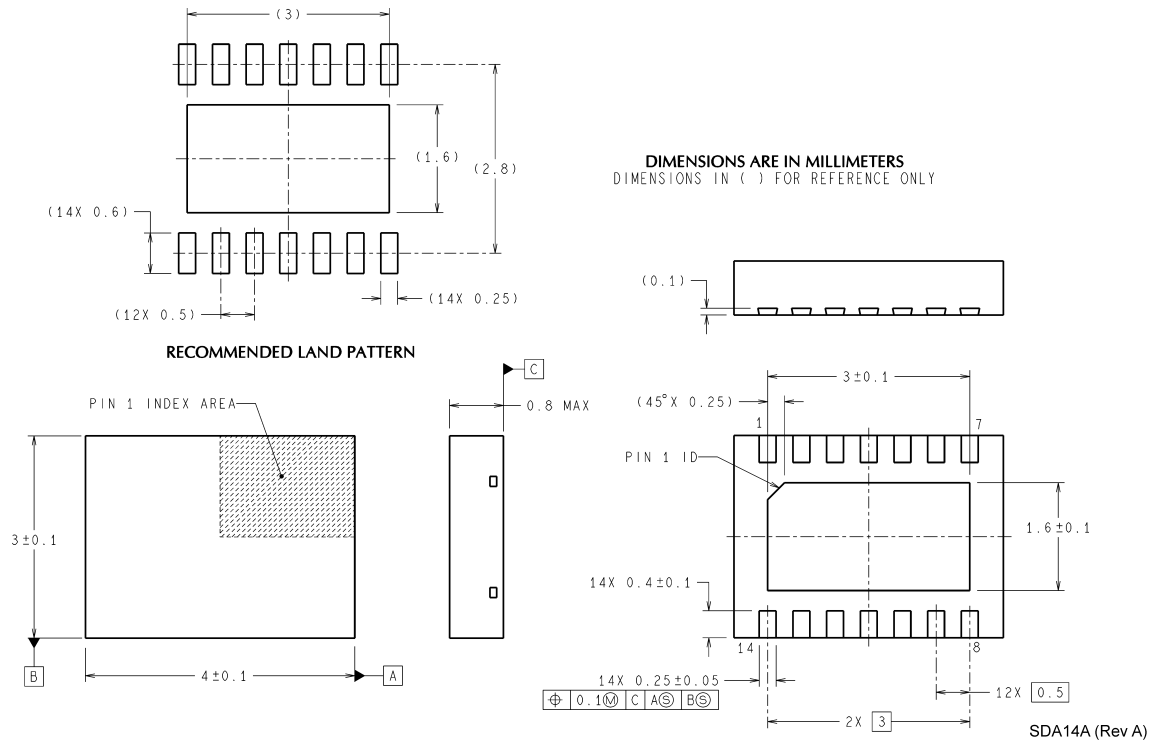


20160011

Revision History

Rev	Date	Description
1.0	7/13/05	Input first set of edits.
1.1	10/3/05	More edits input.
1.2	10/10/05	Input few text edits.
1.3	10/25/04	Added the Typ Perf section.
1.4	11/02/05	Added the X1, X2, and X3 values on the TLA1611A mktg outline.
1.5	11/15/05	Added 3 more curves (66, 67, and 68) and some texts edits.
1.6	11/16/05	Texts edits.
1.7	12/13/05	Added 4 more curves (69, 70, 71, and 72) and did some texts edits.
1.8	12/14/05	First WEB released (per Kashif).
1.9	12/16/05	Coded the LM4928TL (Future Product) for it will be released soon (early January, 2006) per Kashif. Re-released D/S to the WEB.
2.0	01/04/06	Released the TL package to the WEB.
2.1	01/09/06	Edited B7 and B8 (now 73), then re-released D/S to the WEB (per Kashif).
2.2	02/01/06	Text edits, then re-released D/S to the WEB.

Physical Dimensions inches (millimeters) unless otherwise noted



Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

For the most current product information visit us at www.national.com.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE

National Semiconductor manufactures products and uses packing materials that meet the provisions of the Customer Products Stewardship Specification (CSP-9-111C2) and the Banned Substances and Materials of Interest Specification (CSP-9-111S2) and contain no "Banned Substances" as defined in CSP-9-111S2.

Leadfree products are RoHS compliant.



National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europa.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560