



IRF9530, IRF9531 IRF9532, IRF9533

Avalanche Energy Rated
P-Channel Power MOSFETs

January 1994

Features

- -10A and -12A, -80V and -100V
- $r_{DS(ON)} = 0.3\Omega$ and 0.4Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

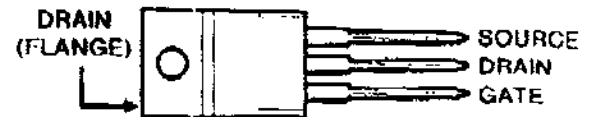
Description

The IRF9530, IRF9531, IRF9532 and IRF9533 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

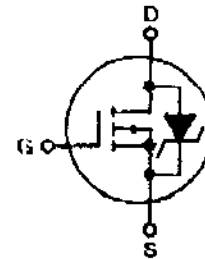
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$) Unless Otherwise Specified

	IRF9530	IRF9531	IRF9532	IRF9533	UNITS
Drain-Source Voltage (1)	V_{DS} -100	-80	-100	-80	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} -100	-80	-100	-80	V
Continuous Drain Current					
$T_C = 25^\circ\text{C}$	I_D -12	-12	-10	-10	A
$T_C = 100^\circ\text{C}$	I_D -7.5	-7.5	-6.5	-6.5	A
Pulsed Drain Current (3)	I_{DM} -48	-48	-40	-40	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D 75	75	75	75	W
(See Figure 14)					
Linear Derating Factor	0.6	0.6	0.6	0.6	W/ $^\circ\text{C}$
(See Figure 14)					
Single Pulse Avalanche Energy Rating (4)	E_{AS} 500	500	500	500	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

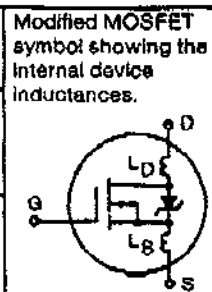
NOTES:

- $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
- Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
- $V_{DD} = 25\text{V}$, Start $T_J = +25^\circ\text{C}$, $L = 6.2\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 12\text{A}$
(See Figures 15 and 11)

Specifications IRF9530, IRF9531, IRF9532, IRF9533

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF9530, IRF9532 IRF9531, IRF9533	BV_{DSS}	$V_{GS} = 0V, I_D = -250\mu A$	-100 -80	-	-	V V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I_{GSS}	$V_{GS} = -20V$	-	-	-500	nA
Gate-Source Leakage Reverse	I_{GSS}	$V_{GS} = 20V$	-	-	500	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}, V_{GS} = 0V$	-	-	-250	μA
		$V_{DS} = \text{Max Rating} \times 0.8, V_{GS} = 0V, T_C = +125^\circ\text{C}$	-	-	-1000	μA
On-State Drain Current (Note 2) IRF9530, IRF9531 IRF9532, IRF9533	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, V_{GS} = -10V$	-12	-	-	A
			-10	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9530, IRF9531 IRF9532, IRF9533	$r_{DS(ON)}$	$V_{GS} = -10V, I_D = -6.5A$	-	0.25	0.3	Ω
			-	0.3	0.4	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)} \text{ Max}, I_D = 6.5A$	2.0	3.8	-	S(V)
Input Capacitance	C_{ISS}	$V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$	-	500	-	pF
Output Capacitance	C_{OSS}	See Figure 10	-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	100	-	pF
Turn-On Delay Time	$t_d(ON)$	$V_{DD} = 0.5 BV_{DSS}, I_D = -12A, R_G = 50\Omega$	-	30	60	ns
Rise Time	t_r	See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	70	140	ns
Turn-Off Delay Time	$t_d(OFF)$		-	70	140	ns
Fall Time	t_f		-	70	140	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	$V_{GS} = -10V, I_D = -12A, V_{DS} = 0.8 \text{ Max Rating}$. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	25	45	nC
Gate-Source Charge	Q_{gs}		-	13	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	12	-	nC
Internal Drain Inductance	L_D	Measured from the contact screw on tab to center of die.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	$R_{\theta JC}$		-	-	1.67	$^\circ\text{C/W}$
Case-to-Sink	$R_{\theta CS}$	Mounting surface flat, smooth and greased	-	1.0	-	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	Typical socket mount	-	-	80	$^\circ\text{C/W}$



Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.	-	-	-12	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	-48	A
Diode Forward Voltage (Note 2)	V_{SD}	$T_C = +25^\circ\text{C}, I_S = -12A, V_{GS} = 0V$	-	-	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = +150^\circ\text{C}, I_F = -12A, di_F/dt = 100A/\mu s$	-	300	-	ns
Reverse Recovered Charge	Q_{RR}	$T_J = +150^\circ\text{C}, I_F = -12A, di_F/dt = 100A/\mu s$	-	1.8	-	μC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$	-	-	-	-

NOTES: 1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$

2. Pulse Test: Pulse width $\leq 300\mu s$.
Duty Cycle $\leq 2\%$

3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)

4. $V_{DD} = 25V$. Start $T_J = +25^\circ\text{C}$. $L = 5.2\text{mH}$. $R_G = 25\Omega$. Peak $i_L = 12A$ (See Figures 15 and 18)

IRF9530, IRF9531, IRF9532, IRF9533

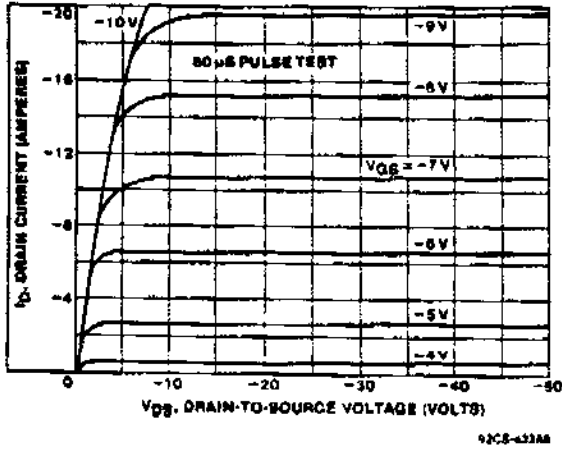


Fig. 1 - Typical Output Characteristics

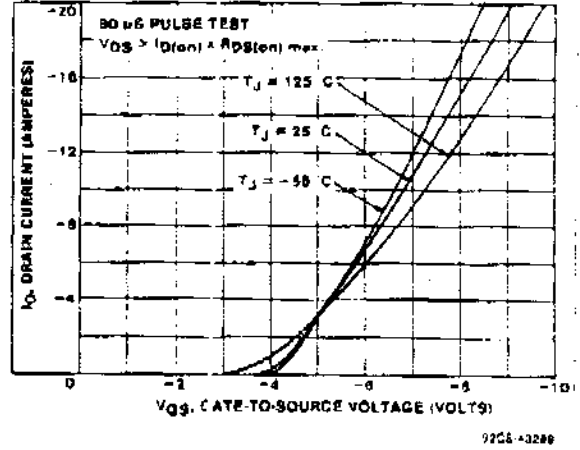


Fig. 2 - Typical Transfer Characteristics

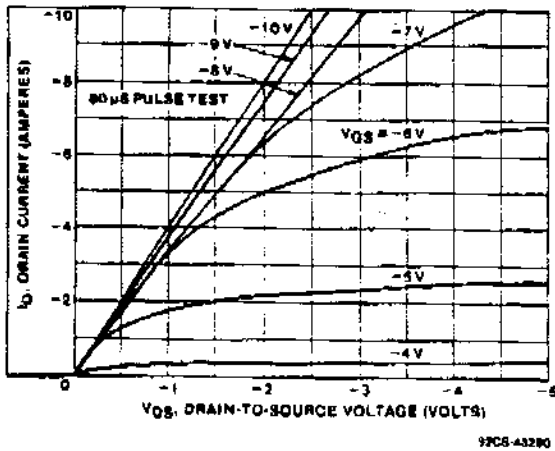


Fig. 3 - Typical saturation characteristic.

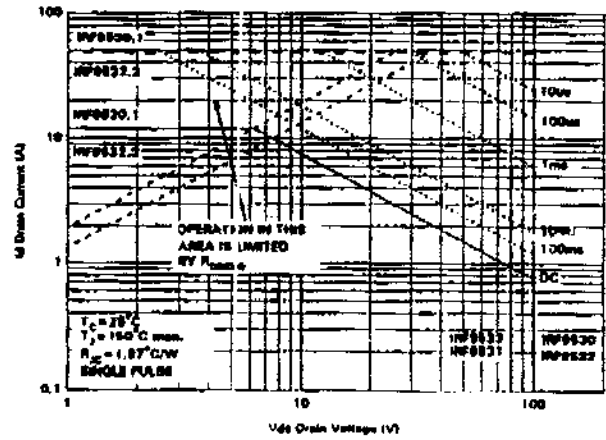


Fig. 4 - Maximum safe operating area.

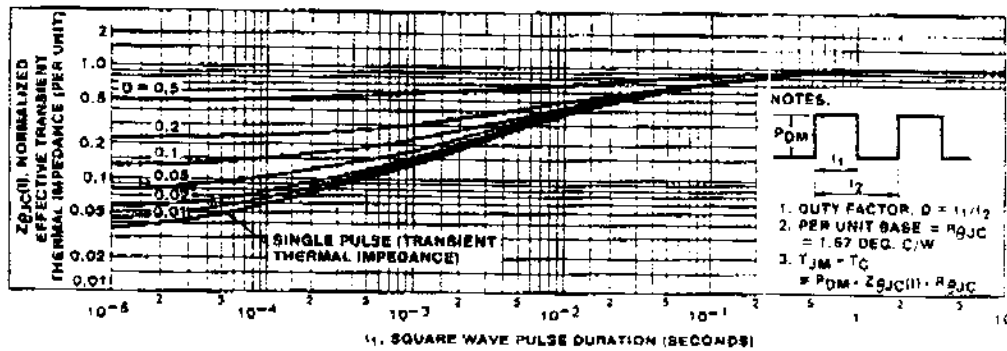


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRF9530, IRF9531, IRF9532, IRF9533

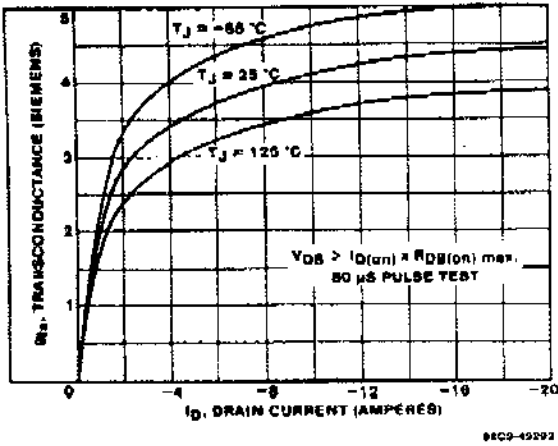


Fig. 6 - Typical transconductance vs. drain current.

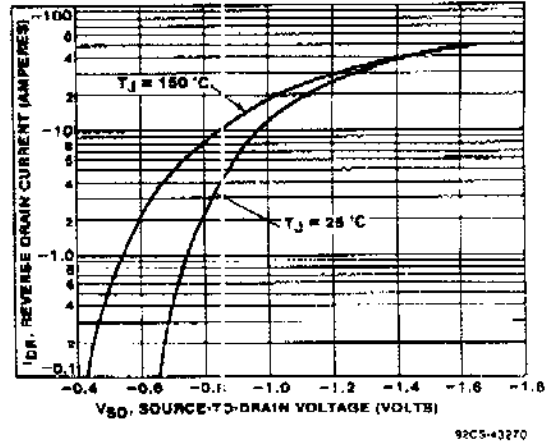


Fig. 7 - Typical source-drain diode forward voltage.

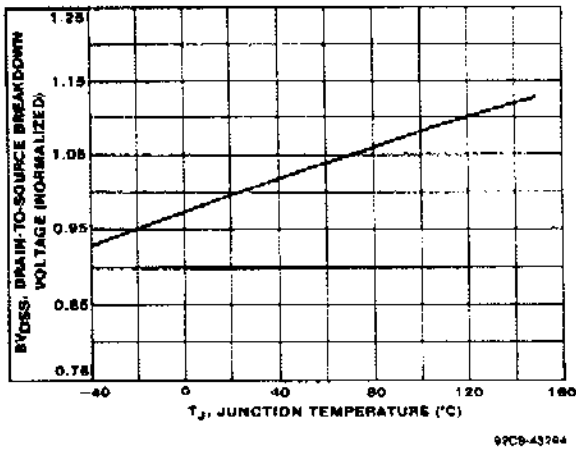


Fig. 8 - Breakdown voltage vs. temperature.

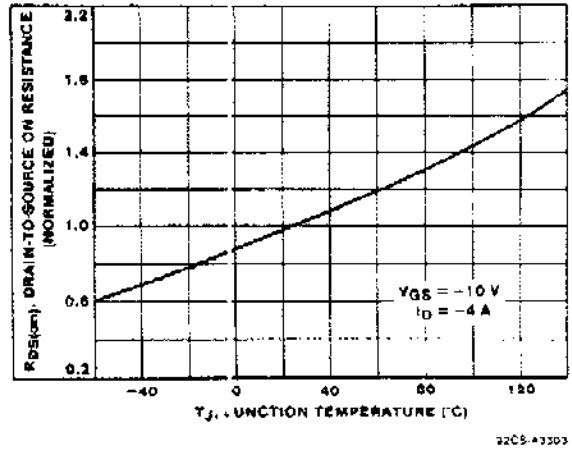


Fig. 9 - Normalized on-resistance vs. temperature.

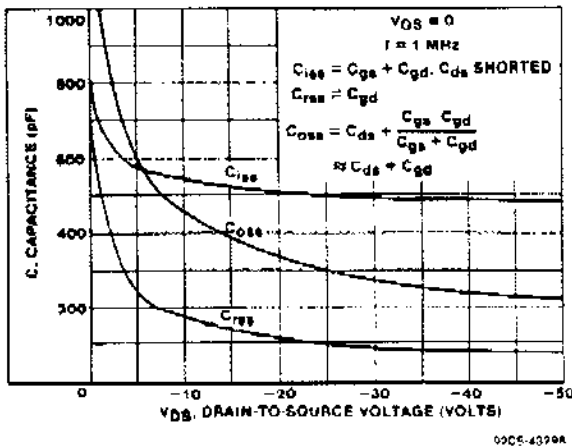


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

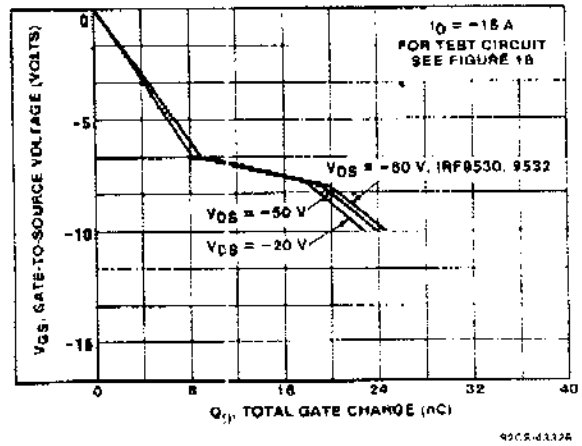
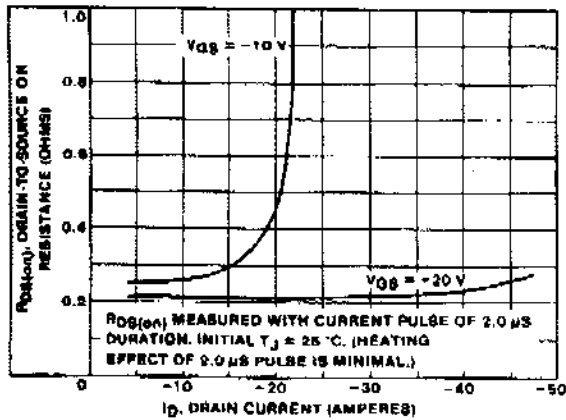


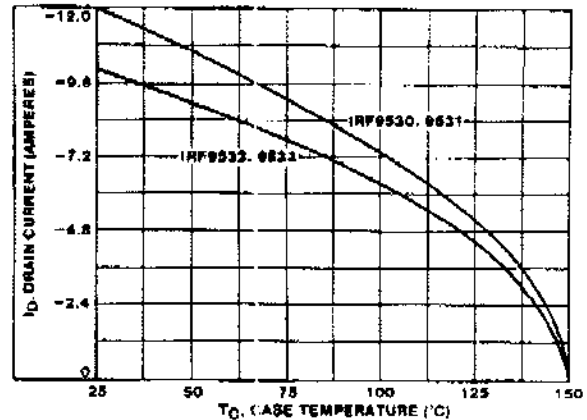
Fig. 11 - Typical gate charge vs. gate-to-source voltage.

IRF9530, IRF9531, IRF9532, IRF9533



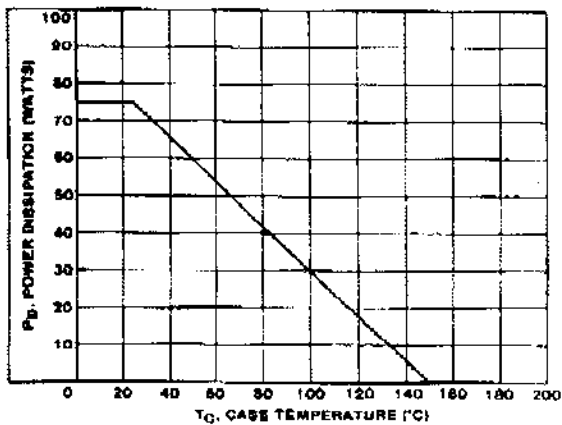
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Fig. 12 - Typical on-resistance vs. drain current.



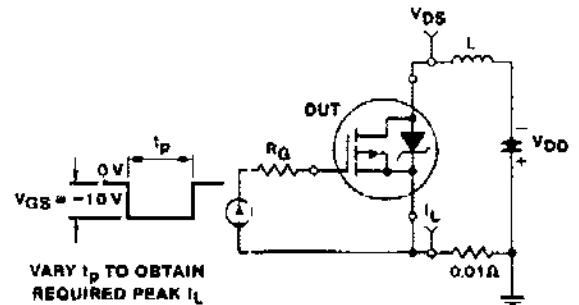
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Fig. 13 - Maximum drain current vs. case temperature.



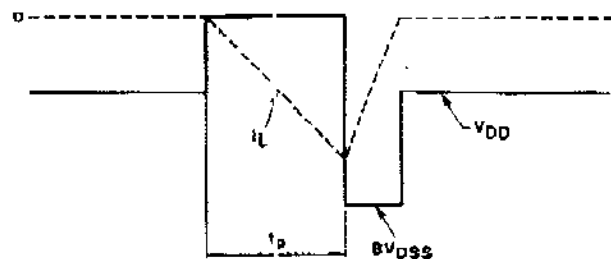
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Fig. 14 - Power vs. temperature derating curve.



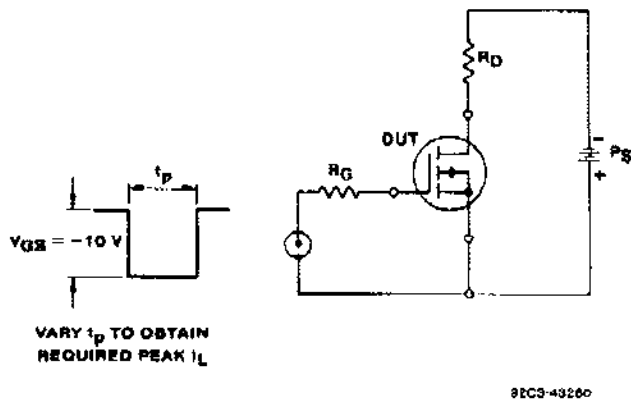
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Fig. 15 - Unclamped inductive test circuit.



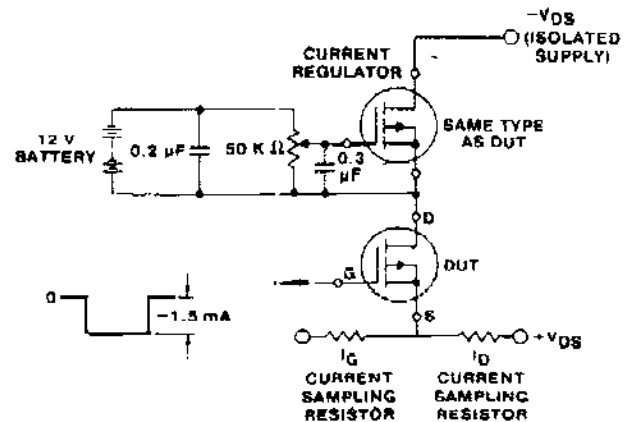
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Fig. 16 - Unclamped inductive waveforms.



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Fig. 17 - Switching time test circuit.



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Fig. 18 - Gate charge test circuit.