

FDP26N40 / FDPF26N40

N-Channel MOSFET

400V, 26A, 0.16Ω

Features

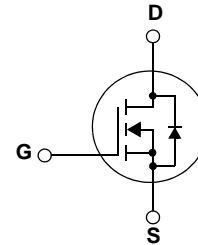
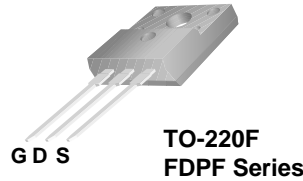
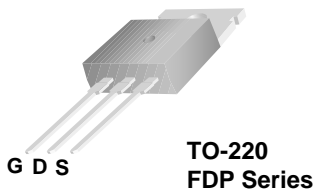
- $R_{DS(on)} = 0.13\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 13A$
- Low gate charge (Typ. 48nC)
- Low C_{RSS} (Typ. 30pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted*

Symbol	Parameter	FDP26N40	FDPF26N40	Units
V_{DSS}	Drain to Source Voltage	400		V
V_{GSS}	Gate to Source Voltage	±30		V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	26	26*
		-Continuous ($T_C = 100^\circ\text{C}$)	15.6	15.6*
I_{DM}	Drain Current	- Pulsed (Note 1)	104	104*
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1352		mJ
I_{AR}	Avalanche Current (Note 1)	26		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	26.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	265	40
		- Derate above 25°C	2.0	0.3
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP26N40	FDPF26N40	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case to Sink Typ.	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP26N40	FDP26N40	TO-220	-	-	50
FDPF26N40	FDPF26N40	TO-220F	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	400	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.5	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 400\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = 320\text{V}, T_C = 125^\circ\text{C}$	-	-	1 10	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 13\text{A}$	-	0.13	0.16	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 20\text{V}, I_D = 13\text{A}$ (Note 4)	-	25.5	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2400	3185	pF
C_{oss}	Output Capacitance		-	390	520	pF
C_{rss}	Reverse Transfer Capacitance		-	30	45	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 320\text{V}, I_D = 26\text{A}$ $V_{GS} = 10\text{V}$	-	48	60	nC
Q_{gs}	Gate to Source Gate Charge		-	15	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	20	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 200\text{V}, I_D = 26\text{A}$ $R_G = 25\Omega$	-	45	100	ns
t_r	Turn-On Rise Time		-	100	210	ns
$t_{d(off)}$	Turn-Off Delay Time		-	115	240	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	-	66	140

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	26	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	104	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 26\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 26\text{A}$	-	406	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	5.17	-	μC

Notes:

- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2: $L = 4\text{mH}, I_{AS} = 26\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
- 3: $I_{SD} \leq 26\text{A}, dI/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
- 4: Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
- 5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

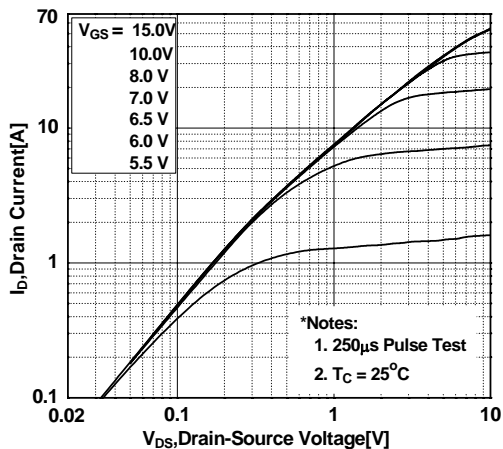


Figure 2. Transfer Characteristics

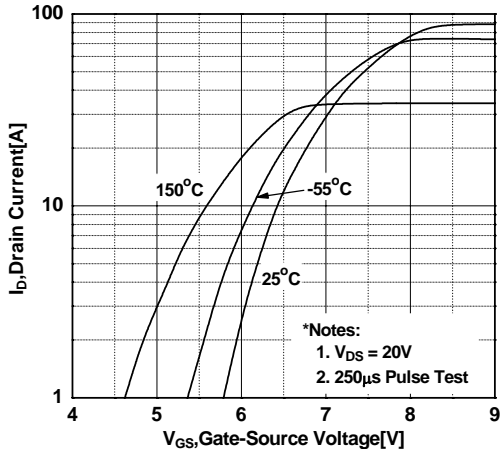


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

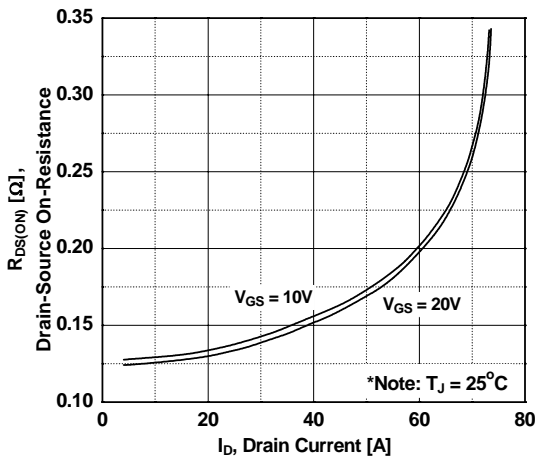


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

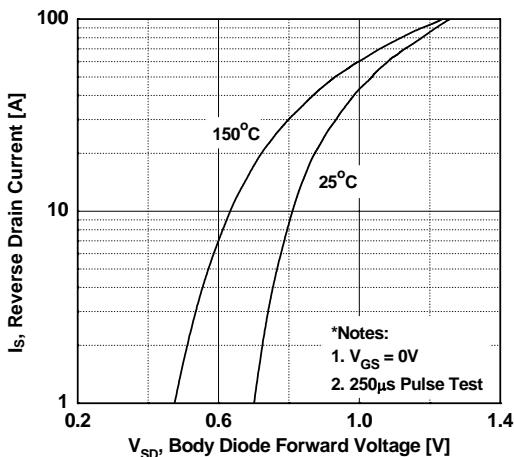


Figure 5. Capacitance Characteristics

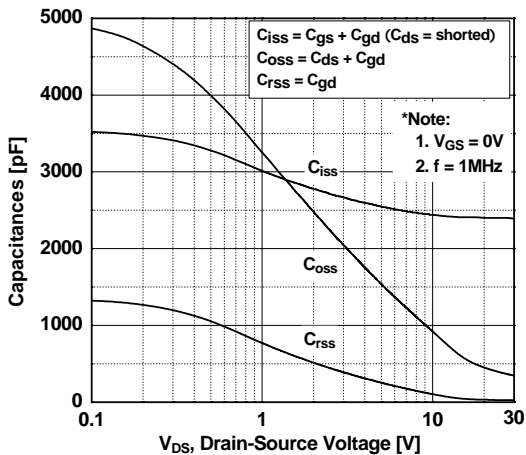
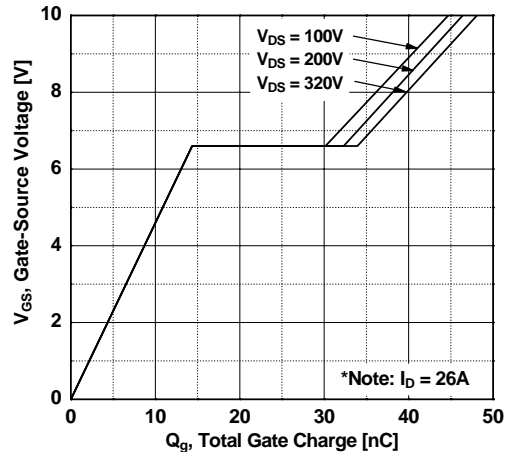


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

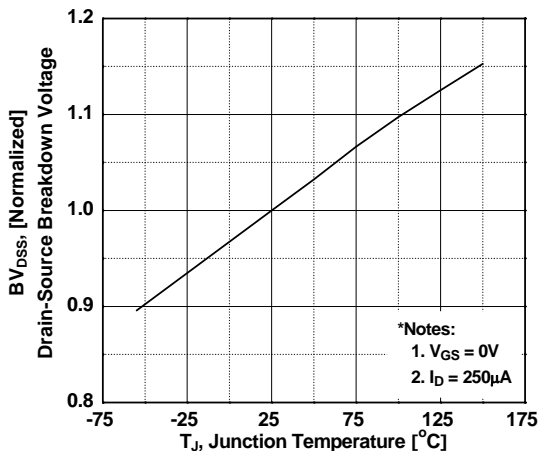


Figure 8. On-Resistance Variation vs. Temperature

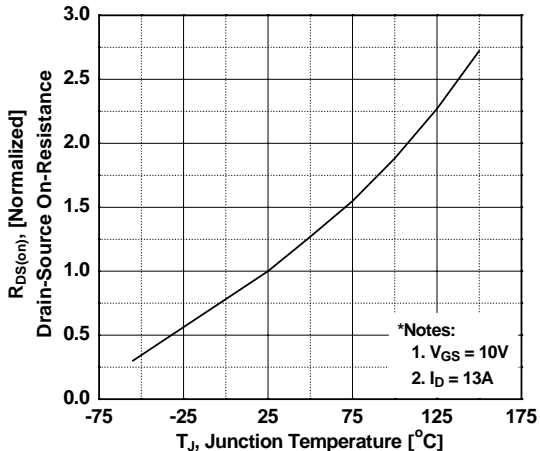


Figure 9. Maximum Safe Operating Area - FDP26N40

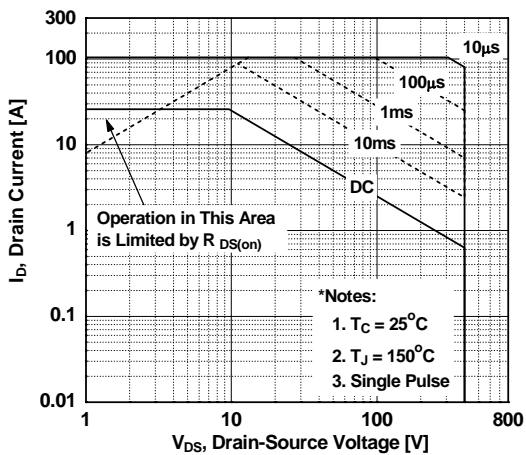


Figure 10. Maximum Safe Operating Area

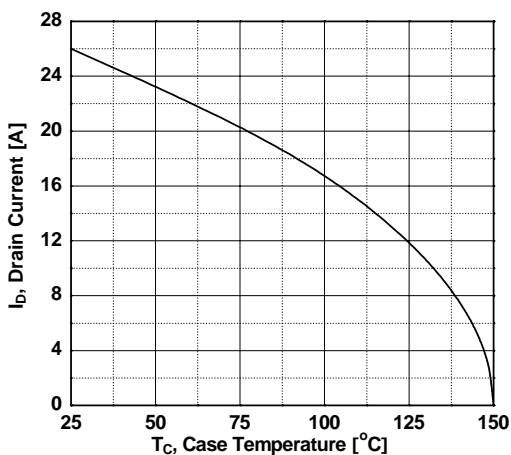
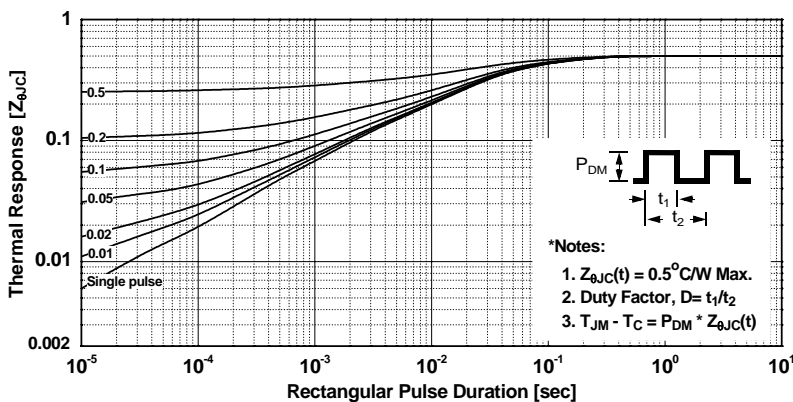
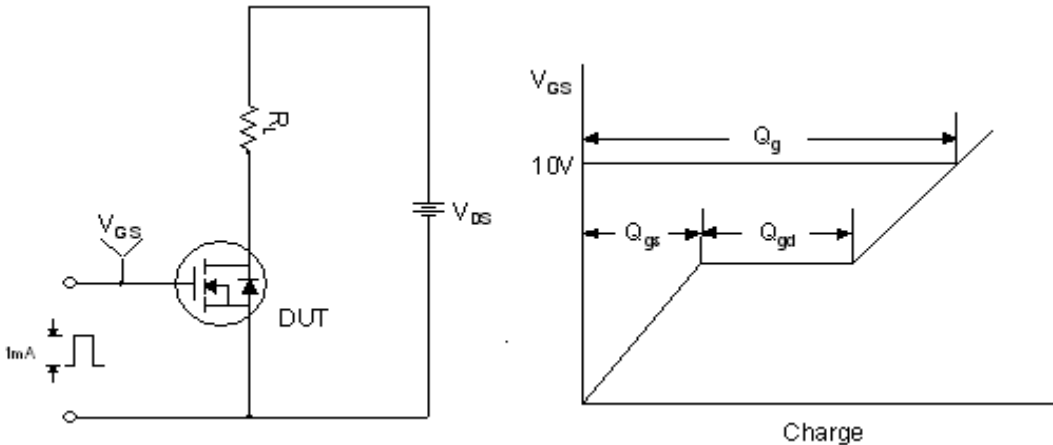


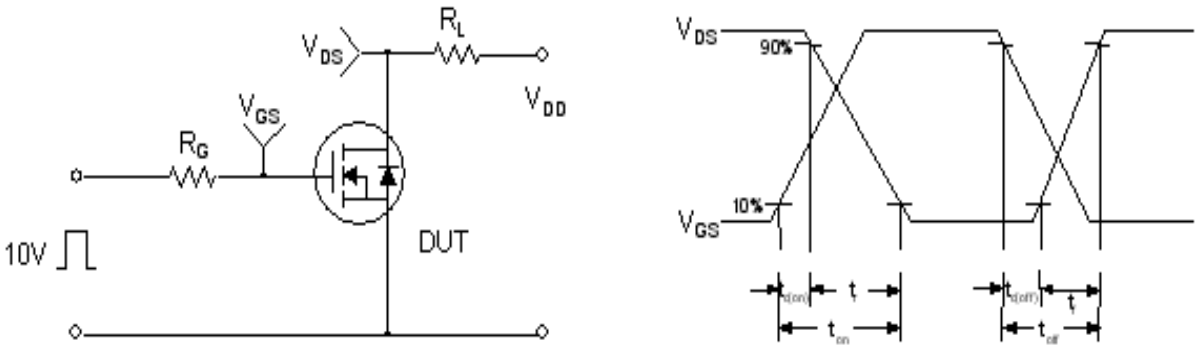
Figure 11. Transient Thermal Response Curve - FDP26N40



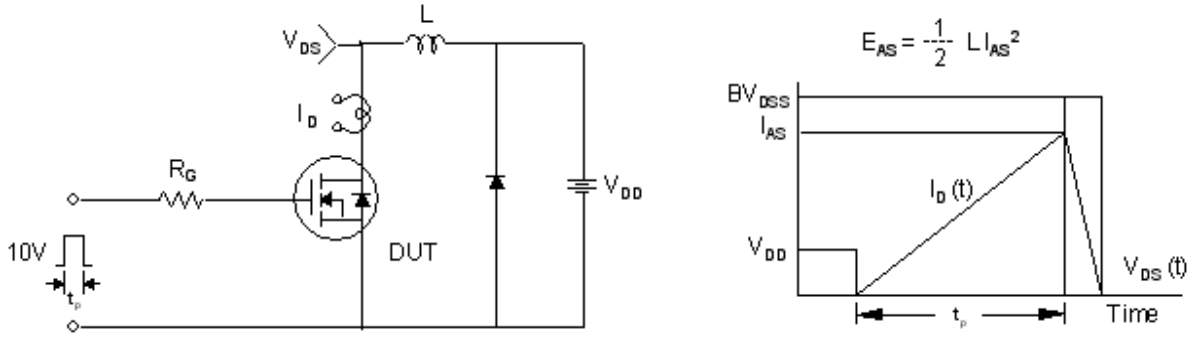
Gate Charge Test Circuit & Waveform



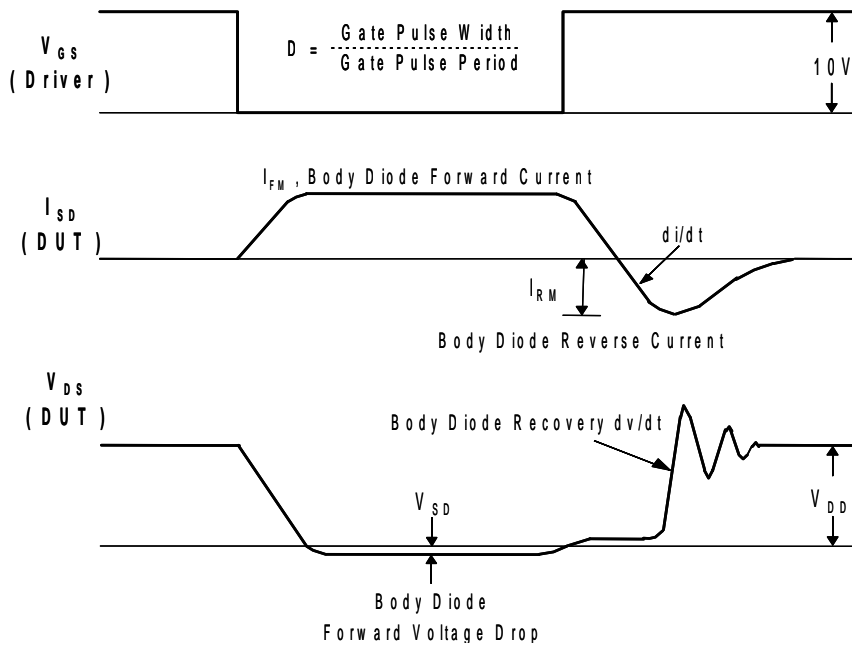
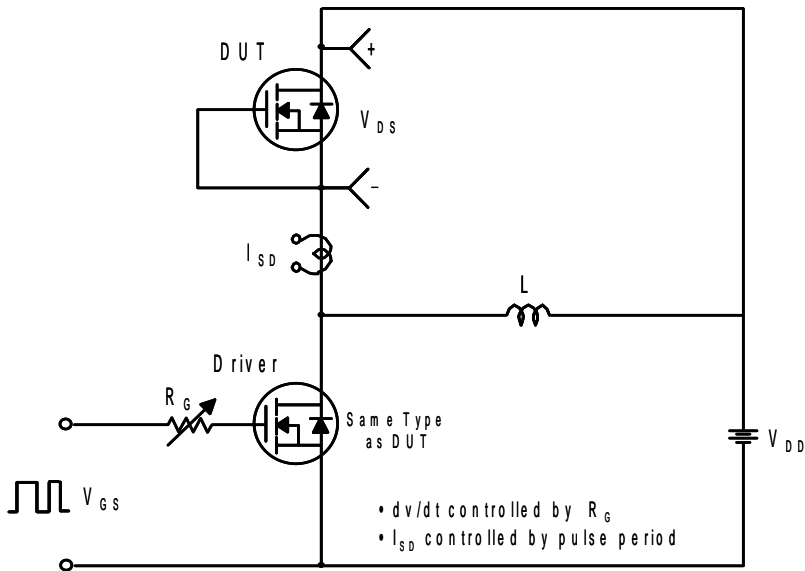
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

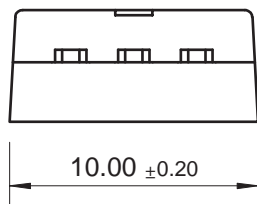
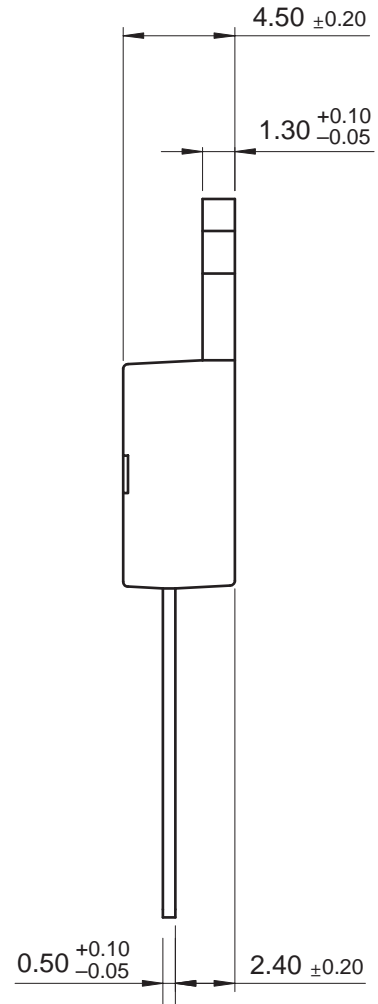
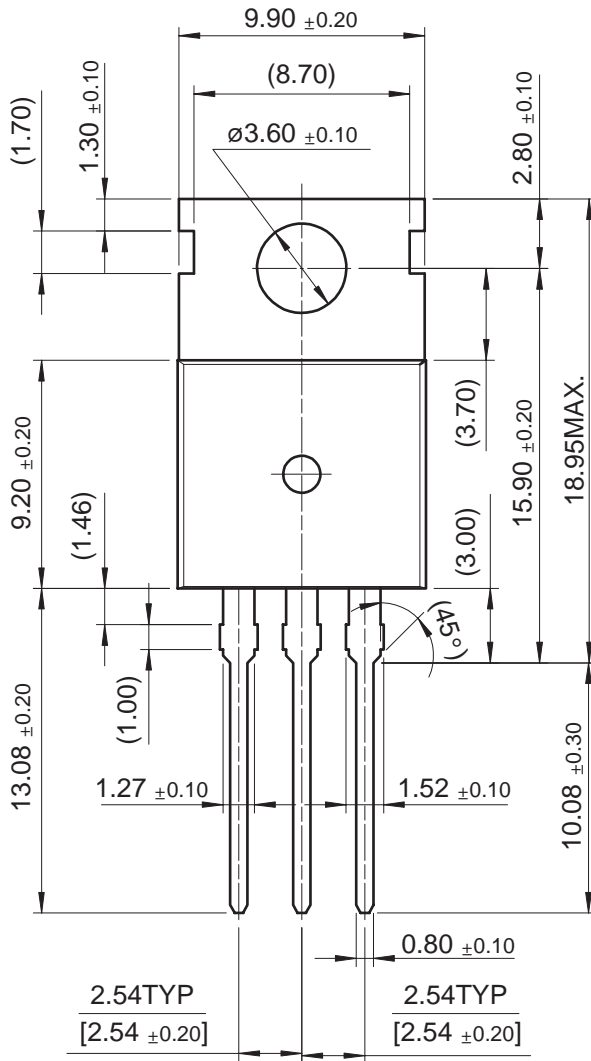


Peak Diode Recovery dv/dt Test Circuit & Waveforms



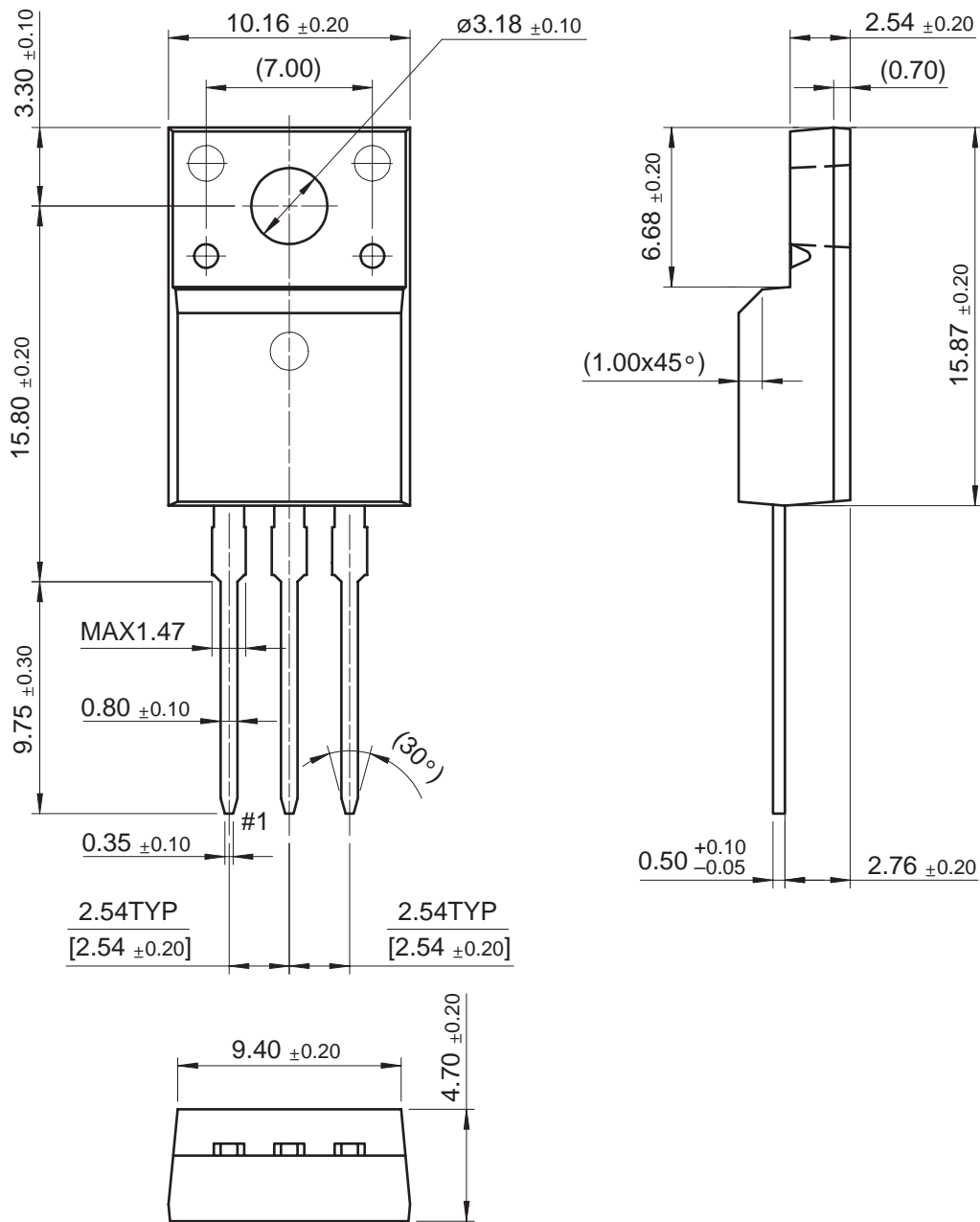
Mechanical Dimensions

TO-220



Mechanical Dimensions

TO-220F





Dimensions in Millimeters



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

ACE ^x ®	FPS TM	PDP-SPM TM	SupreMOS TM
Build it Now TM	FRFET [®]	Power220 [®]	SyncFET TM
CorePLUS TM	Global Power Resource SM	POWEREDGE [®]	SYSTEM [®]
CROSSVOLT TM	Green FPS TM	Power-SPM TM	GENERAL
CTL TM	Green FPS TM e-Series TM	PowerTrench [®]	The Power Franchise [®]
Current Transfer Logic TM	GTO TM	Programmable Active Droop TM	power [®]
EcoSPARK [®]	<i>i-Lo</i> TM	QFET [®]	the
EZSWITCH TM *	IntelliMAX TM	QS TM	franchise
 TM	ISOPLANAR TM	QT Optoelectronics TM	TinyBoost TM
 [®]	MegaBuck TM	Quiet Series TM	TinyBuck TM
Fairchild [®]	MICROCOUPLER TM	RapidConfigure TM	TinyLogic [®]
Fairchild Semiconductor [®]	MicroFET TM	SMART START TM	TINYOPTO TM
FACT Quiet Series TM	MicroPak TM	SPM [®]	TinyPower TM
FACT [®]	MillerDrive TM	STEALTH TM	TinyPWM TM
FAST [®]	Motion-SPM TM	SuperFET TM	TinyWire TM
FastvCore TM	OPTOLOGIC [®]	SuperSOT TM -3	µSerDes TM
FlashWriter [®] *	OPTOPLANAR [®]	SuperSOT TM -6	UHC [®]
		SuperSOT TM -8	Ultra FRFET TM
			UniFET TM
			VCX TM

* EZSWITCHTM and FlashWriter[®] are trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I33