FAIRCHILD SEMICONDUCTOR®

April 2005

# FDD6676AS

## 30V N-Channel PowerTrench® SyncFET™

### General Description

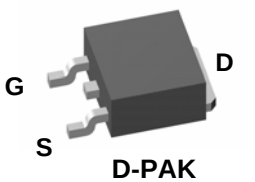
The FDD6676AS is designed to replace a single MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low $R_{DS(ON)}$ and low gate charge. The FDD6676AS includes a patented combination of a MOSFET monolithically integrated with a Schottky diode using Fairchild's monolithic SyncFET technology.

### Applications

- DC/DC converter
- Low side notebook

### Features

- 90 A, 30 V $R_{DS(ON)}$ = 5.7 mΩ @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 7.1 mΩ @ $V_{GS}$ = 4.5 V
- Includes SyncFET schottky body diode
- Low gate charge (46nC typical)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

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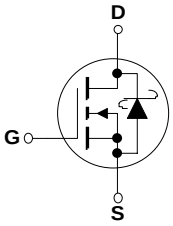


## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 3) | 90 | A |
| | – Pulsed | (Note 1a) | 100 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1) | 70 | W |
| | | (Note 1a) | 3.1 | |
| | | (Note 1b) | 1.3 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 1.8 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 40 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1b) | 96 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDD6676AS | FDD6676AS | 13'' | 12mm | 2500 units |
| FDD6676AS | FDD6676AS_NL (Note 4) | 13'' | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain-Source Avalanche Ratings (Note 2)** | | | | | | |
| $W_{DSS}$ | Drain-Source Avalanche Energy | Single Pulse, $V_{DD}$ = 15 V, $I_D$ = 16A | | 108 | 250 | mJ |
| $I_{AR}$ | Drain-Source Avalanche Current | | | | 16 | A |
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 10 mA, Referenced to 25°C | | 31 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 500 | μA |
| | | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V, $T_J$=125°C | | 11 | | mA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA | 1 | 1.5 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 10 mA, Referenced to 25°C | | –3.6 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 16 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 15 A<br>$V_{GS}$ = 10 V, $I_D$ = 16 A,$T_J$=125°C | | 4.7<br>5.8<br>6.7 | 5.7<br>7.1<br>8.4 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 16 A | | 61 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 2500 | | pF |
| $C_{oss}$ | Output Capacitance | | | 710 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 270 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 0 V, f = 1.0 MHz | | 1.6 | | Ω |
| **Switching Characteristics (Note 2)** | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 12 | 21 | ns |
| $t_r$ | Turn–On Rise Time | | | 12 | 22 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 46 | 74 | ns |
| $t_f$ | Turn–Off Fall Time | | | 28 | 44 | ns |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 4.5 V, $R_{GEN}$ = 6 Ω | | 20 | 32 | ns |
| $t_r$ | Turn–On Rise Time | | | 24 | 38 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 35 | 56 | ns |
| $t_f$ | Turn–Off Fall Time | | | 27 | 43 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge, Vgs = 10V | $V_{DS}$ = 15 V, $I_D$ = 16 A | | 46 | 64 | nC |
| $Q_g$ | Total Gate Charge, Vgs = 5V | | | 25 | 35 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 7 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 9 | | nC |

## Electrical Characteristics (continued)

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 3.5 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 3.5 A (Note 2) | | 0.4 | 0.7 | V |
| $t_{RR}$ | Diode Reverse Recovery Time | $dI_F/dt$ = 300A/us, $I_F$ = 16A | | 25 | | ns |
| $I_{RM}$ | Maximum Recovery Current | | | 1.9 | | A |
| $Q_{RR}$ | Diode Reverse Recovery Charge | | | 24 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ = 40°C/W when mounted on a 1in$^2$ pad of 2 oz copper

b) $R_{\theta JA}$ = 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

**3.** Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where $P_D$ is maximum power dissipation at $T_C$ = 25°C and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS}$ = 10V. Package current limitation is 21A

**4.** FDD6676AS_NL is a lead free product. The FDD6676AS_NL marking will appear on the reel label.

## Typical Characteristics

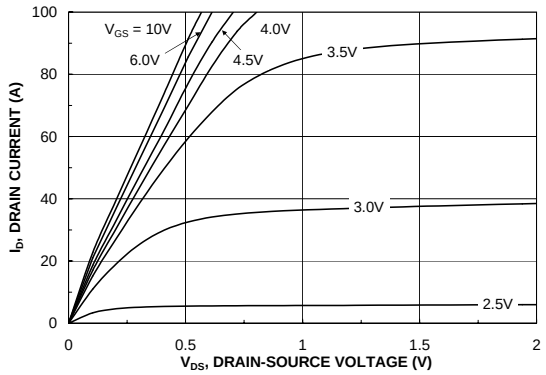


**Figure 1. On-Region Characteristics**

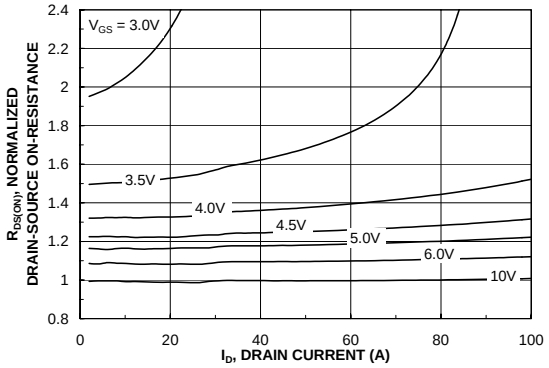


**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage**

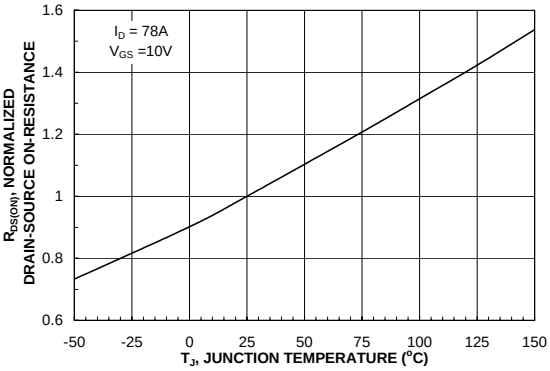


**Figure 3. On-Resistance Variation with Temperature**

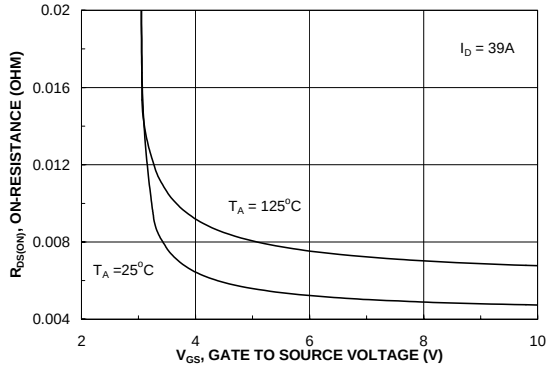


**Figure 4. On-Resistance Variation with Gate-to-Source Voltage**

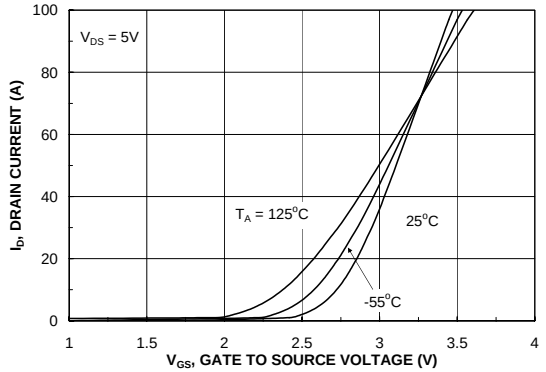


**Figure 5. Transfer Characteristics**

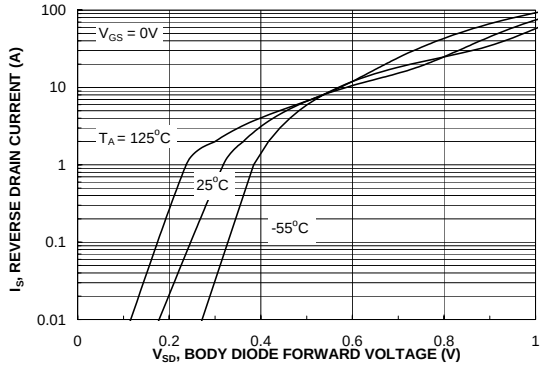


**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## Typical Characteristics

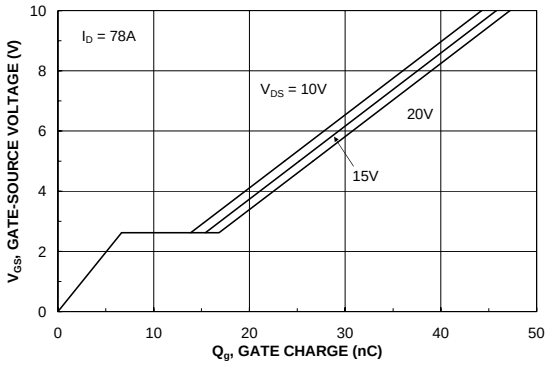


**Figure 7. Gate Charge Characteristics**

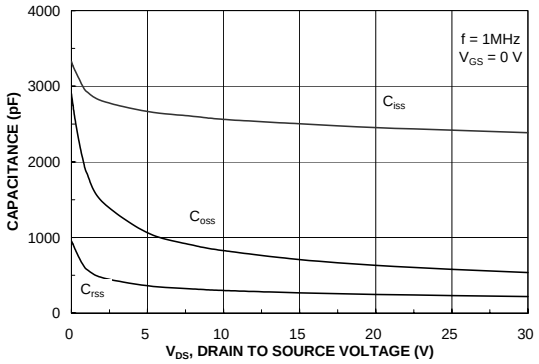


**Figure 8. Capacitance Characteristics**

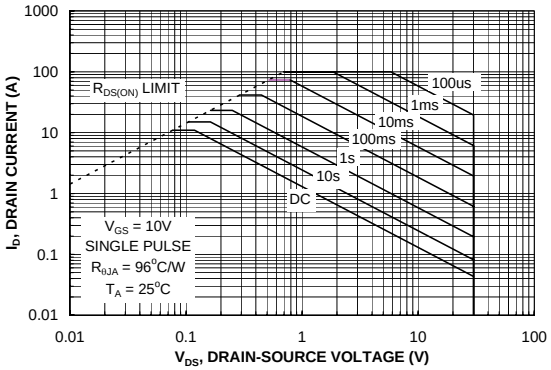


**Figure 9. Maximum Safe Operating Area**

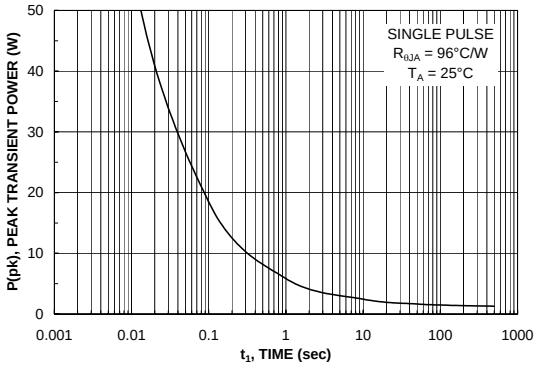


**Figure 10. Single Pulse Maximum Power Dissipation**

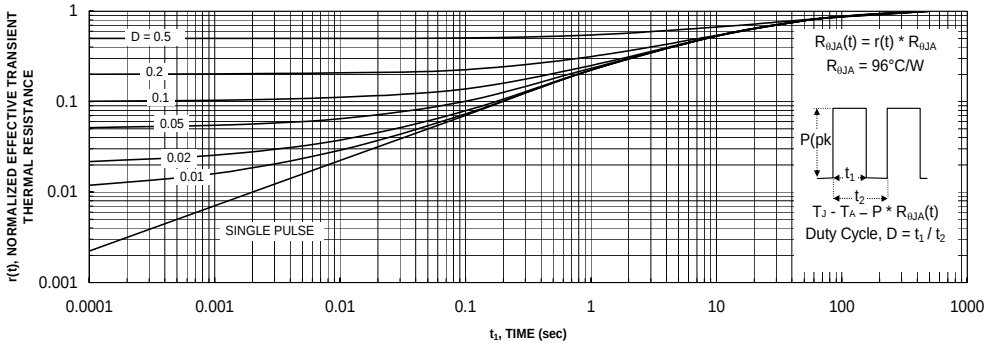


**Figure 11. Transient Thermal Response Curve**

**Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.**

## Typical Characteristics (continued)

### SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDD6676AS.

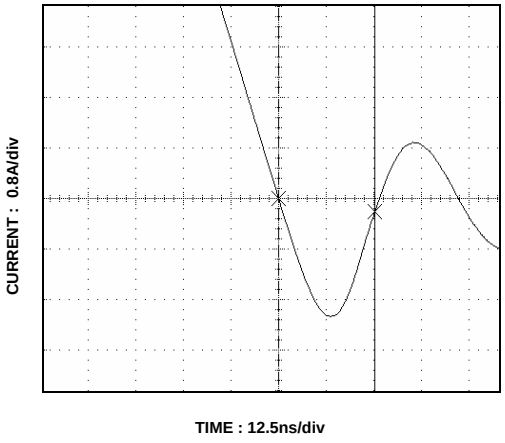


**Figure 12. FDD6676AS SyncFET body diode reverse recovery characteristic.**

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDD6676A).

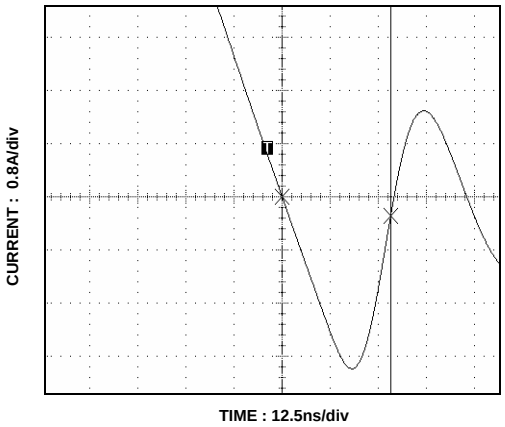


**Figure 13. Non-SyncFET (FDD6676A) body diode reverse recovery characteristic.**

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

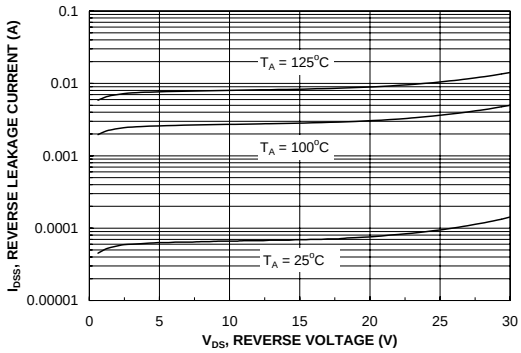


**Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.**

## Typical Characteristics

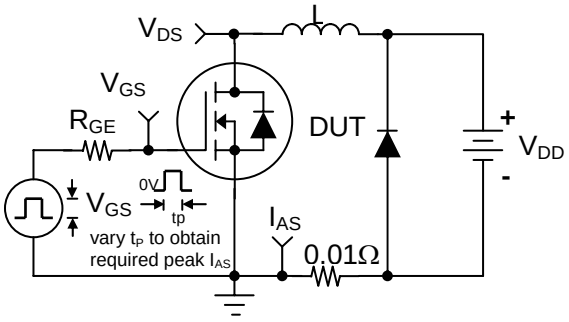


Figure 15. Unclamped Inductive Load Test Circuit

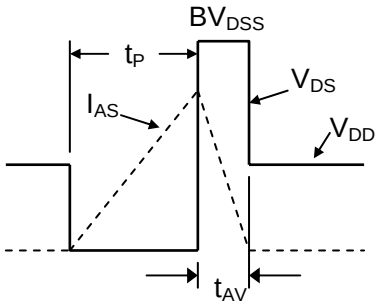


Figure 16. Unclamped Inductive Waveforms

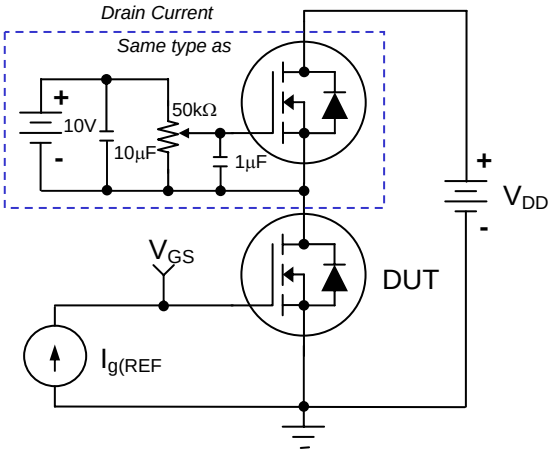


Figure 17. Gate Charge Test Circuit

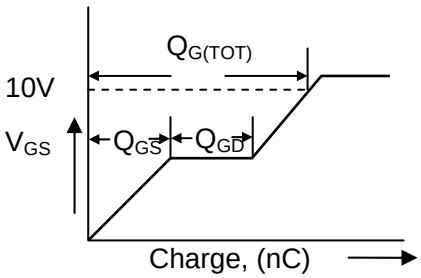


Figure 18. Gate Charge Waveform

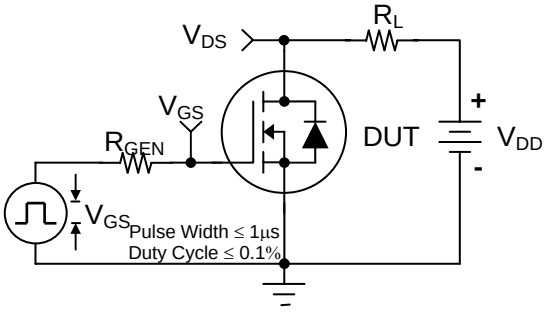


Figure 19. Switching Time Test Circuit

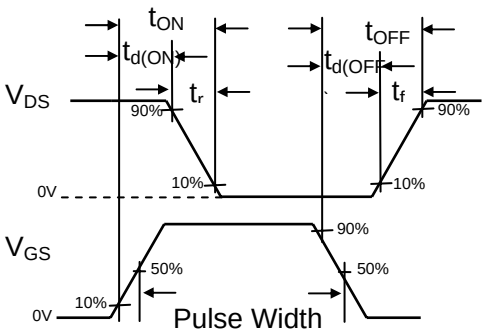


Figure 20. Switching Time Waveforms

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