

FDB12N50TM

N-Channel MOSFET

500V, 11.5A, 0.65Ω

Features

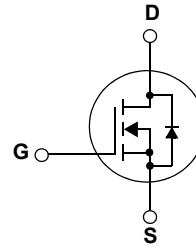
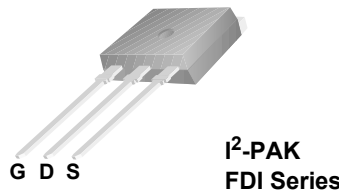
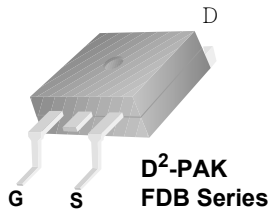
- $R_{DS(on)} = 0.55\Omega$ (Typ.) @ $V_{GS} = 10V, I_D = 6A$
- Low gate charge (Typ. 22nC)
- Low C_{rss} (Typ. 12pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant



Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	±30	V
I_D	Drain Current	-Continuous ($T_C = 25^\circ\text{C}$)	11.5
		-Continuous ($T_C = 100^\circ\text{C}$)	6.9
I_{DM}	Drain Current	- Pulsed (Note 1)	46
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	456
I_{AR}	Avalanche Current	(Note 1)	11.5
E_{AR}	Repetitive Avalanche Energy	(Note 1)	16.7
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	165
		- Derate above 25°C	1.33
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.75	$^\circ\text{C}/\text{W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction to Ambient*	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

*When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB12N50	FDB12N50TM	D ² -PAK	330mm	24mm	800
FDI12N50	FDI12N50TU	I ² -PAK	-	-	50

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.66	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 6\text{A}$	-	0.55	0.65	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 25\text{V}, I_D = 6\text{A}$ (Note 4)	-	11	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	985	1315	pF
C_{oss}	Output Capacitance		-	140	190	pF
C_{rss}	Reverse Transfer Capacitance		-	12	17	pF
Q_g	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 11.5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4, 5)	-	22	30	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	10	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 11.5\text{A}$ $R_G = 25\Omega$ (Note 4, 5)	-	25	60	ns
t_r	Turn-On Rise Time		-	60	130	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	105	ns
t_f	Turn-Off Fall Time		-	35	85	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	11.5	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	46	A	
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 11.5\text{A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 11.5\text{A}$	-	370	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\text{A}/\mu\text{s}$ (Note 4)	-	3.8	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 6.9\text{mH}, I_{AS} = 11.5\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 11.5\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

Peak Diode Recovery dv/dt Test Circuit & Waveforms

