Quadruple 64-bit static shift register

HEF4731B; HEF4731V
LSI

DESCRIPTION

The HEF4731B and HEF4731V are quadruple 64-bit static shift registers each with separate serial data inputs (D_A to D_D), clock inputs ($\overline{CP}_A$ to $\overline{CP}_D$) and data outputs (O_{63A} to O_{63D}) from the 64th register position.

Recommended supply voltage range for HEF4731B is 3 to 15 V and for HEF4731V is 4,5 to 12,5 V.

Data are shifted to the next stage on the negative-going transitions of the clock. Low impedance outputs are provided for direct interface to TTL.

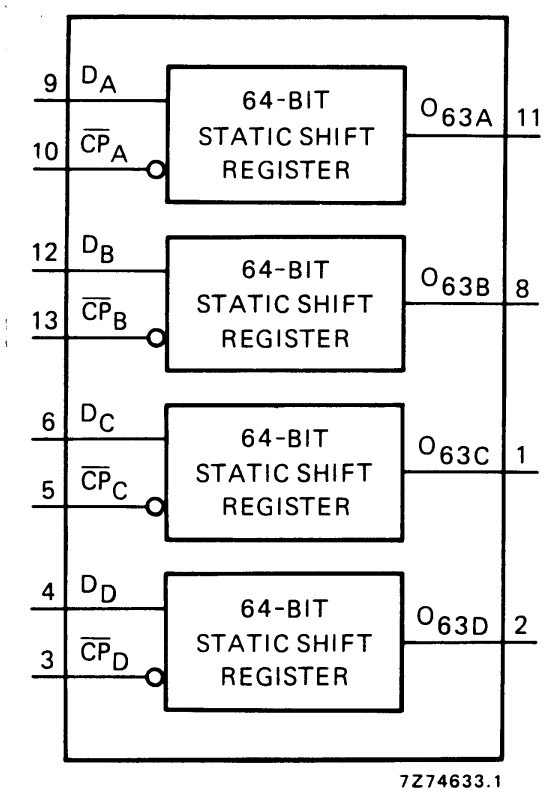

Fig.1 Functional diagram.

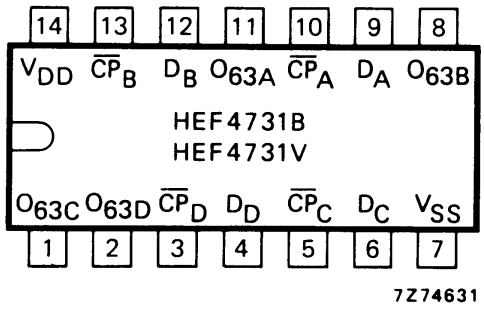

Fig.2 Pinning diagram.

HEF4731BP; HEF4731VP(N): 14-lead DIL; plastic (SOT27-1)

HEF4731BD; HEF4731VD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category LSI

See Family Specifications

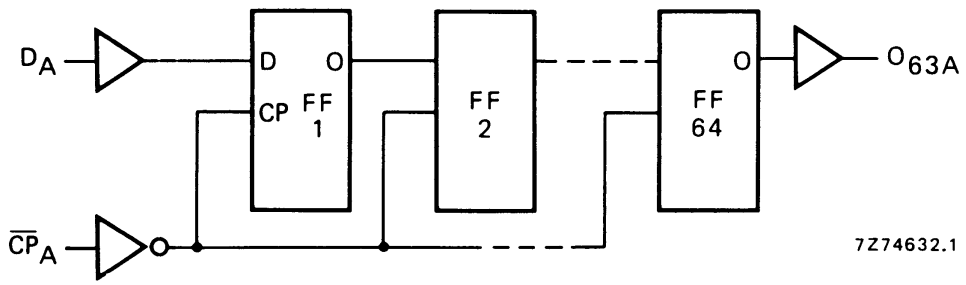

Fig.3 Logic diagram (one of 64-bits shift register).

The values given at V_{DD} = 15 V in the following DC and AC characteristics, are not applicable to the HEF4731V, because of its reduced supply voltage range.

DC CHARACTERISTICS

V_{SS} = 0 V; V_I = V_{SS} or V_{DD}

	V_{DD} V	V_{OL} V	V_{OH} V	SYMBOL	T_{amb} (°C)						
					−40		+ 25		+ 85		
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Output (source)	5		2,5	$-I_{OH}$	3		2,5		2,0		mA
current	5		4,6		1		0,85		0,65		mA
HIGH	10		9,5		3		2,5		2,0		mA
	15		13,5		10		8,5		6,5		mA
Output (sink)	4,75	0,4		I_{OL}	2,3		2,0		1,6		mA
current	10	0,5			6,0		5,0		4,0		mA
LOW	15	1,5			20,0		18,0		14,0		mA

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	13 000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	55 000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	140 000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)