October 1987 Revised April 2002 CD4503BC Hex Non-Inverting 3-STATE Buffer

CD4503BC

Hex Non-Inverting 3-STATE Buffer

General Description

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SEMICONDUCTOR

The CD4503BC is a hex non-inverting 3-STATE buffer with high output current sink and source capability. 3-STATE outputs make it useful in bus-oriented applications. Two separate disable inputs are provided. Buffers 1 through 4 are controlled by the disable 4 input. Buffers 5 and 6 are controlled by the disable 2 input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

Features

- \blacksquare Wide supply voltage range: 3.0 V_{DC} to 18 V_{DC}
- 3-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- Pin-for-pin replacement for MM80C97 and MC14503

Ordering Code:

Order Number	Package Number	Package Description
CD4503BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4503BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4503BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

OUT4

 \mathbf{v}_{SS}

IN₄

also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

 IN_5

оит₅

Connection Diagram IN₆

OUT₆

DIS₂

Vop

DIS4

IN₁

OUT₁

 IN_2

Top View

OUT2

 IN_3

OUT3



Truth Table

	In	Disable Input	Out
	0	0	0
	1	0	1
	Х	1	3-STATE
X = Don't C	are		

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CD4503BC

Absolute Maximum Ratings(Note 1) (Note 2)

Supply Voltage (V _{DD})	-0.5V to +18V
Input Voltage (V _{IN})	-0.5V to +0.5V
Storage Temperature Range (T _S)	$-65^{\circ}C$ to $+150^{\circ}C$
Power Dissipation (P _D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T _L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})

+3V to +15V -55°C to +125°C

Note 2: $V_{SS} = 0V$ unless otherwise specified.

DC Electrical Characteristics (Note 2)

Cumhal	Parameter	Conditions -	-5	–55°C		+25°C			+125°C	
Symbol			Min	Max	Min	Тур	Max	Min	Max	onits
I _{DD}	Quiescent Device	$V_{DD} = 5V,$		1			1		30	
	Current	$V_{IN} = V_{DD} \text{ or } V_{SS}$								
		$V_{DD} = 10V,$		2			2		60	
		$V_{IN} = V_{DD} \text{ or } V_{SS}$								μΛ
		V _{DD} = 15V,		4			4		120	
		$V_{IN} = V_{DD} \text{ or } V_{SS}$								
V _{OL}	LOW Level	$V_{IN} = V_{DD}$ or 0								
	Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	
V _{OH}	HIGH Level	$V_{IN} = V_{DD} \text{ or } 0$								
	Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		
VIL	LOW Level	$V_{DD} = 5V,$		1.5		2.25	1.5		1.5	
	Input Voltage	$V_{O} = 4.5V \text{ or } 0.5V$								
		$V_{DD} = 10V,$		3.0		4.50	3.0		3.0	
		V _O = 9.0V or 1.0V								v
		V _{DD} = 15V,		4.0		6.75	4.0		4.0	
		V _O = 13.5V or 1.5V								
VIH	HIGH Level	$V_{DD} = 5V,$	3.5		3.5	2.75		3.5		
	Input Voltage	$V_0 = 0.5V \text{ or } 4.5V$								
		V _{DD} = 10V,	7.0		7.0	5.5		7.0		V
		$V_0 = 1.0V \text{ or } 9.0V$								v
		$V_{DD} = 15V,$	11.0		11.0	8.25		11.0		
		V _O = 1.5V or 13.5V								
I _{OL}	LOW Level Output	$V_{DD} = 4.5V, V_{OL} = 0.4V$	2.8		2.3	2.55		1.60		
	Current	$V_{DD} = 5.0V, \ V_{OL} = 0.4V$	3.0		2.4	2.75		1.75		m (
		$V_{DD} = 10V, V_{OL} = 0.5V$	7.85		6.35	7.00		4.45		mA
		$V_{DD} = 15V, V_{OL} = 1.5V$	19.95		16.10	25.00		11.30		
I _{OH}	HIGH Level Output	$V_{DD} = 5V, V_{OH} = 4.6V$	-1.28		-1.02	-1.76		-0.7		
	Current	$V_{DD} = 10V, V_{OH} = 9.5V$	-3.20		-2.60	-4.5		-1.8		mA
		$V_{DD} = 15V, V_{OH} = 13.5V$	-8.20		-6.80	-17.6		-4.8		
l _{oz}	3-STATE Leakage Current	$V_{DD} = 15V$		±0.1		±10 ⁻⁴	±0.1		±1.0	μA
I _{IN}	Input Current	V _{DD} = 15V		±0.1		±10 ⁻⁴	±0.1		±1.0	μA

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical	Characteristics	(Note 4)
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$T_A = 25^\circ C, C_I$	$= 50 \text{ pF}, \text{ R}_{\text{L}} = 200 \text{ k}\Omega, \text{ Input}$	$t_r = t_f = 20$ ns, unless otherwise spe	cified				Ct C
Symbol	Parameter	Conditions	Min	Тур	Max	Units	L G
t _{PHL} , t _{PLH}	Propagation Delay Time	$V_{DD} = 5V$		75	100		Β
		$V_{DD} = 10V$		35	40	ns	ဂ
		$V_{DD} = 15V$		25	30		
t _{PLZ} , t _{PHZ}	Propagation Delay Time,	$V_{DD} = 5V$		80	125		
	Logical Level to HIGH	$V_{DD} = 10V$		40	90	ns	
	Impedance State	$V_{DD} = 15V$		35	70		
t _{PZL} , t _{PZH}	Propagation Delay Time,	$V_{DD} = 5V$		95	175		
	High Impedance State to	$V_{DD} = 10V$		40	80	ns	
	Logical Level	$V_{DD} = 15V$		35	70		
t _{TLH}	Output Rise Time	$V_{DD} = 5V$		45	80		
		$V_{DD} = 10V$		23	40	ns	
		$V_{DD} = 15V$		18	35		
t _{THL}	Output Fall Time	$V_{DD} = 5V$		45	80		
		$V_{DD} = 10V$		23	40	ns	
		$V_{DD} = 15V$		18	35		

Note 4: AC Parameters are guaranteed by DC correlated testing.









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