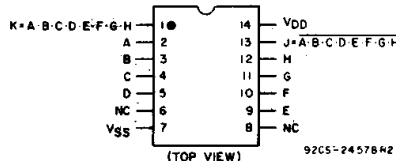


# CMOS 8-Input NAND/AND Gate

High-Voltage Types (20-Volt Rating)

■ CD4068B NAND/AND gate provides the system designer with direct implementation of the positive-logic 8-input NAND and AND functions and supplements the existing family of CMOS gates.

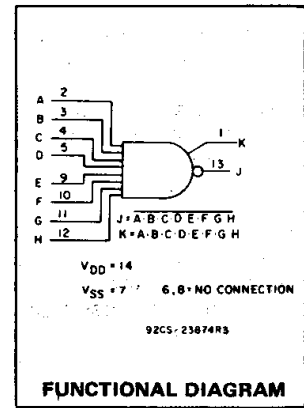
The CD4068B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline package (NSR suffix), and in chip form (H suffix).



NC = NO CONNECTION  
**TERMINAL ASSIGNMENT**

**Features:**

- Medium-Speed Operation:  
t<sub>PHL</sub>, t<sub>PLH</sub> = 75 ns (typ.) at V<sub>DD</sub> = 10 V
- Buffered inputs and outputs
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V<sub>DD</sub> = 5 V  
2 V at V<sub>DD</sub> = 10 V 2.5 V at V<sub>DD</sub> = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For T <sub>A</sub> = Full Package Temperature Range)	3	18	V

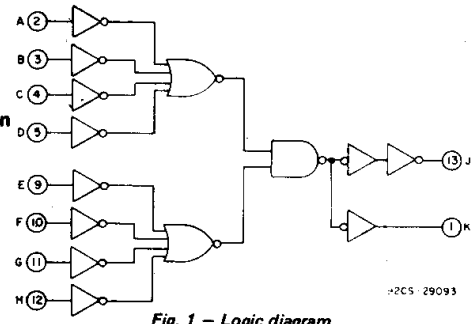


Fig. 1 – Logic diagram.

**STATIC ELECTRICAL CHARACTERISTICS**

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	–	0,5	5	0,25	0,25	7,5	7,5	–	0,01	0,25	μA
	–	0,10	10	0,5	0,5	15	15	–	0,01	0,5	
	–	0,15	15	1	1	30	30	–	0,01	1	
	–	0,20	20	5	5	150	150	–	0,02	5	
Output Low (Sink) Current I <sub>OL</sub> Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	–	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	–	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	–	
Output High (Source) Current, I <sub>OH</sub> Min.	4,6	0,5	5	–0,64	–0,61	–0,42	–0,36	–0,51	–1	–	mA
	2,5	0,5	5	–2	–1,8	–1,3	–1,15	–1,6	–3,2	–	
	9,5	0,10	10	–1,6	–1,5	–1,1	–0,9	–1,3	–2,6	–	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	–	0,5	5	0,05			–	0	0,05	–	V
	–	0,10	10	0,05			–	0	0,05	–	
	–	0,15	15	0,05			–	0	0,05	–	
Output Voltage: High-Level, V <sub>OH</sub> Min.	–	0,5	5	4,95			4,95	5	–	–	V
	–	0,10	10	9,95			9,95	10	–	–	
	–	0,15	15	14,95			14,95	15	–	–	
Input Low Voltage, V <sub>IL</sub> Max.	0,5,4,5	–	5	1,5			–	–	1,5	–	V
	1,9	–	10	3			–	–	3	–	
	1,5,13,5	–	15	4			–	–	4	–	
Input High Voltage, V <sub>IH</sub> Min.	0,5,4,5	–	5	3,5			3,5	–	–	–	V
	1,9	–	10	7			7	–	–	–	
	1,5,13,5	–	15	11			11	–	–	–	
Input Current I <sub>IN</sub> Max.		0,18	18	±0,1	±0,1	±1	±1	–	±10 <sup>–5</sup>	±0,1	μA

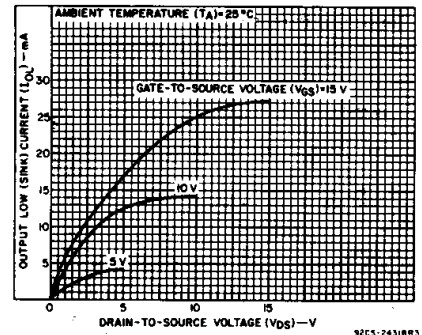


Fig. 2 – Typical output low (sink) current characteristics.

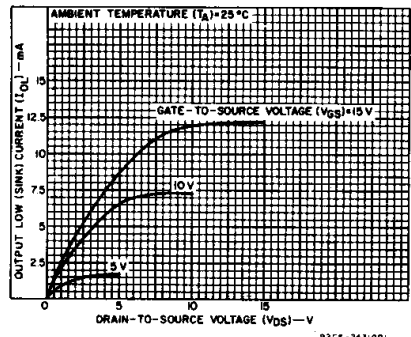


Fig. 3 – Minimum output low (sink) current characteristics.

**COMMERCIAL CMOS HIGH VOLTAGE ICs**

# CD4068B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	
Voltages referenced to $V_{SS}$ Terminal	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10mA$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ C$ to $+100^\circ C$	500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	Derate Linearly at 12mW/ $^\circ C$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79mm$ ) from case for 10s max	$+265^\circ C$

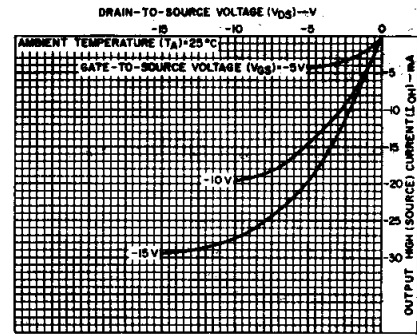


Fig. 4 - Typical output high (source) current characteristics.

## DYNAMIC ELECTRICAL CHARACTERISTICS

# CD4068B Types

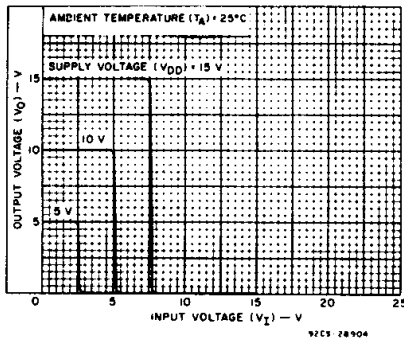


Fig. 9 - Typical voltage transfer characteristics (NAND output).

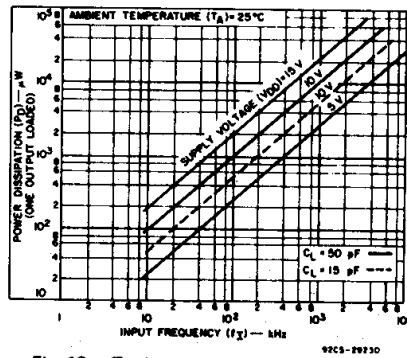


Fig. 10 - Typical dynamic power dissipation as a function of frequency.

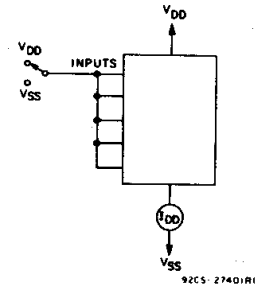


Fig. 11 - Quiescent-device-current test circuit.

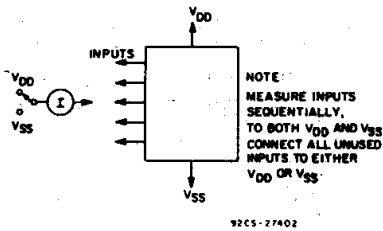


Fig. 12 - Input current test circuit.

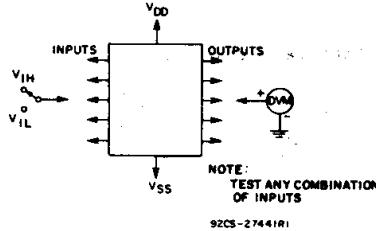


Fig. 13 - Input-voltage test circuit.

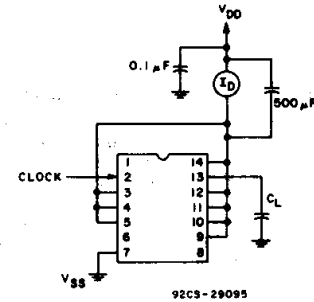
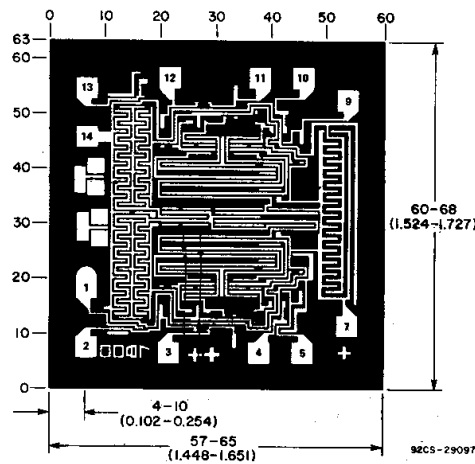


Fig. 14 - Dynamic power dissipation test circuit.



Dimensions and pad layout for CD4068BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

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