

DATA SHEET

74F564

Octal D flip-flop (3-State)

Product specification

1996 Jan 05

IC15 Data Handbook

Octal D flip-flop (3-State)

74F564

FEATURES

- 74F564 is broadside pinout version of 74F534
- Inputs and Outputs on opposite side of package allow easy interface to Microprocessors
- Useful as an Input or Output port for Microprocessors
- 3-State Outputs for Bus interfacing
- Common Output Enable
- 74F574 is a non-inverting version of 74F564

DESCRIPTION

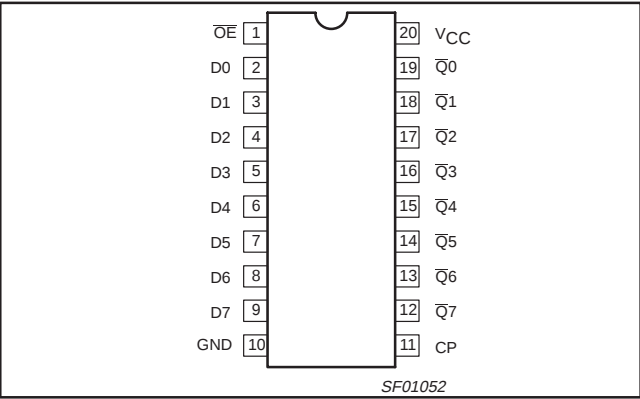
The 74F564 has a broadside pinout configuration to facilitate PC board layout and allows easy interface with microprocessors.

It is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition is transferred to the corresponding flip-flop's $\overline{Q}$ output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independently of the register operation. When $\overline{OE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION



TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F564	180MHz	50mA

ORDERING INFORMATION

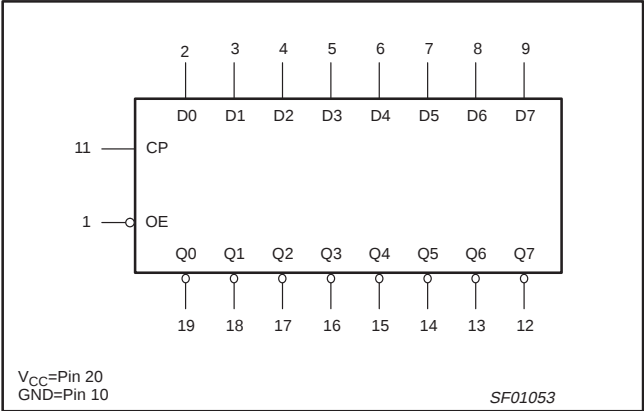
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG. DWG #
20-Pin Plastic DIP	N74F564N	SOT146-1
20-Pin Plastic SOL	N74F564D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

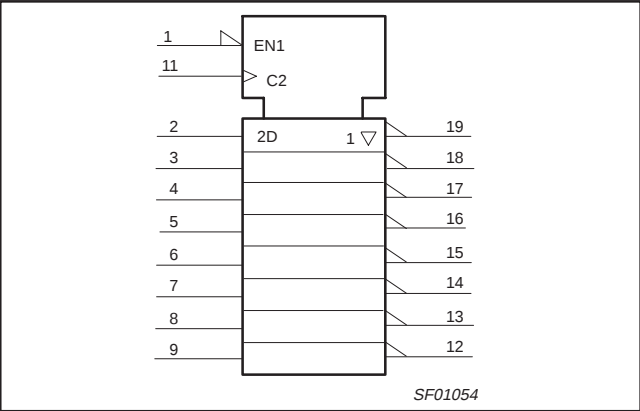
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20 μ A/0.6mA
$\overline{OE}$	Output Enable input (active Low)	1.0/1.0	20 μ A/0.6mA
CP	Clock Pulse input (active rising edge)	1.0/1.0	20 μ A/0.6mA
$\overline{Q0} - \overline{Q7}$	3-State outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 μ A in the High state and 0.6mA in the Low state.

LOGIC SYMBOL



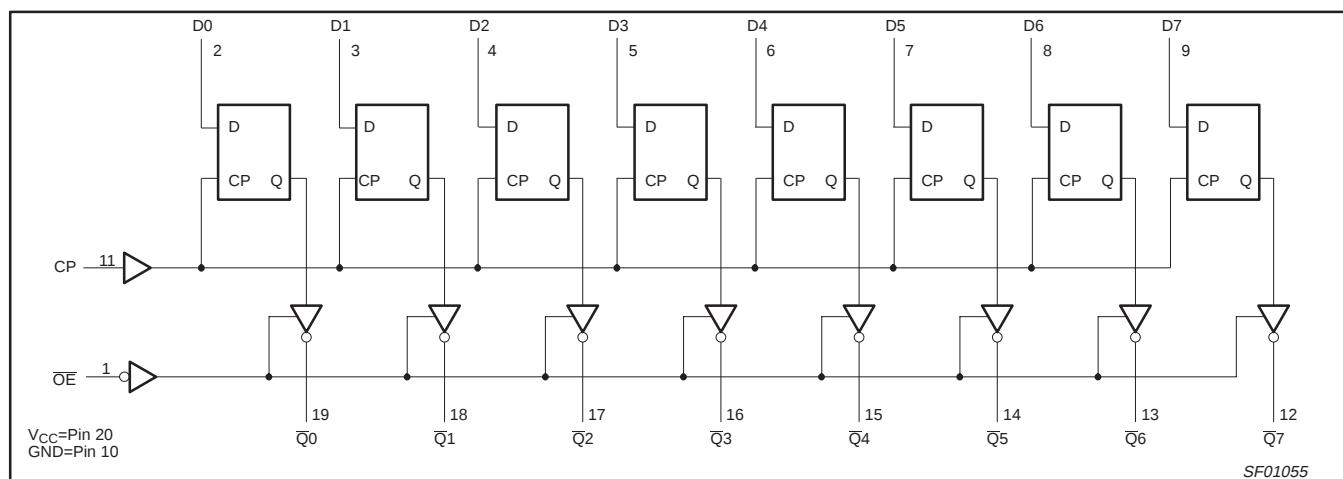
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODES
$\overline{OE}$	CP	Dn		$\overline{Q}0 - \overline{Q}7$	
L	$\uparrow$	l	L	H	Load and read register
L	$\uparrow$	h	H	L	
L	$\uparrow$	X	NC	NC	Hold
H	$\uparrow$	X	NC	Z	Disable outputs
H	$\uparrow$	Dn	Dn	Z	

H	=	High voltage level
h	=	High voltage level one setup time prior to the Low-to-High clock transition
L	=	Low voltage level
l	=	Low voltage level one setup time prior to the Low-to-High clock transition
NC	=	No change
X	=	Don't care
Z	=	High impedance "off" state
↑	=	Low-to-High clock transition
⤴	=	Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	−0.5 to +7.0	V
V _{IN}	Input voltage	−0.5 to +7.0	V
I _{IN}	Input current	−30 to +5.0	mA
V _{OUT}	Voltage applied to output in High output state	−0.5 to +V _{CC}	V
I _{OUT}	Current applied to output in Low output state	48	mA
T _{amb}	Operating free-air temperature range	0 to +70	°C
T _{stg}	Storage temperature	−65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ^{NO TAG}		LIMITS			UNIT
				MIN	TYP NO TAG	MAX	
V _{OH}	High-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	±10%V _{CC}	2.4			V
			±5%V _{CC}	2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OL} = MAX	±10%V _{CC}		0.35	0.50	V
			±5%V _{CC}		0.35	0.50	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			−0.73	−1.2	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				100	μA
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.5V				−0.6	mA
I _{OZH}	Off-state output current, High-level voltage applied	V _{CC} = MAX, V _O = 2.7V				50	μA
I _{OZL}	Off-state output current, Low-level voltage applied	V _{CC} = MAX, V _O = 0.5V				−50	μA
I _{OS}	Short-circuit output current ^{NO TAG}	V _{CC} = MAX		−60		−150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX		45	65	mA
		I _{CCL}			50	75	mA
		I _{CCZ}			55	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5V ± 10% C _L = 50pF, R _L = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
f _{MAX}	Maximum Clock frequency	Waveform NO TAG	160	180		150		MHz	
t _{PLH} t _{PHL}	Propagation delay CP to Qn	Waveform NO TAG	3.5 3.5	5.0 5.0	8.0 8.0	3.0 3.0	8.5 8.5	ns	
t _{PZH} t _{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.0	4.5 5.5	7.5 8.0	2.0 3.5	8.0 8.5	ns	
t _{PHZ} t _{PLZ}	Output Disable time from High or Low level	Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns	

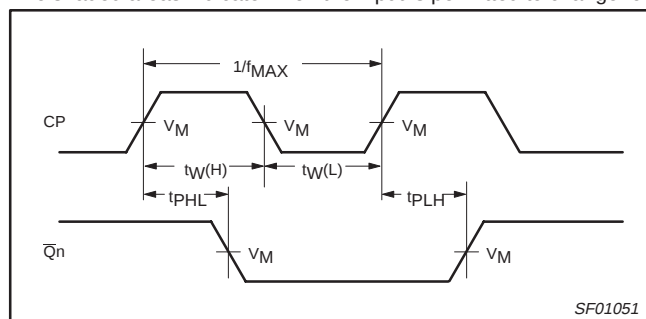
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t _S (H) t _S (L)	Setup time, Dn to CP	Waveform 3	2.0 2.0			2.0 2.5		ns
t _h (H) t _h (L)	Hold time, Dn to CP	Waveform 3	1.0 1.0			1.5 1.5		ns
t _w (H) t _w (L)	CP pulse width, High or Low	Waveform NO TAG	3.5 3.5			3.5 3.5		ns

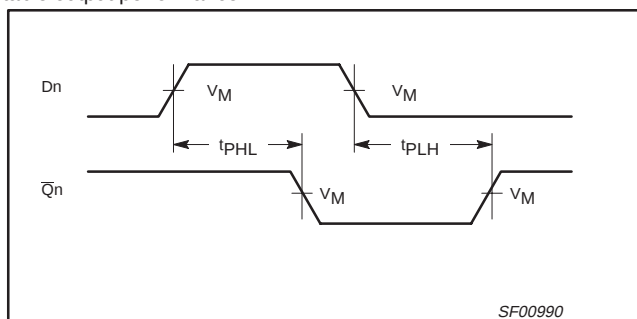
AC WAVEFORMS

For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable, Clock Pulse Widths, and Maximum Clock Frequency



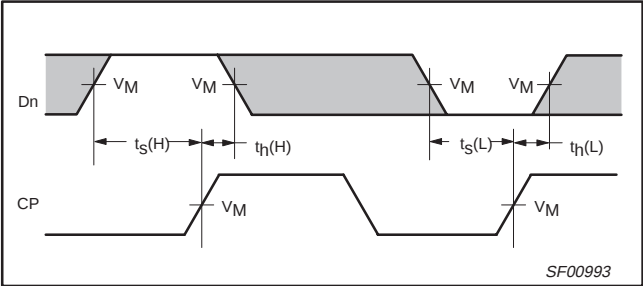
Waveform 2. Propagation Delay for Data to Outputs

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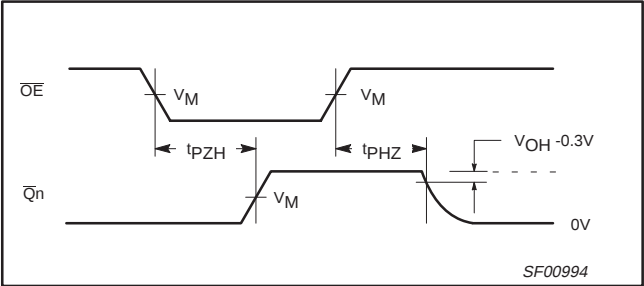
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AC WAVEFORMS (Continued)

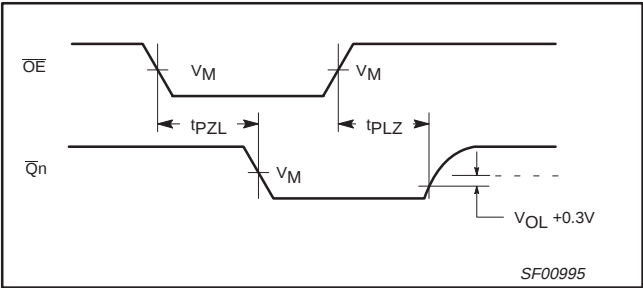
For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.



Waveform 3. Data Setup and Hold Times

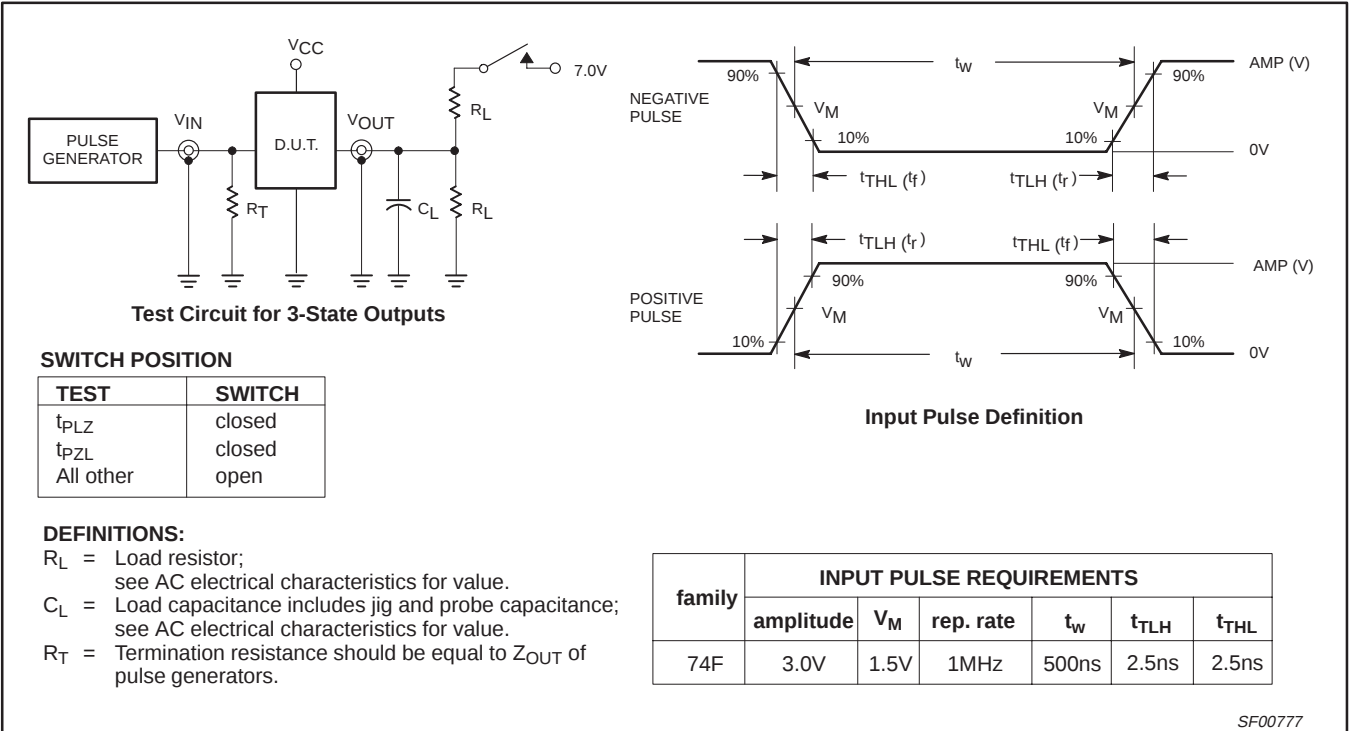


Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



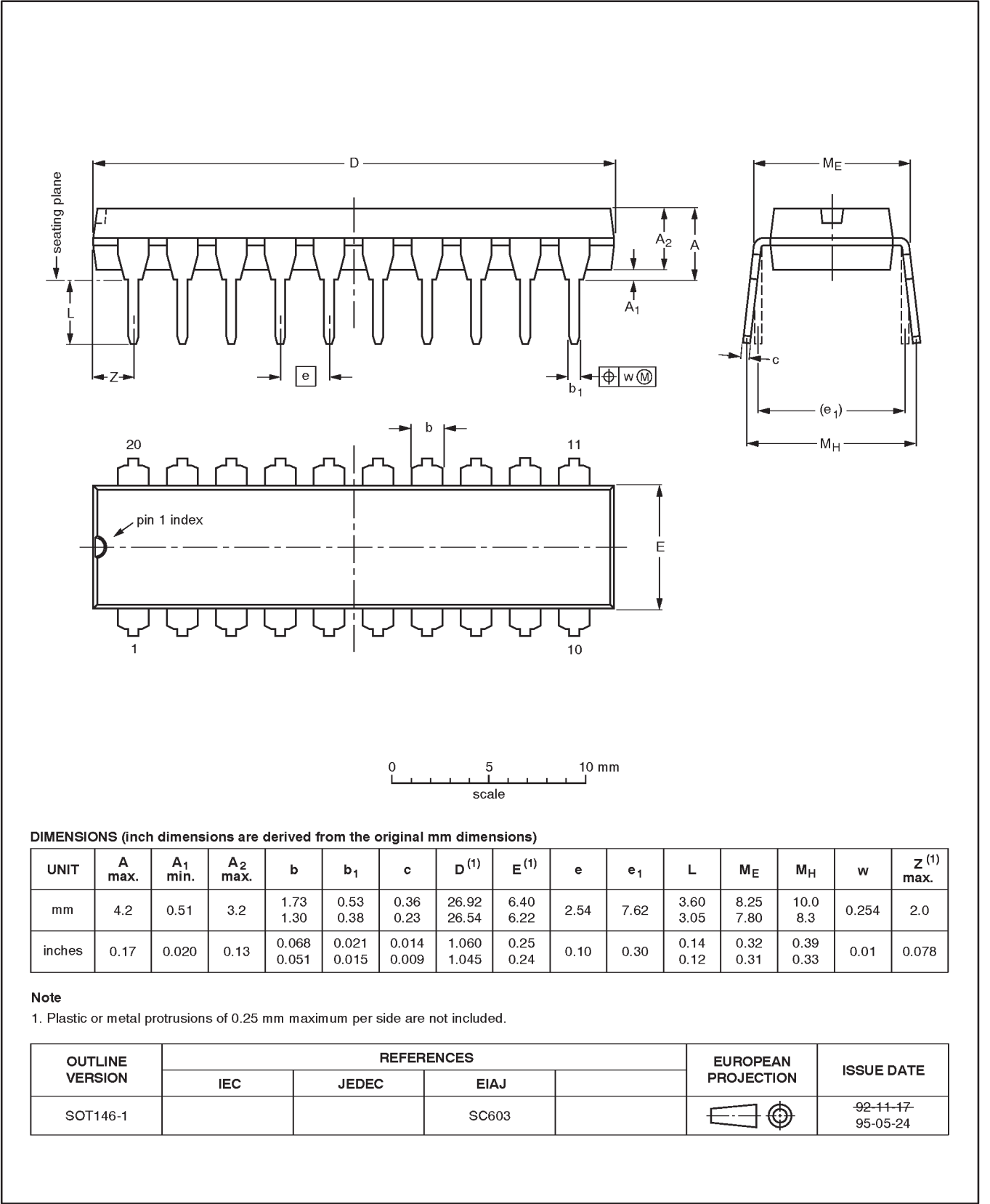
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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

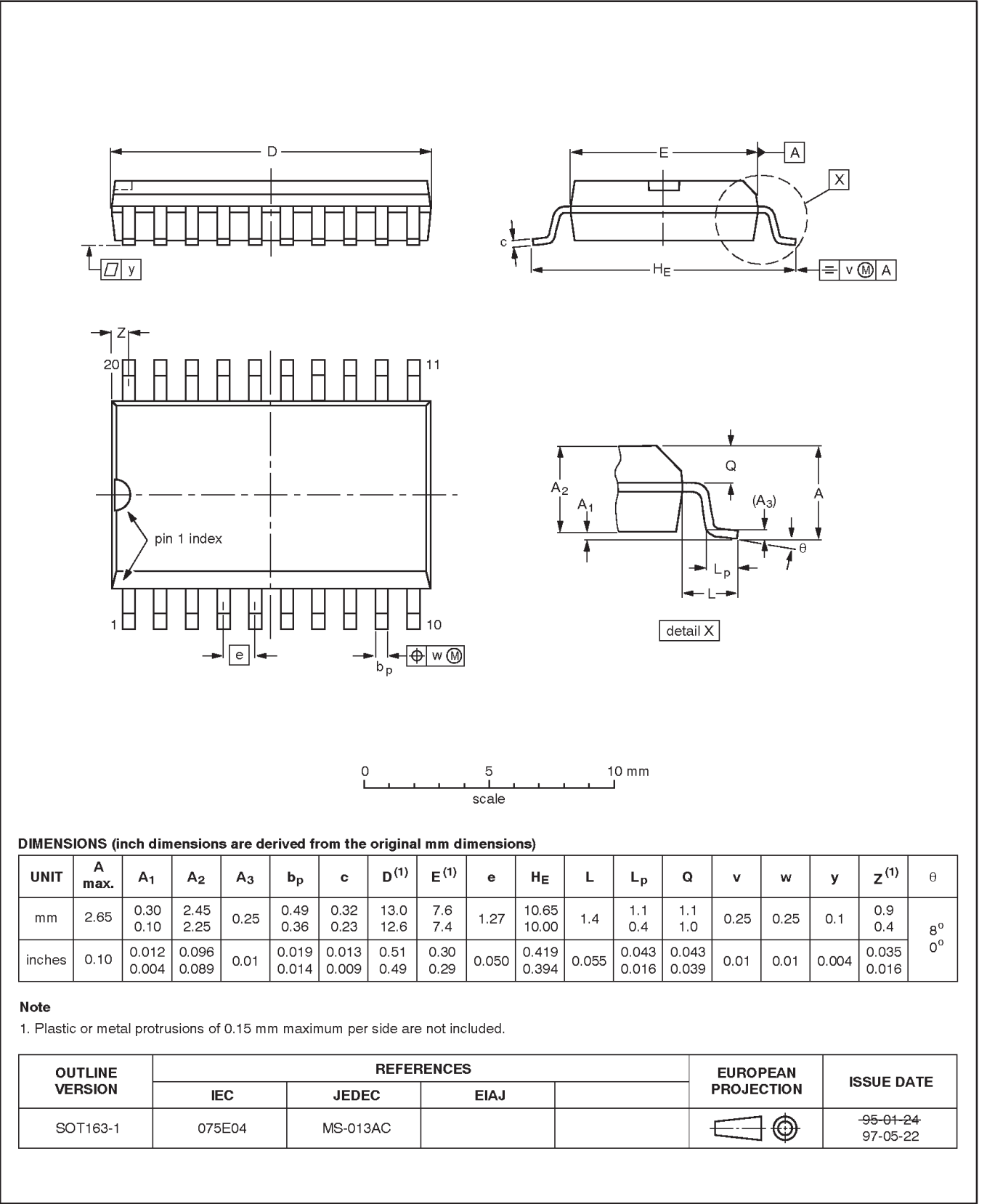


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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



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NOTES

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DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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