

# DATA SHEET

## **74F456**

Octal buffer/driver with parity,  
non-inverting (3-State)

Product specification  
Supersedes data of 1999 Jan 08  
IC15 Data Handbook

2000 Aug 01

Octal buffer/driver with parity, non-inverting (3-State)

74F456

FEATURES

- High impedance NPN base inputs for reduced loading (40µA in High and Low states)
- 74F456 combines 74F244 and 74F280A functions in one package
- 74F456 is a center pin version of the 74F656A
- Non-Inverting
- 3-State outputs sink 64mA and source 15mA
- 24-pin plastic Slim DIP (300 mil) package
- Broadside pinout simplifies PC board layout

DESCRIPTION

The 74F456 is an octal buffer and line driver with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F456	7.5ns	64mA

ORDERING INFORMATION

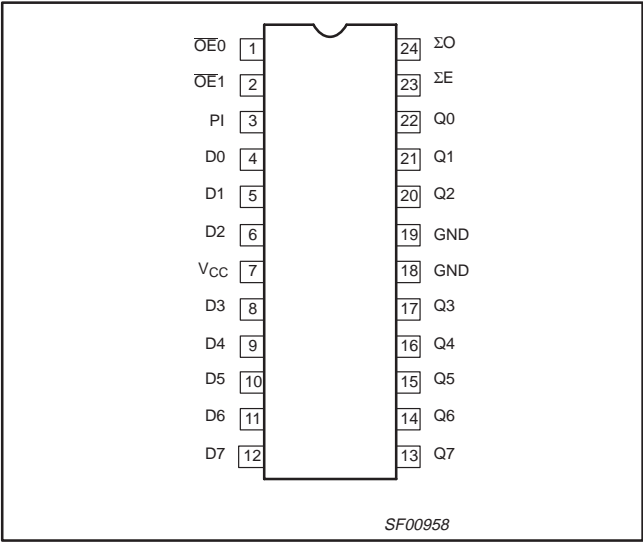
DESCRIPTION	COMMERCIAL RANGE V <sub>CC</sub> = 5V ±10%, T <sub>amb</sub> = 0°C to +70°C	PKG DWG #
24-pin plastic Slim DIP (300mil)	N74F456N	SOT222-1
24-pin plastic SOL	N74F456D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

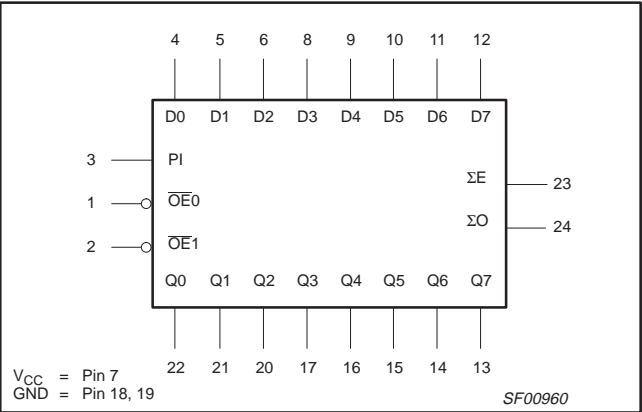
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0–D7	Data inputs	2.0/0.066	40µA/40µA
PI	Parity input	1.0/0.033	20µA/20µA
OE0, OE1	Output Enable inputs (active Low)	1.0/0.033	20µA/20µA
ΣE, ΣO	Parity outputs	750/106.7	15mA/64mA
Q0–Q7	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



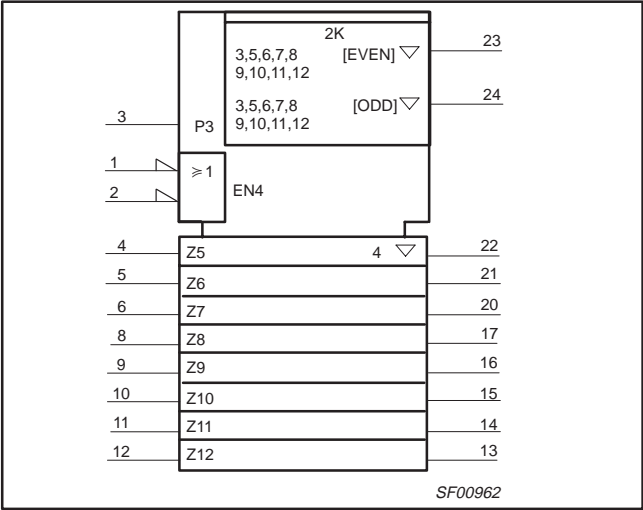
LOGIC SYMBOL



Octal buffer/driver with parity, non-inverting (3-State)

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LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS			OUTPUTS
OE0	OE1	Dn	Qn
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = High voltage level  
L = Low voltage level  
Z = High impedance "off" state  
X = Don't care

FUNCTION TABLE for PARITY OUTPUTS

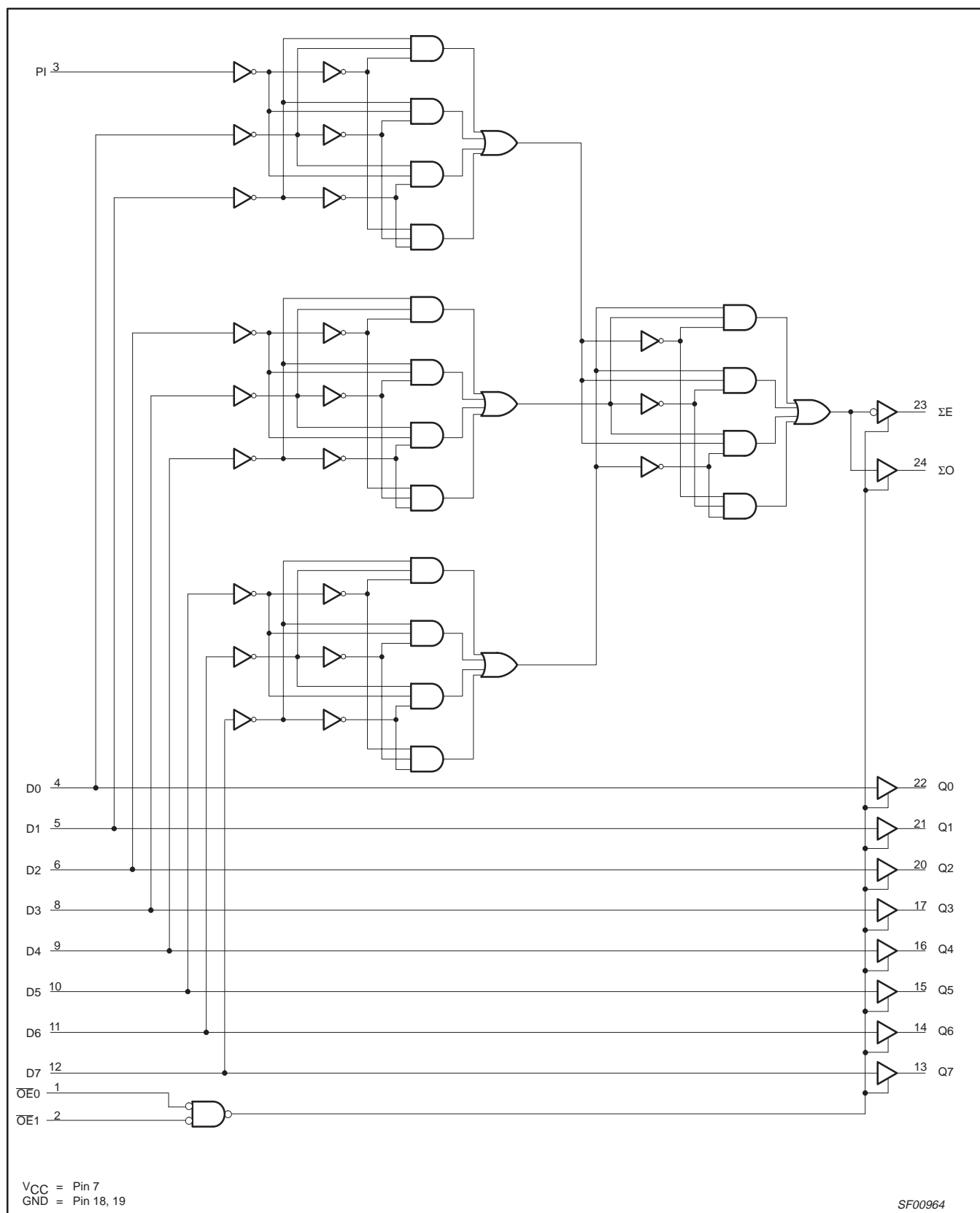
INPUTS	OUTPUTS	
Number of inputs, High (PI, D0 - D7)	ΣE	ΣO
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any OE <sub>n</sub> = High	Z	Z

H = High voltage level  
L = Low voltage level  
Z = High impedance "off" state  
X = Don't care

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## LOGIC DIAGRAM



SF00964

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	−0.5 to +7.0	V
$V_{IN}$	Input voltage	−0.5 to +7.0	V
$I_{IN}$	Input current	−30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	−0.5 to + $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	128	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature range	−65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			−18	mA
$I_{OH}$	High-level output current			−15	mA
$I_{OL}$	Low-level output current			64	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

## Octal buffer/driver with parity, non-inverting (3-State)

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**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT
						MIN	TYP <sup>2</sup>	MAX	
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V
					±5%V <sub>CC</sub>	2.7	3.3		V
				I <sub>OH</sub> = -15mA	±10%V <sub>CC</sub>	2.0			V
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>			0.55	V
					±5%V <sub>CC</sub>		0.42	0.55	V
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V
I <sub>I</sub>	Input current at maximum input voltage		V <sub>CC</sub> = 0.0V, V <sub>I</sub> = 7.0V					100	μA
I <sub>IH</sub>	High-level input current	Dn	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					40	μA
		PI, $\overline{OE}$ n						20	μA
I <sub>IL</sub>	Low-level input current	Dn	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-40	μA
		PI, $\overline{OE}$ n						-20	μA
I <sub>OZH</sub>	Off-state output current High-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					50	μA
I <sub>OZL</sub>	Off-state output current Low-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V					-50	μA
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX			-100		-225	mA
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				50	80	mA
		I <sub>CCL</sub>					78	110	mA
		I <sub>CCZ</sub>					63	90	mA

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**AC ELECTRICAL CHARACTERISTICS**

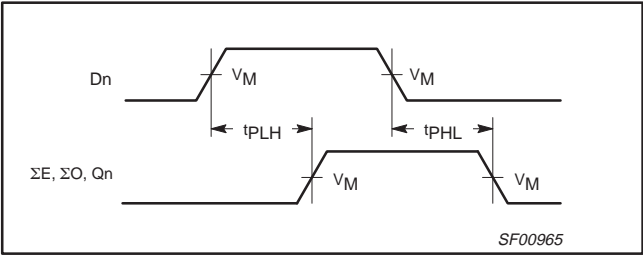
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to Qn	Waveform 1	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.0 7.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay Dn to ΣE, ΣO	Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	14.0 16.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level	Waveform 3 Waveform 4	2.5 4.0	4.0 8.0	8.0 10.5	2.5 4.0	9.0 11.5	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level	Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	7.5 8.0	ns

Octal buffer/driver with parity, non-inverting (3-State)

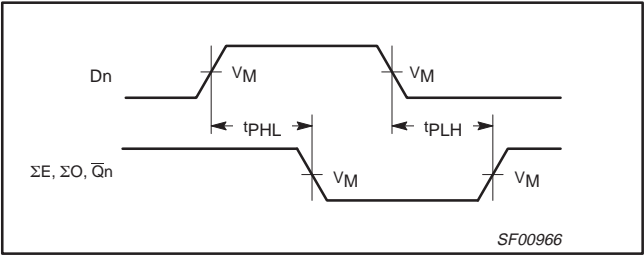
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AC WAVEFORMS

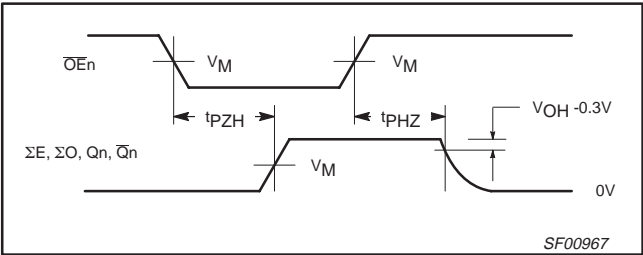
For all waveforms,  $V_M = 1.5V$ .



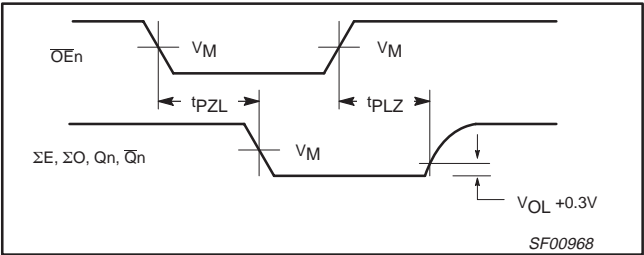
Waveform 1. Propagation Delay, Non-Inverting Outputs



Waveform 2. Propagation Delay, Inverting Outputs

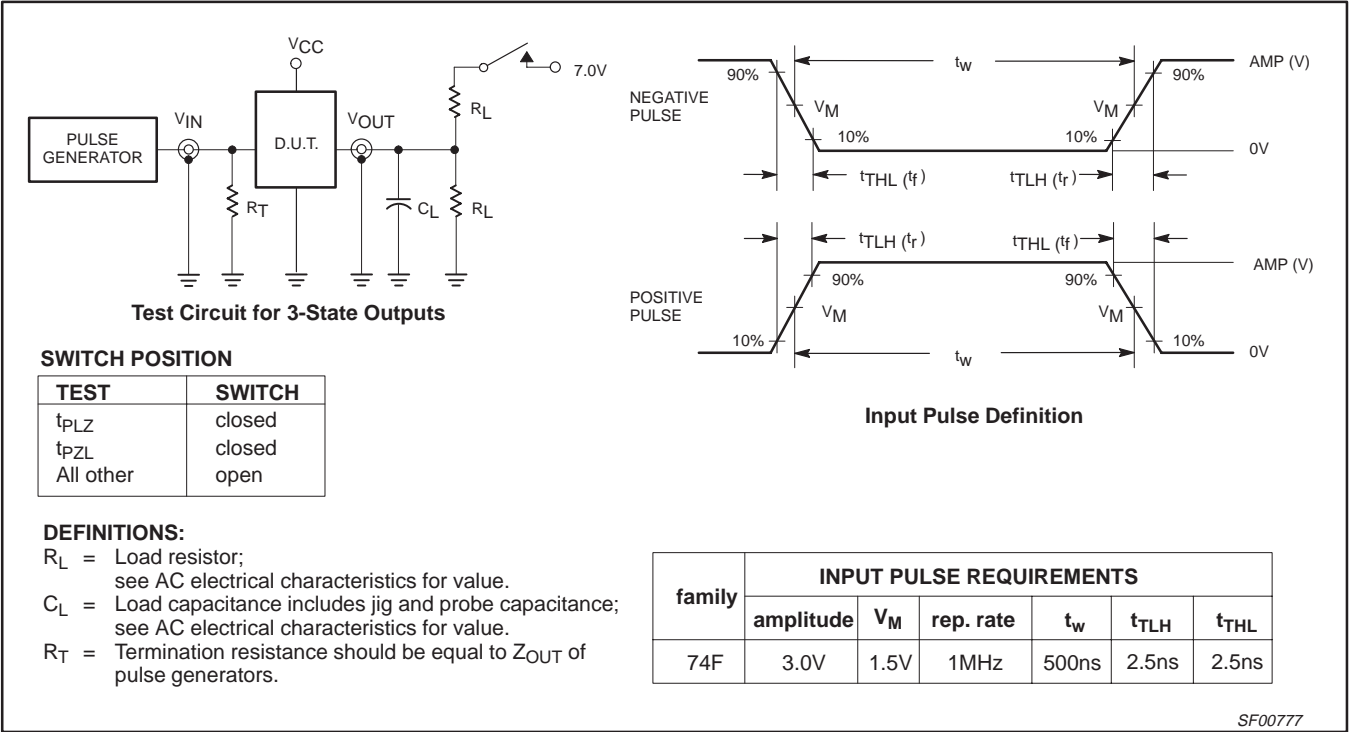


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

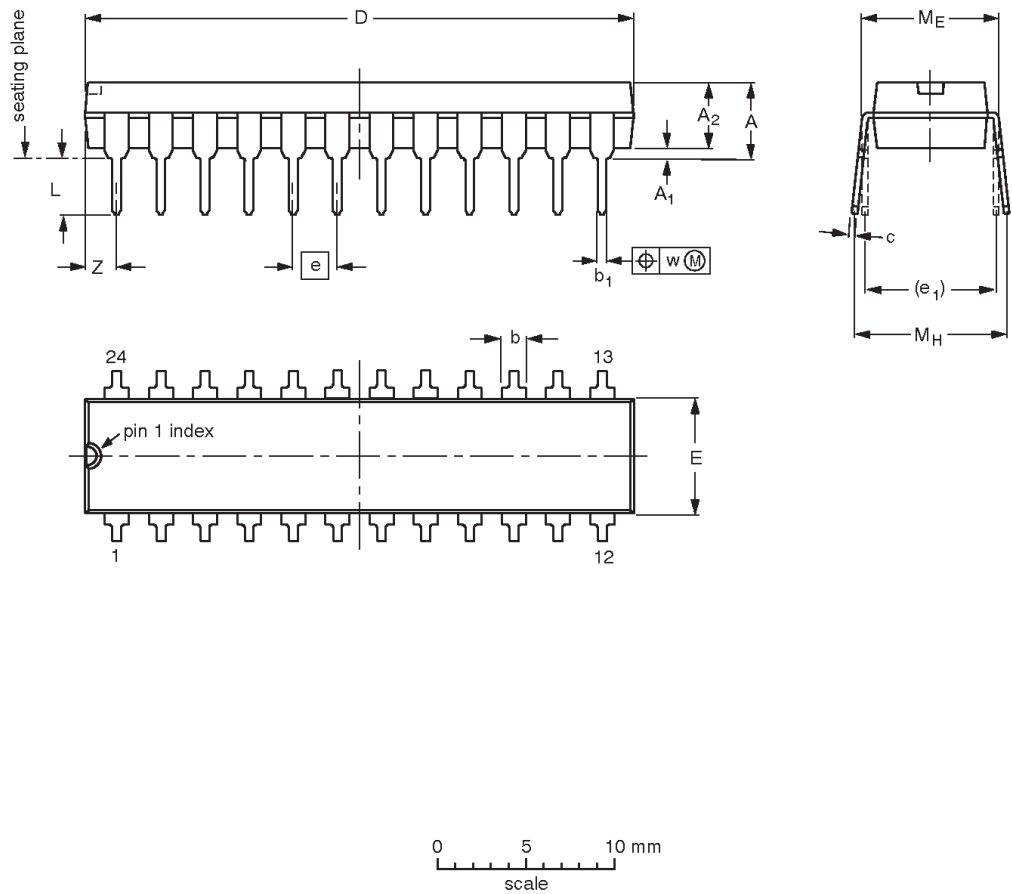


Octal buffer/driver with parity, non-inverting (3-State)

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DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

**Note**  
1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

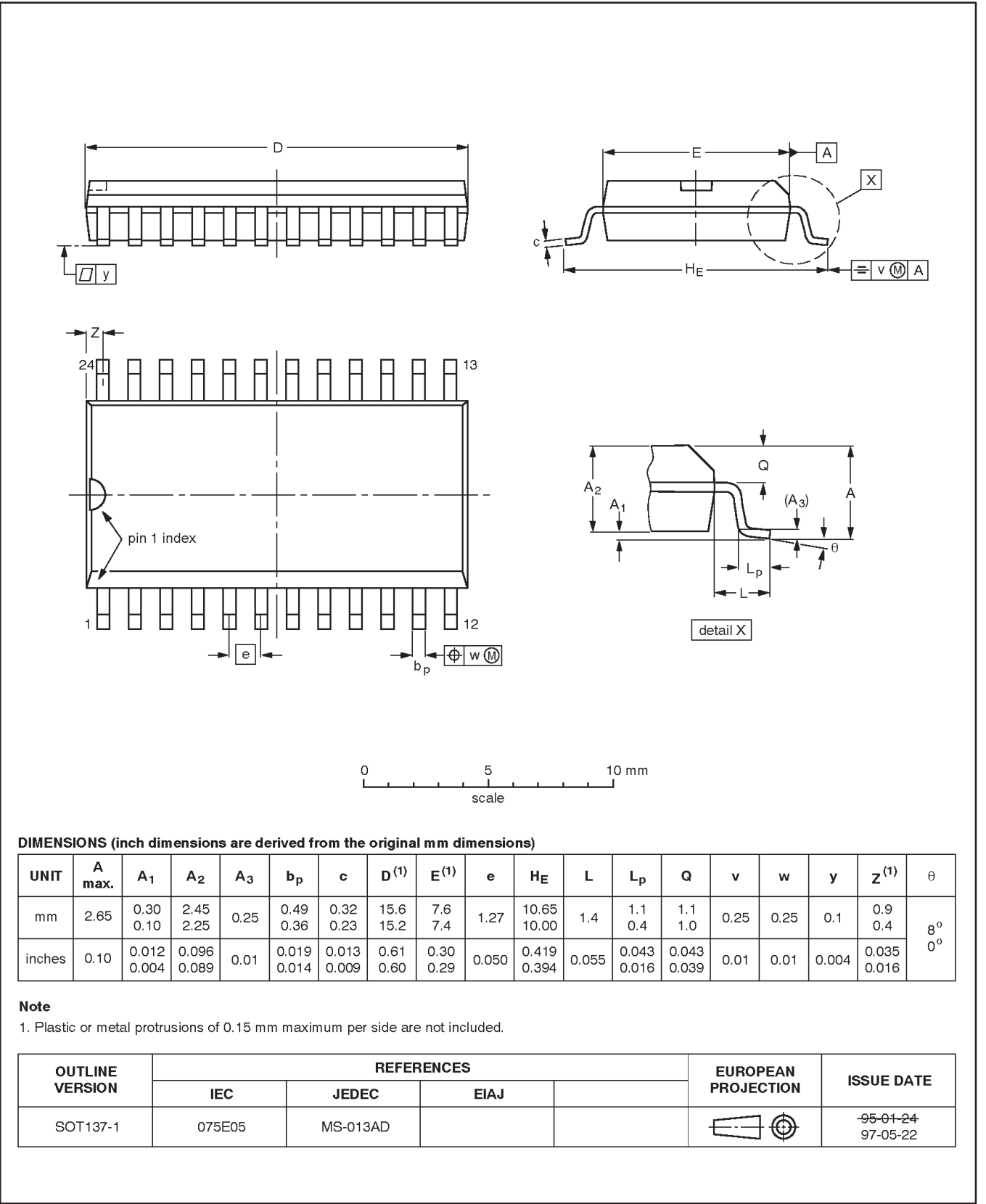


Octal buffer/driver with parity, non-inverting (3-State)

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SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



## Octal buffer/driver with parity, non-inverting (3-State)

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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