

# CMOS Dual 'D'-Type Flip-Flop

High-Voltage Types (20-Volt Rating)

■ CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and  $\bar{Q}$  outputs. These devices can be used for shift register applications, and, by connecting  $\bar{Q}$  output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

### RECOMMENDED OPERATING CONDITIONS

At  $T_A = 25^\circ\text{C}$ , Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC   | $V_{DD}$ (V) | LIMITS |      | UNITS         |
|--|--------------|--------|------|---------------|
|  |              | MIN.   | MAX. |               |
| Supply-Voltage Range<br>(For $T_A =$ Full Package Temperature Range) | —            | 3      | 18   | V             |
| Data Setup Time $t_S$  | 5            | 40     | —    | ns            |
|  | 10           | 20     | —    |               |
| Clock Pulse Width $t_W$  | 15           | 15     | —    | ns            |
|  | 5            | 140    | —    |               |
| Clock Input Frequency $f_{CL}$                                       | 10           | 60     | —    | ns            |
|  | 15           | 40     | —    |               |
| Clock Input Frequency $f_{CL}$                                       | 5            | —      | 3.5  | MHz           |
|  | 10           | dc     | 8    |               |
|  | 15           | —      | 12   |               |
| Clock Rise or Fall Time $t_{r,CL}, t_{f,CL}$                         | 5            | —      | 500  | $\mu\text{s}$ |
|  | 10           | —      | 30   |               |
|  | 15           | —      | 6    |               |
| Set or Reset Pulse Width $t_W$                                       | 5            | 180    | —    | ns            |
|  | 10           | 80     | —    |               |
|  | 15           | 50     | —    |               |

\*If more than one unit is cascaded in a parallel clocked operation,  $t_{r,CL}$  should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

# CD4013B Types

### Features:

- Set-Reset capability
- Static flip-flop operation — retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation — 16 MHz (typ.) clock toggle rate at 10V
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package temperature range; 100 nA at 18 V and  $25^\circ\text{C}$
- Noise margin (over full package temperature range):  
1 V at  $V_{DD}=5\text{ V}$   
2 V at  $V_{DD}=10\text{ V}$   
2.5 V at  $V_{DD}=15\text{ V}$
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

### Applications:

- Registers, counters, control circuits

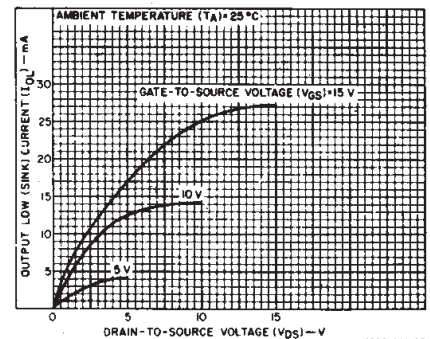
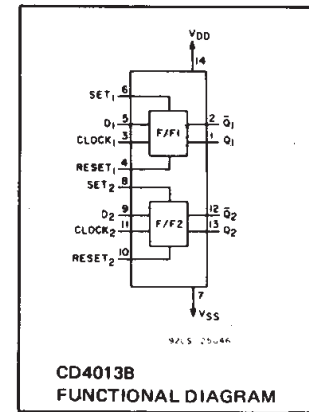


Fig. 1 — Typical output low (sink) current characteristics.

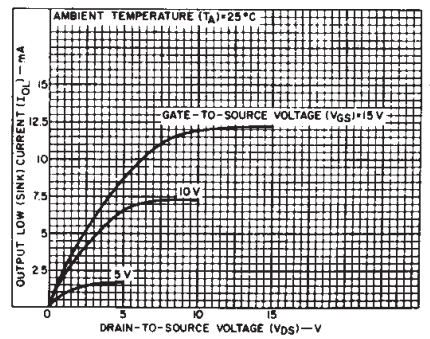


Fig. 2 — Minimum output low (sink) current characteristics.

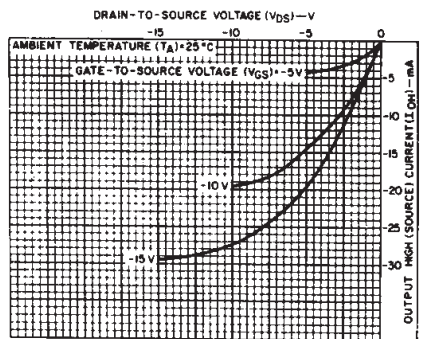


Fig. 3 — Typical output high (source) current characteristics.

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# CD4013B Types

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                     | CONDITIONS            |                        |                        | LIMITS AT INDICATED TEMPERATURES (°C) |       |       |       |       |                   |      | UNITS |
|--|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
|  | V <sub>O</sub><br>(V) | V <sub>IN</sub><br>(V) | V <sub>DD</sub><br>(V) | -55                                   | -40   | +85   | +125  | +25   |                   |      |       |
|  |                       |                        |                        |                                       |       |       |       | Min.  | Typ.              | Max. |       |
| Quiescent Device Current<br>I <sub>DD</sub> Max.   | —                     | 0.5                    | 5                      | 1                                     | 1     | 30    | 30    | —     | 0.02              | 1    | μA    |
|  | —                     | 0.10                   | 10                     | 2                                     | 2     | 60    | 60    | —     | 0.02              | 2    |       |
|  | —                     | 0.15                   | 15                     | 4                                     | 4     | 120   | 120   | —     | 0.02              | 4    |       |
|  | —                     | 0.20                   | 20                     | 20                                    | 20    | 600   | 600   | —     | 0.04              | 20   |       |
| Output Low (Sink) Current, I <sub>OL</sub> Min.    | 0.4                   | 0.5                    | 5                      | 0.64                                  | 0.61  | 0.42  | 0.36  | 0.51  | 1                 | —    | mA    |
|  | 0.5                   | 0.10                   | 10                     | 1.6                                   | 1.5   | 1.1   | 0.9   | 1.3   | 2.6               | —    |       |
|  | 1.5                   | 0.15                   | 15                     | 4.2                                   | 4     | 2.8   | 2.4   | 3.4   | 6.8               | —    |       |
| Output High (Source) Current, I <sub>OH</sub> Min. | 4.6                   | 0.5                    | 5                      | -0.64                                 | -0.61 | -0.42 | -0.36 | -0.51 | -1                | —    | mA    |
|  | 2.5                   | 0.5                    | 5                      | -2                                    | -1.8  | -1.3  | -1.15 | -1.6  | -3.2              | —    |       |
|  | 9.5                   | 0.10                   | 10                     | -1.6                                  | -1.5  | -1.1  | -0.9  | -1.3  | -2.6              | —    |       |
| Output Voltage: Low-Level, V <sub>OL</sub> Max.    | —                     | 0.5                    | 5                      | 0.05                                  |       |       |       | —     | 0                 | 0.05 | V     |
|  | —                     | 0.10                   | 10                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
|  | —                     | 0.15                   | 15                     | 0.05                                  |       |       |       | —     | 0                 | 0.05 |       |
| Output Voltage: High-Level, V <sub>OH</sub> Min.   | —                     | 0.5                    | 5                      | 4.95                                  |       |       |       | 4.95  | 5                 | —    | V     |
|  | —                     | 0.10                   | 10                     | 9.95                                  |       |       |       | 9.95  | 10                | —    |       |
|  | —                     | 0.15                   | 15                     | 14.95                                 |       |       |       | 14.95 | 15                | —    |       |
| Input Low Voltage, V <sub>IL</sub> Max.            | 0.5, 4.5              | —                      | 5                      | 1.5                                   |       |       |       | —     | —                 | 1.5  | V     |
|  | 1.9                   | —                      | 10                     | 3                                     |       |       |       | —     | —                 | 3    |       |
|  | 1.5, 13.5             | —                      | 15                     | 4                                     |       |       |       | —     | —                 | 4    |       |
| Input High Voltage, V <sub>IH</sub> Min.           | 0.5, 4.5              | —                      | 5                      | 3.5                                   |       |       |       | 3.5   | —                 | —    | V     |
|  | 1.9                   | —                      | 10                     | 7                                     |       |       |       | 7     | —                 | —    |       |
|  | 1.5, 13.5             | —                      | 15                     | 11                                    |       |       |       | 11    | —                 | —    |       |
| Input Current, I <sub>IN</sub> Max.                | —                     | 0.18                   | 18                     | ±0.1                                  | ±0.1  | ±1    | ±1    | —     | ±10 <sup>-5</sup> | ±0.1 | μA    |

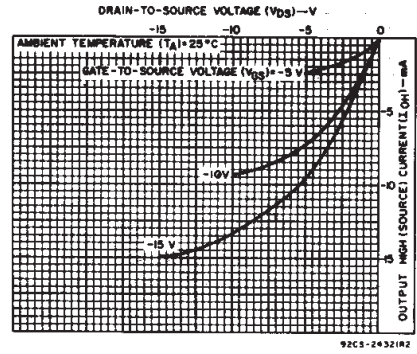


Fig. 4 — Minimum output high (source) current characteristics.

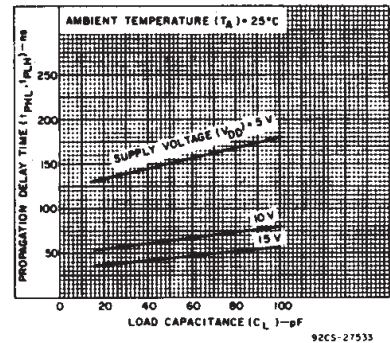


Fig. 5 — Typical propagation delay time vs. load capacitance (CLOCK or SET to Q, CLOCK or RESET to Q).

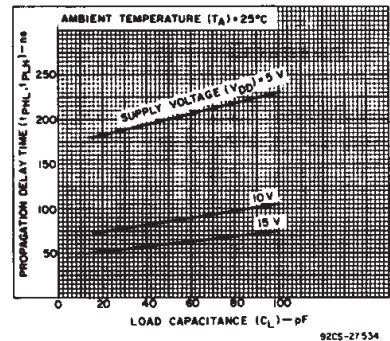


Fig. 6 — Typical propagation delay time vs. load capacitance (SET to Q or RESET to Q).

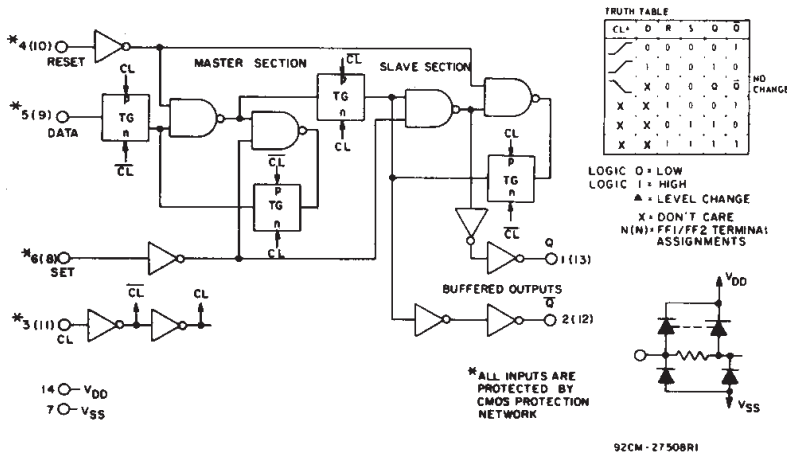


Fig. 7 — Logic diagram and truth table for CD4013B (one of two identical flip-flops).

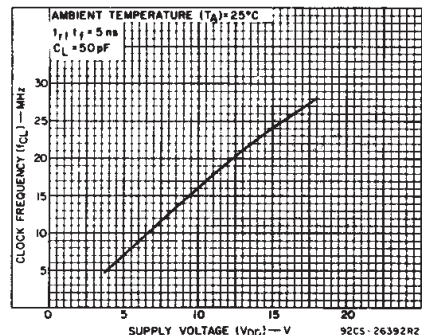


Fig. 8 — Typical maximum clock frequency vs. supply voltage.

# CD4013B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

### DC SUPPLY-VOLTAGE RANGE, (V<sub>DD</sub>)

Voltages referenced to V<sub>SS</sub> Terminal ..... -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V<sub>DD</sub> +0.5V

DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA

### POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):

For T<sub>A</sub> = -55°C to +100°C ..... 500mW

For T<sub>A</sub> = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW

### DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T<sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW

OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55°C to +125°C

STORAGE TEMPERATURE RANGE (T<sub>stg</sub>) ..... -65°C to +150°C

### LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

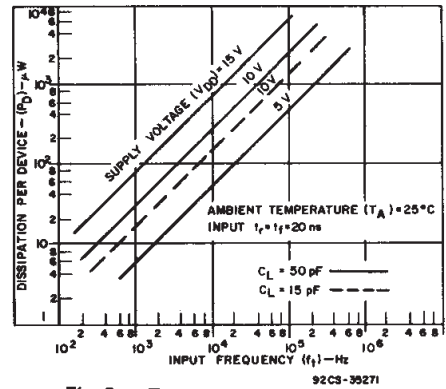


Fig. 9 – Typical power dissipation vs. frequency.

## TEST CIRCUITS

### DYNAMIC ELECTRICAL CHARACTERISTICS

At T<sub>A</sub> = 25°C; Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 20 kΩ

| CHARACTERISTIC  | TEST CONDITIONS<br>V <sub>DD</sub> (V) | LIMITS         |                 |                   | UNITS |
|---|--|----------------|-----------------|-------------------|-------|
|   |  | MIN.           | TYP.            | MAX.              |       |
| Propagation Delay Time:<br>Clock to Q or $\bar{Q}$ Outputs<br>t <sub>PHL</sub> , t <sub>PLH</sub> | 5<br>10<br>15                          | —<br>—<br>—    | 150<br>65<br>45 | 300<br>130<br>90  | ns    |
| Set to Q or Reset to $\bar{Q}$ t <sub>PLH</sub>   | 5<br>10<br>15                          | —<br>—<br>—    | 150<br>65<br>45 | 300<br>130<br>90  | ns    |
| Set to $\bar{Q}$ or Reset to Q t <sub>PHL</sub>   | 5<br>10<br>15                          | —<br>—<br>—    | 200<br>85<br>60 | 400<br>170<br>120 | ns    |
| Transition Time t <sub>THL</sub> , t <sub>TLH</sub>   | 5<br>10<br>15                          | —<br>—<br>—    | 100<br>50<br>40 | 200<br>100<br>80  | ns    |
| Maximum Clock Input<br>Frequency# f <sub>CL</sub>   | 5<br>10<br>15                          | 3.5<br>8<br>12 | 7<br>16<br>24   | —<br>—<br>—       | MHz   |
| Minimum Clock Pulse Width<br>t <sub>w</sub>   | 5<br>10<br>15                          | —<br>—<br>—    | 70<br>30<br>20  | 140<br>60<br>40   | ns    |
| Minimum Set or Reset Pulse<br>Width t <sub>w</sub>  | 5<br>10<br>15                          | —<br>—<br>—    | 90<br>40<br>25  | 180<br>80<br>50   | ns    |
| Minimum Data Setup Time t <sub>s</sub>  | 5<br>10<br>15                          | —<br>—<br>—    | 20<br>10<br>7   | 40<br>20<br>15    | ns    |
| Minimum Data Hold Time t <sub>h</sub>   | 5<br>10<br>15                          | —<br>—<br>—    | 2<br>2<br>2     | 5<br>5<br>5       | ns    |
| Clock Input Rise or Fall Time<br>t <sub>rCL</sub> , t <sub>fCL</sub>                              | 5<br>10<br>15                          | —<br>—<br>—    | —<br>—<br>—     | 500<br>30<br>6    | μs    |
| Input Capacitance C <sub>IN</sub>   | Any Input                              | —              | 5               | 7.5               | pF    |

#Input t<sub>r</sub>, t<sub>f</sub> = 5 ns.

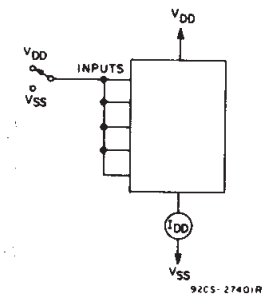


Fig. 10 – Quiescent device current.

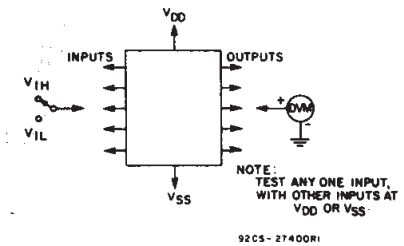


Fig. 11 – Input voltage.

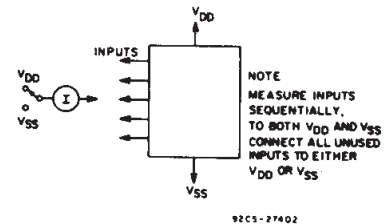


Fig. 12 – Input current.

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## CD4013B Types

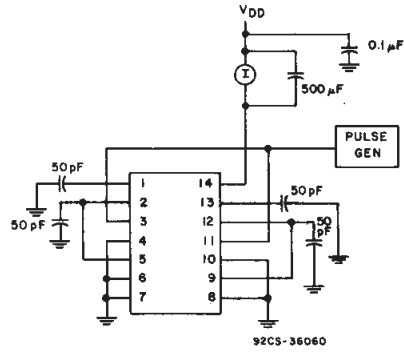
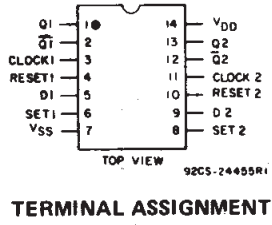
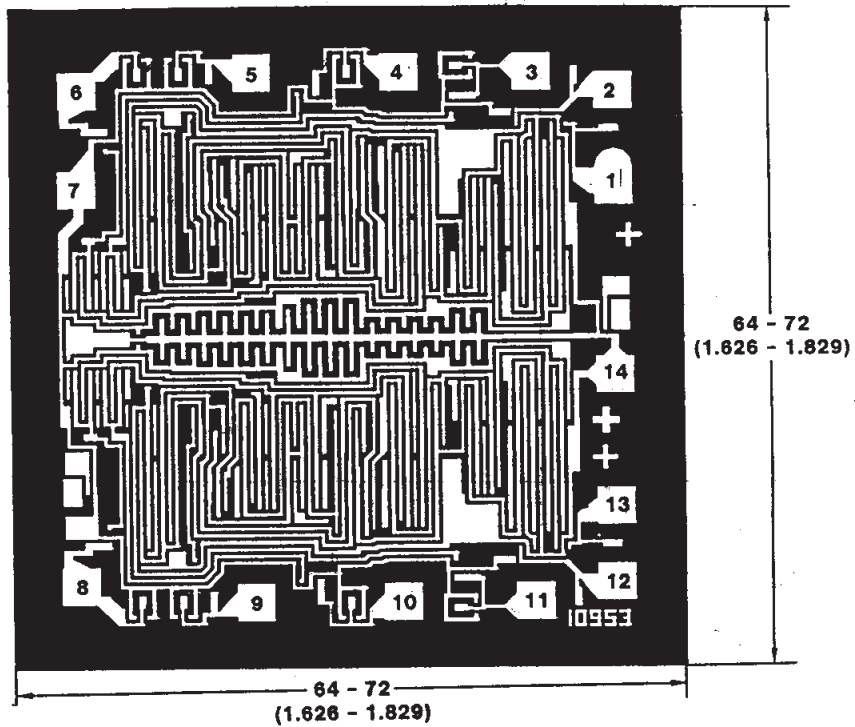


Fig. 13—Dynamic power dissipation test circuit.

### DIMENSIONS AND PAD LAYOUT FOR CD4013BH



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup>               |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|--|
| 89267AKB3T       | OBSOLETE              | CFP          | WR              | 14   |             | None                    | Call TI          | Call TI                                    |
| CD4013BE         | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | Level-NC-NC-NC                             |
| CD4013BF         | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | Call TI          | Level-NC-NC-NC                             |
| CD4013BF3A       | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | Call TI          | Level-NC-NC-NC                             |
| CD4013BM         | ACTIVE                | SOIC         | D               | 14   | 50          | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| CD4013BM96       | ACTIVE                | SOIC         | D               | 14   | 2500        | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| CD4013BMT        | ACTIVE                | SOIC         | D               | 14   | 250         | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| CD4013BNSR       | ACTIVE                | SO           | NS              | 14   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-2-260C-1 YEAR/<br>Level-1-235C-UNLIM |
| CD4013BPW        | ACTIVE                | TSSOP        | PW              | 14   | 90          | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM                         |
| CD4013BPWR       | ACTIVE                | TSSOP        | PW              | 14   | 2000        | Pb-Free (RoHS)          | CU NIPDAU        | Level-1-250C-UNLIM                         |
| JM38510/05151BCA | ACTIVE                | CDIP         | J               | 14   | 1           | None                    | Call TI          | Level-NC-NC-NC                             |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

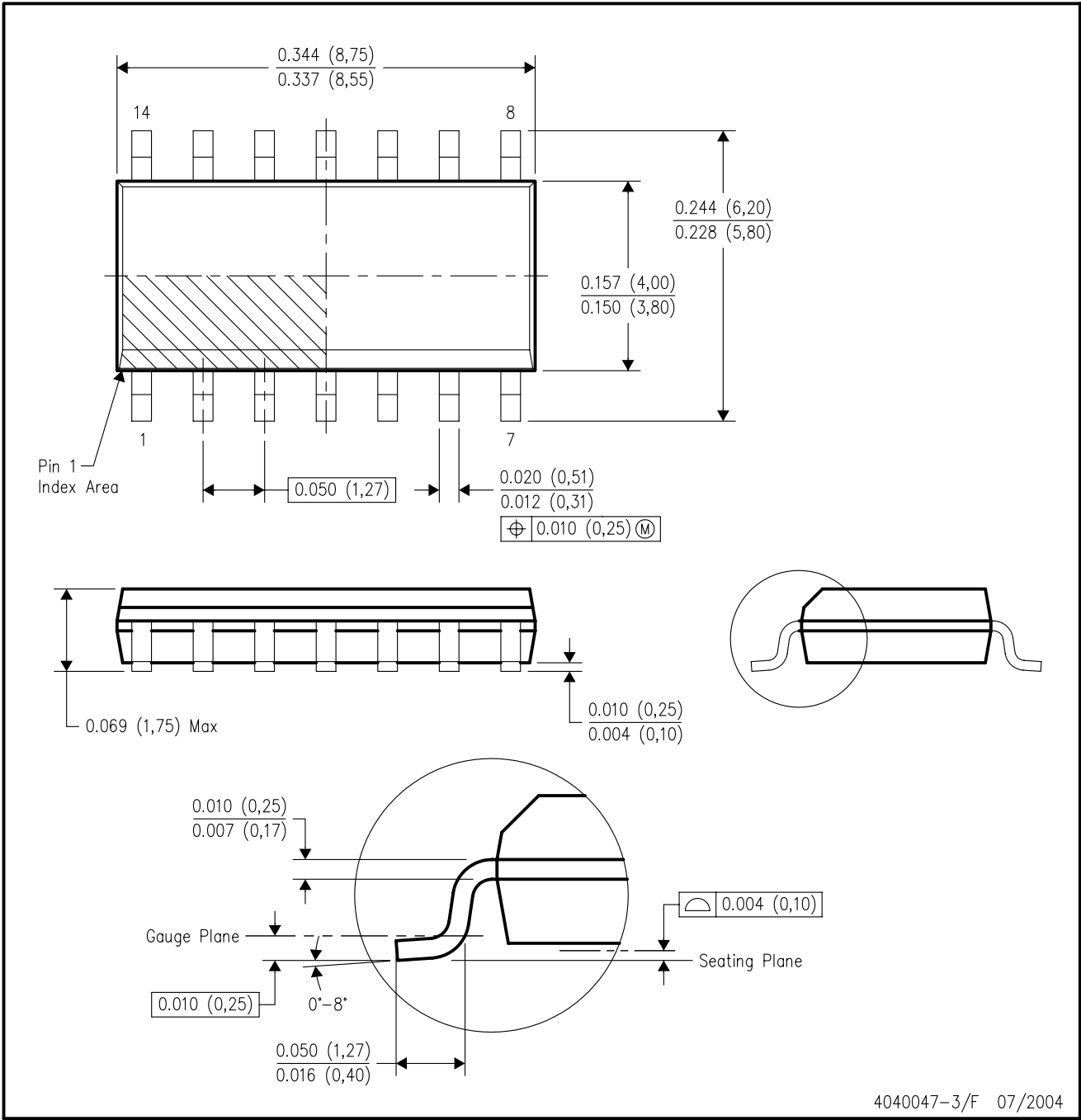
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AB.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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